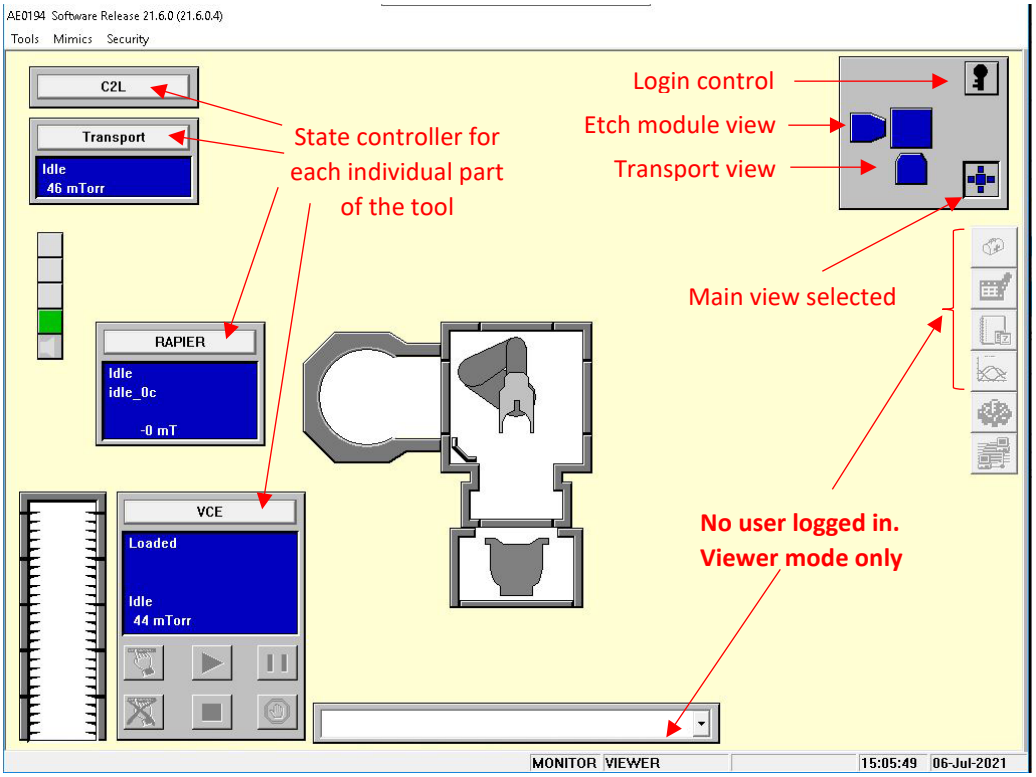
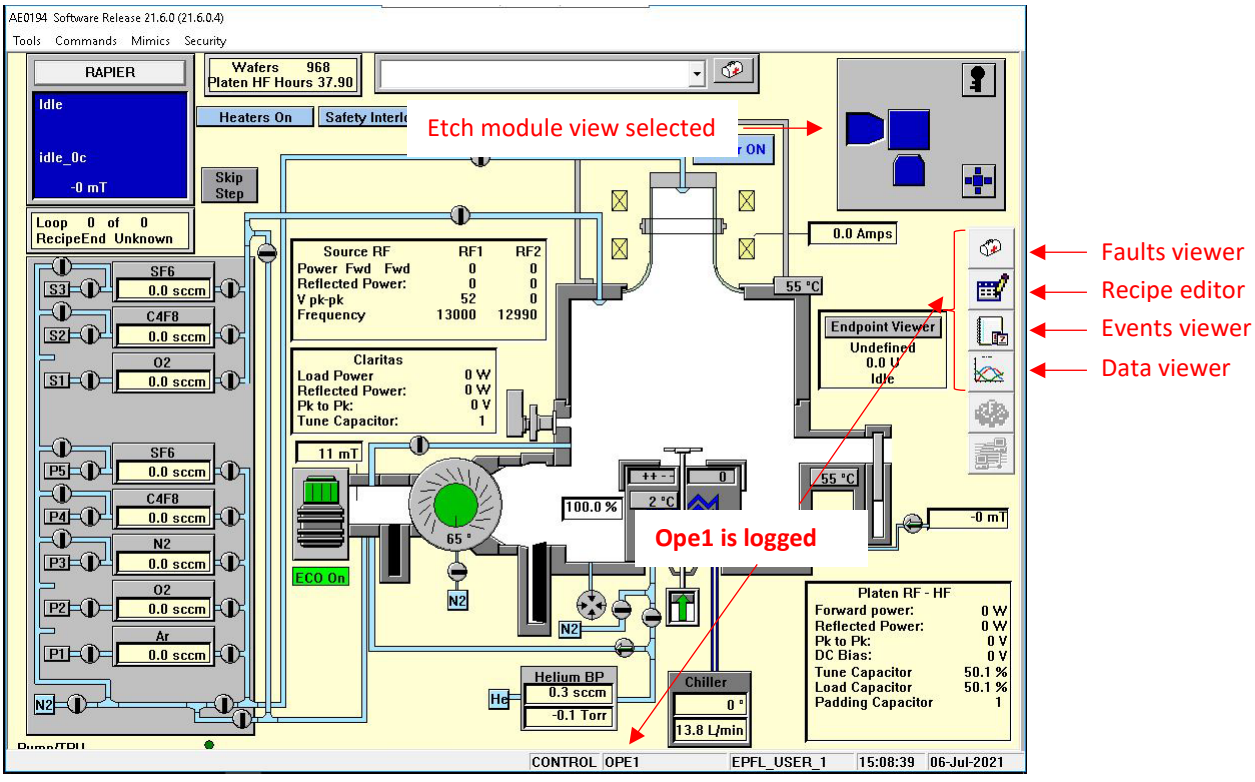
SPTS Rapier Silicon Etcher

Login, main view and control boxes



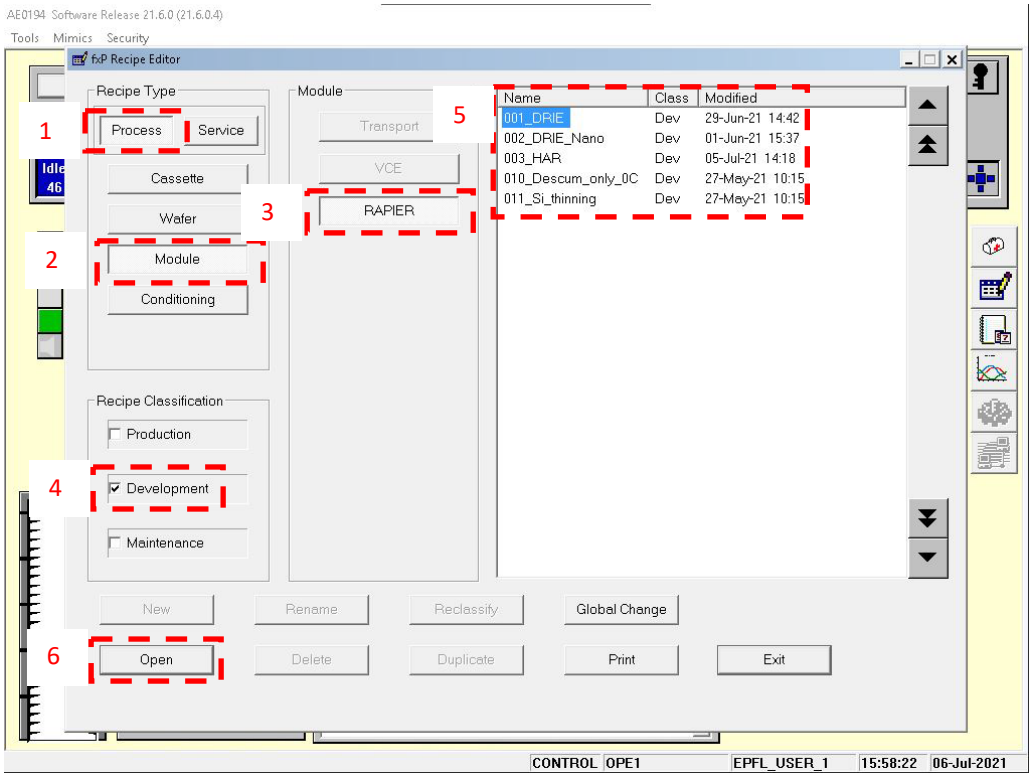
Log on software if necessary (auto logout after 30min) **Login ID:** **01**
Password: **01**

Select **main view** as starting point.



Recipe edition

Open the recipe editor, select **1 "Process"** & **2 "Module"** type recipe**, 3 "Rapier"** module and **4 "Development"** classification to shorten the list with only recipes of interest. **5 Select your recipe** in the list and click **6 "Open".**



For recipe names 00x_ (DRIE, HAR): ONLY modify the number of loops available at final step, do NOT edit process time in each step.

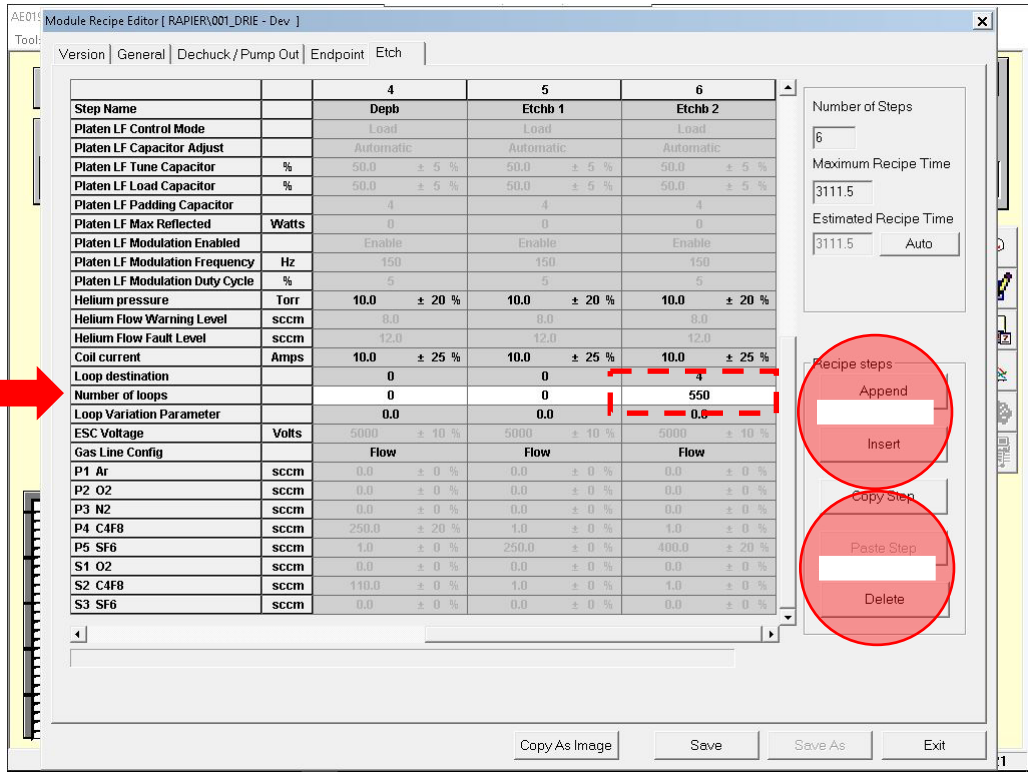
For recipe names 01x_: ONLY modify the process time of final step. These are continuous etching process so there's no loop number.

!!!! DO NOT **Append/Insert/Copy/Delete Steps** of recipes !!!!

"Save" and **"Exit"** until your reach software main view.

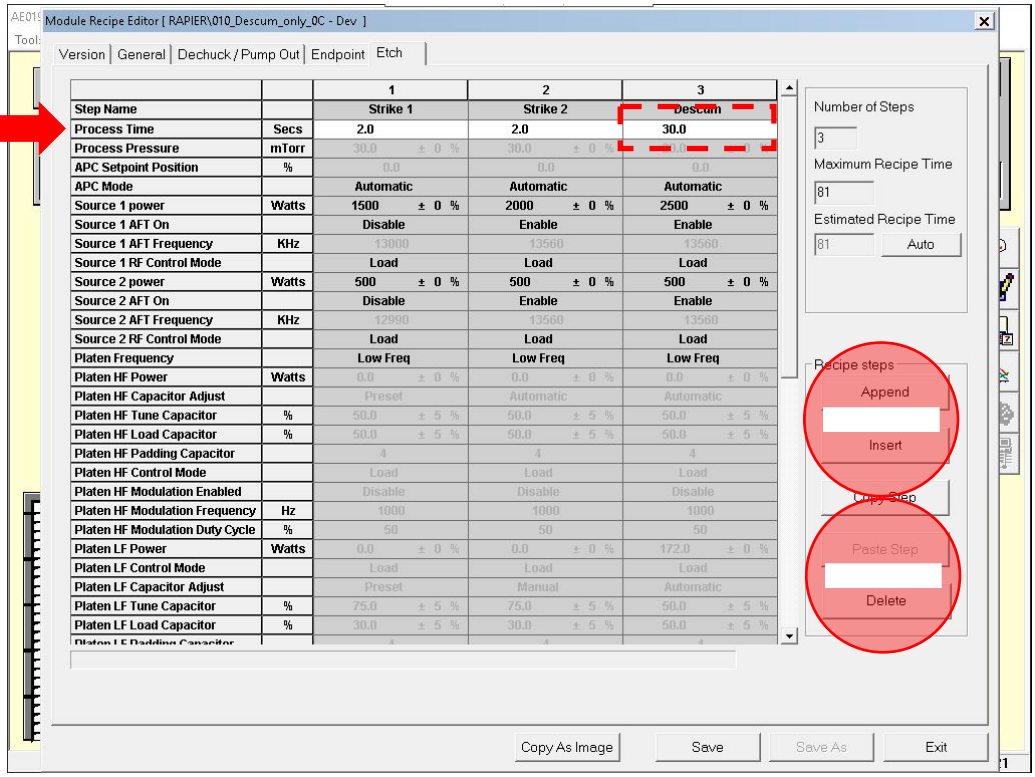
Process	Etch rates*	Remarks
DRIE	Trench 2um: 300nm/loop. Trench >200um: 800nm/loop.	If O_2 descum step: initial PR removal of 10nm/sec. Notch on SOI <300nm. PR etch rate 6nm/loop. SiO_2 etch rate 2.5nm/loop.
High Aspect Ratio (HAR)	Hole 10um: 200nm/loop. Trench 2um: 165nm/loop.	SiO_2 hard mask required (2.5nm/loop). Last 300nm of mask not viable because of faceting.
DRIE-Nano	Trench 350nm: 150nm/loop.	For sub-microns patterns. Scallops <50nm. Depth limited to tens of um.
Oxide_RIE	SiO_2: 235nm/min Si_3N_4: 110nm/min	PR etch rate 170nm/min. Thin layers only (<1um) & O2 cleaning compulsory.
Wafer thinning	4.4 um/min.	Uniformity +/- 3.5%.

* etch rates as design dependent (total surface load as well as local CD). Etch rate typically reduces in time and with increasing aspect ratio of the structure (ARDE).



For recipe names 00x_ (DRIE, HAR): ONLY modify the number of loops available at final step

!!!! DO NOT **Append/Insert/Copy/Delete Steps** of recipes !!!!

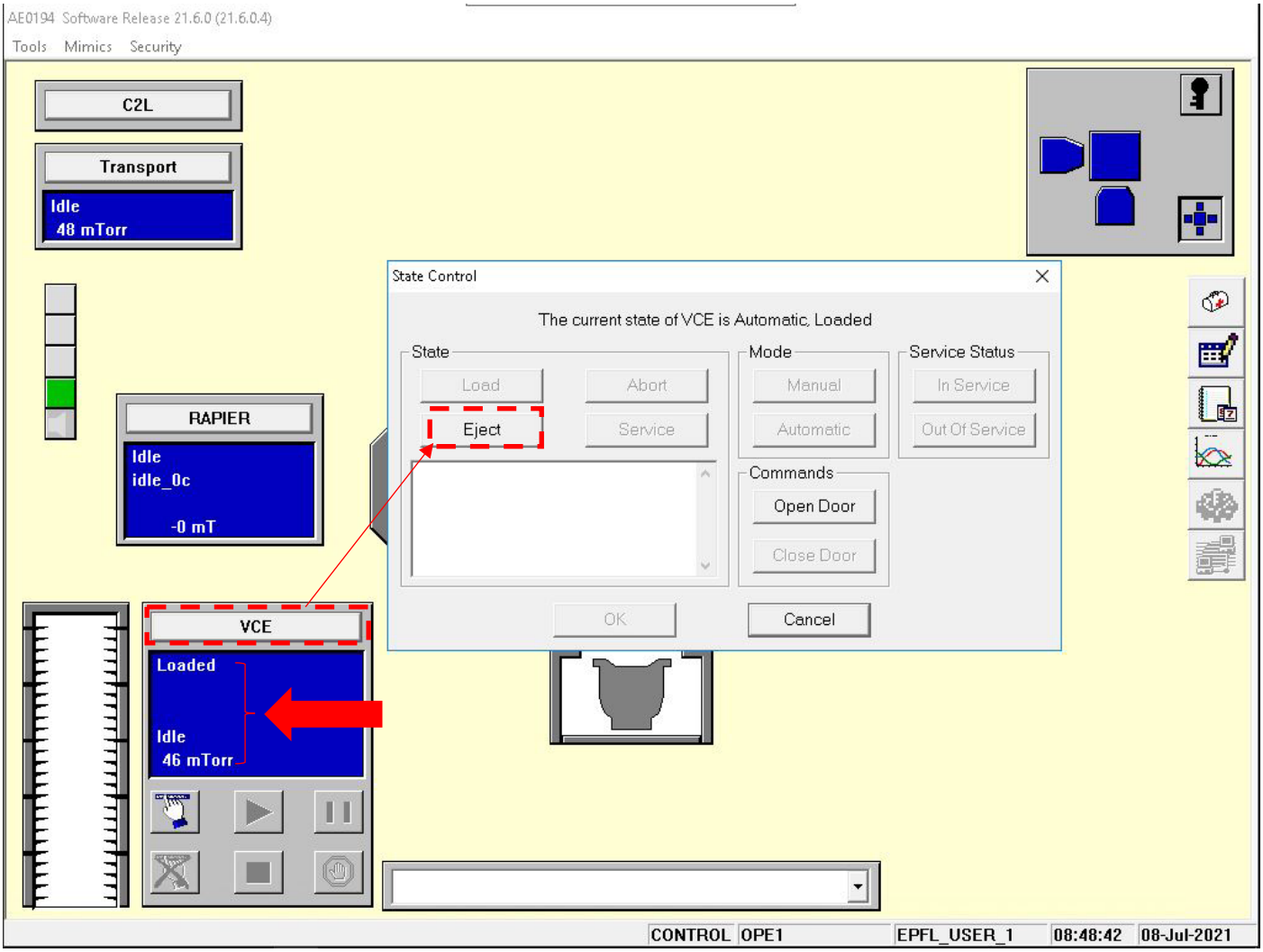


For recipe names 01x_: modify the process time of final step

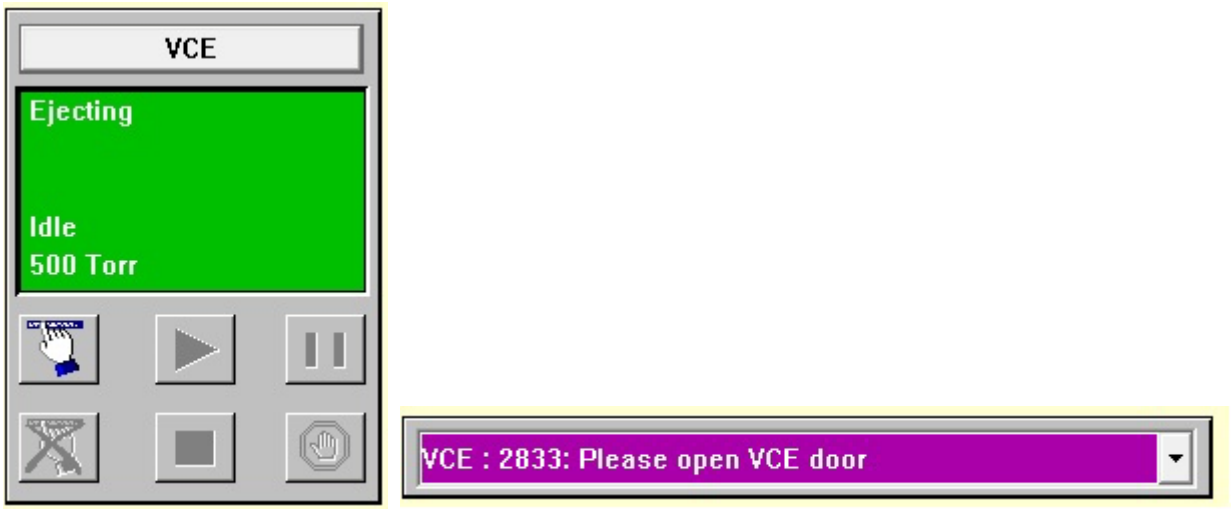
!!!! DO NOT **Append/Insert/Copy/Delete Steps** of recipes !!!!

Wafer loading and recipe start

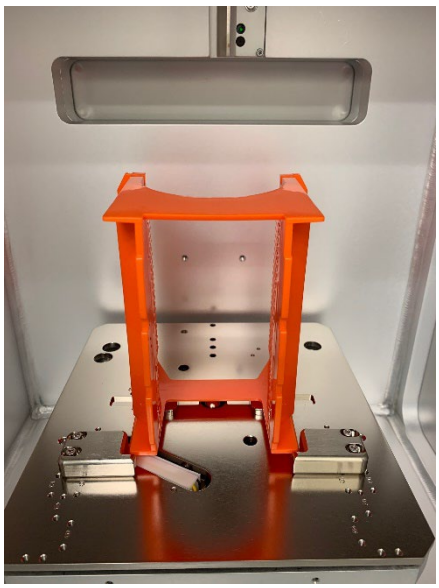
If the Vacuum Cassette Elevator **VCE** is under vacuum/loaded, open its **State Control** and click **“Eject”**, then **“OK”.**

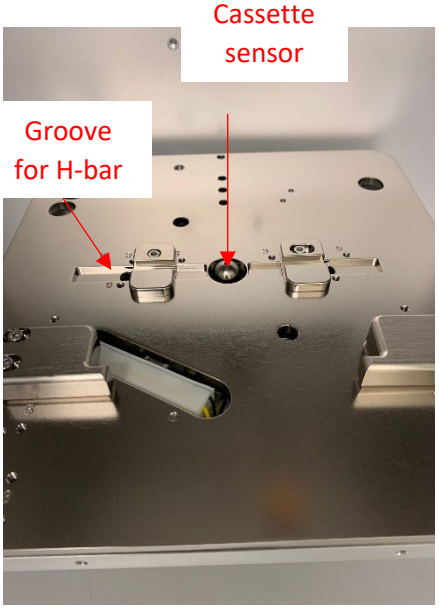


Wait for the VCE to confirm for door opening (1/8 turn counter-clockwise).

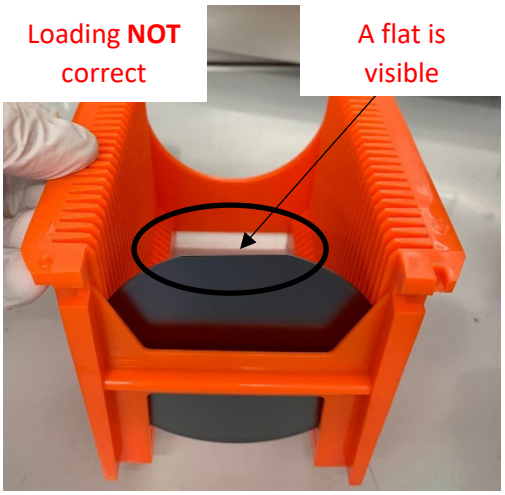


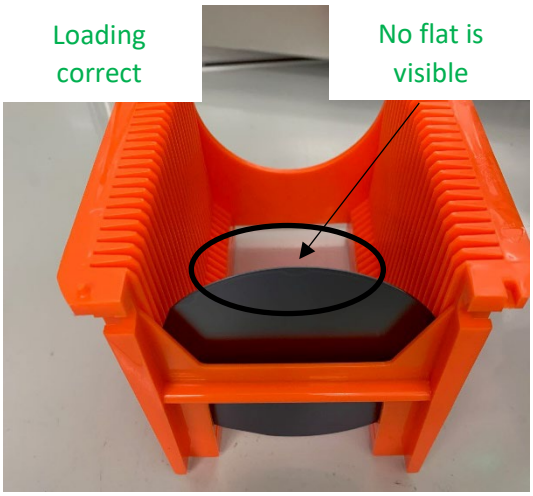
The cassette is positioned H-bar down, and at a fixed and calibrated position into a mechanical groove, pressing down on its presence sensor.





For correct optical detection of the wafer(s), the wafers must be loaded with no flat visible:





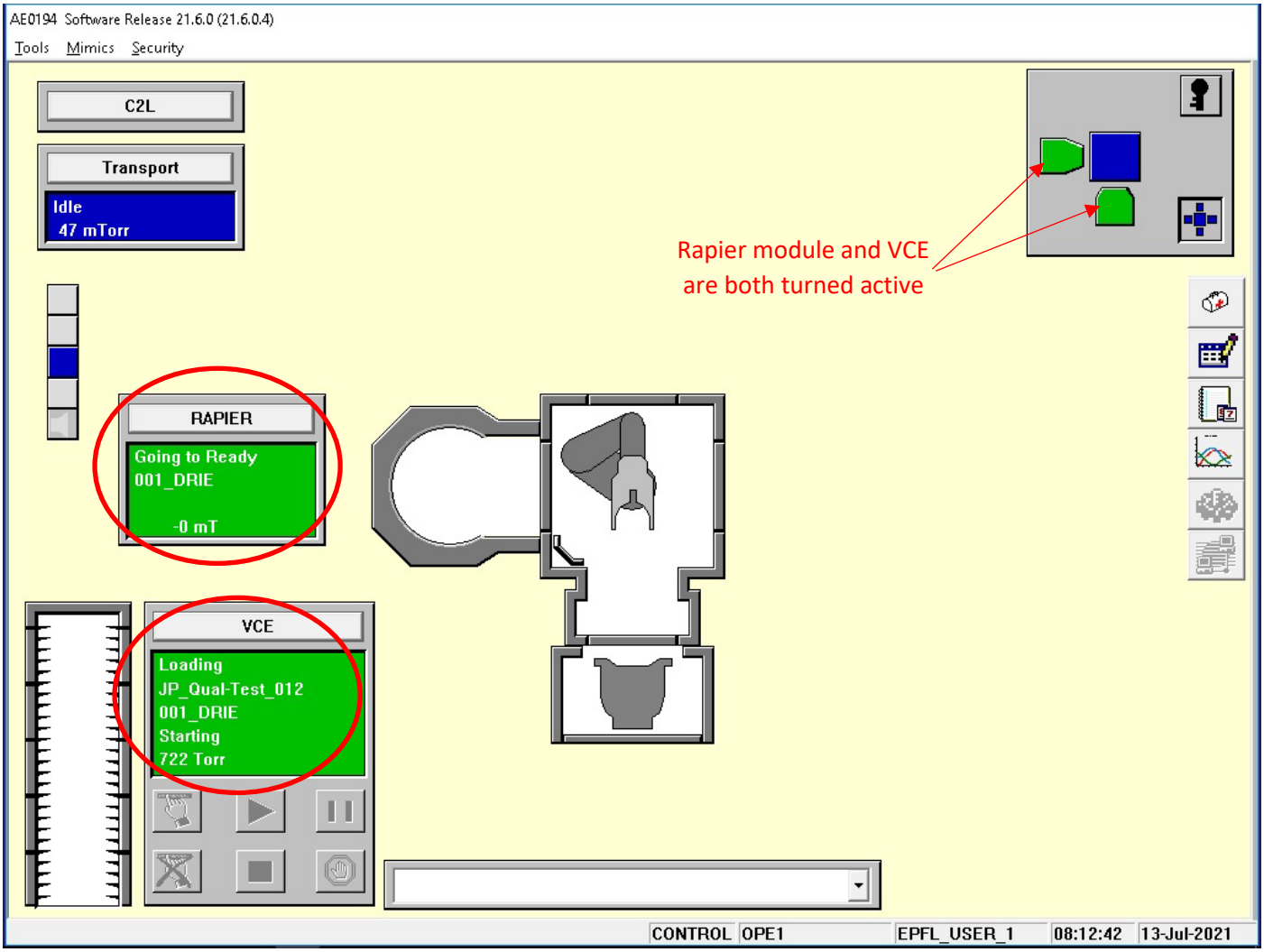
Place the cassette back in the **VCE** and lock the door (1/8 turn clockwise).

On the **VCE** control box, click  to **Select Cassette Recipe**.

Then press  and input a relevant **Lot ID.**

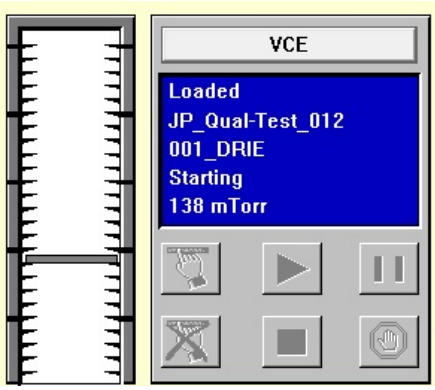
Finally **Confirm Recipe "START".**

Rapier chamber will automatically go to **Ready state**, and **VCE** will **Load** the cassette.

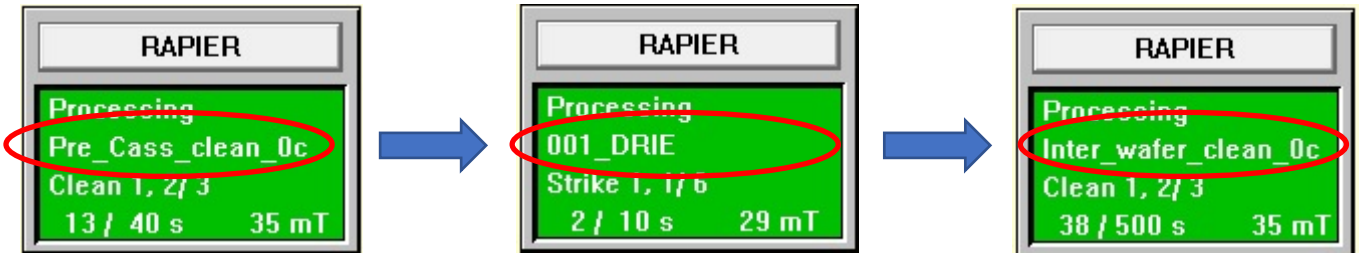


When **Loaded**, the **VCE** will show:

wafer(s) position(s)
Lot ID
Selected recipe

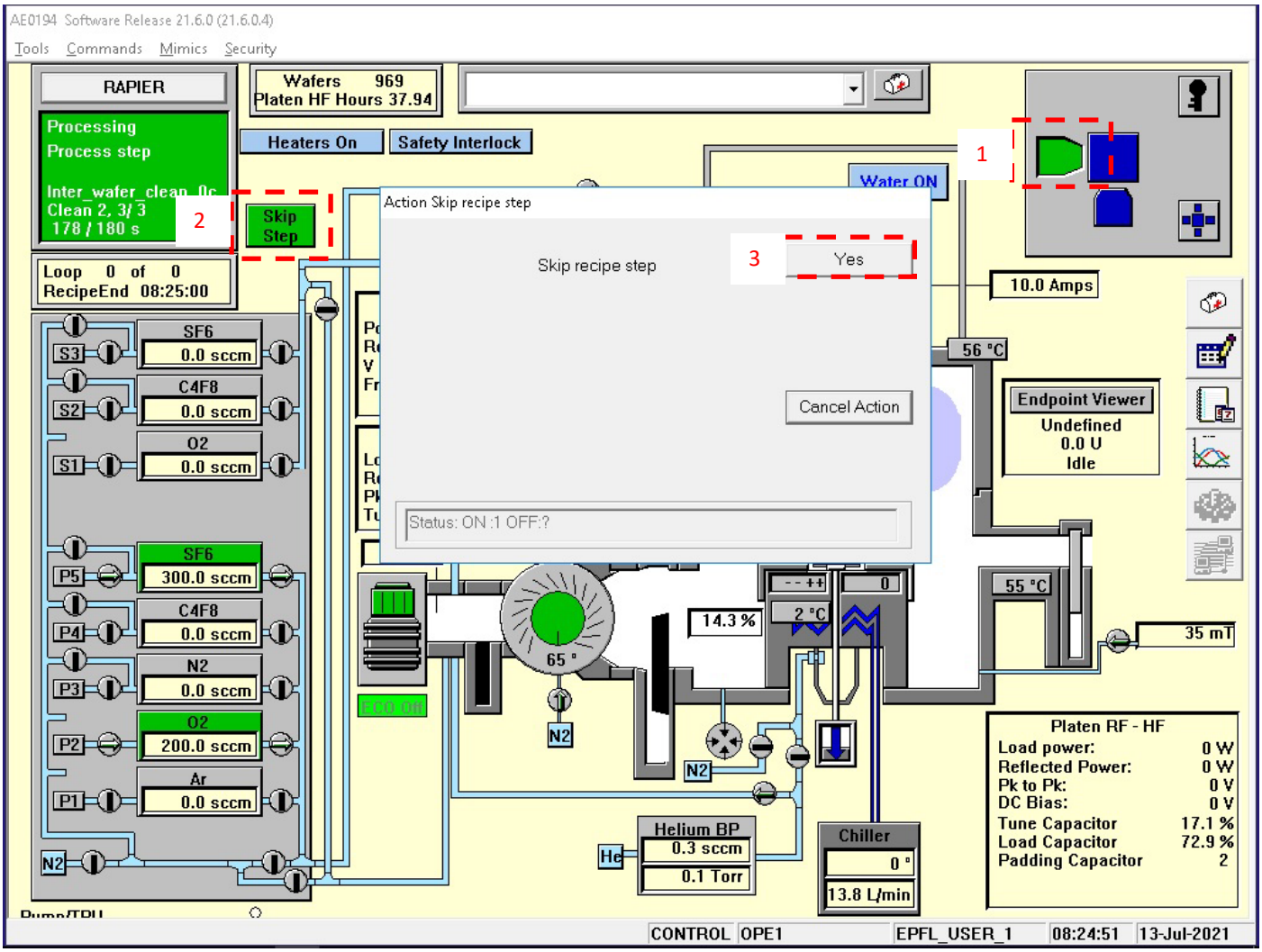


If applicable, pre-cassette, inter-wafer(s) and post-cassette cleaning/conditioning will automatically happen (wafer-less steps) in the **Rapier** chamber.



Anytime during process, it is possible to **Skip a Step**: from the main view, **1 Select etch module view**, click the **2 Skip Step** button, and **3 confirm the action.**

Skip Step is NOT advised to do on automatic pre-cassette, inter-wafer(s) and post-cassette cleaning/conditioning!



Wait for the **Rapier** module to be **Idle state** after process completion and for the **VCE** to confirm for door opening (1/8 turn counter-clockwise).

After collecting your wafers**,** place the cassette back in the **VCE** and in its appropriate position, and lock the door (1/8 turn clockwise).