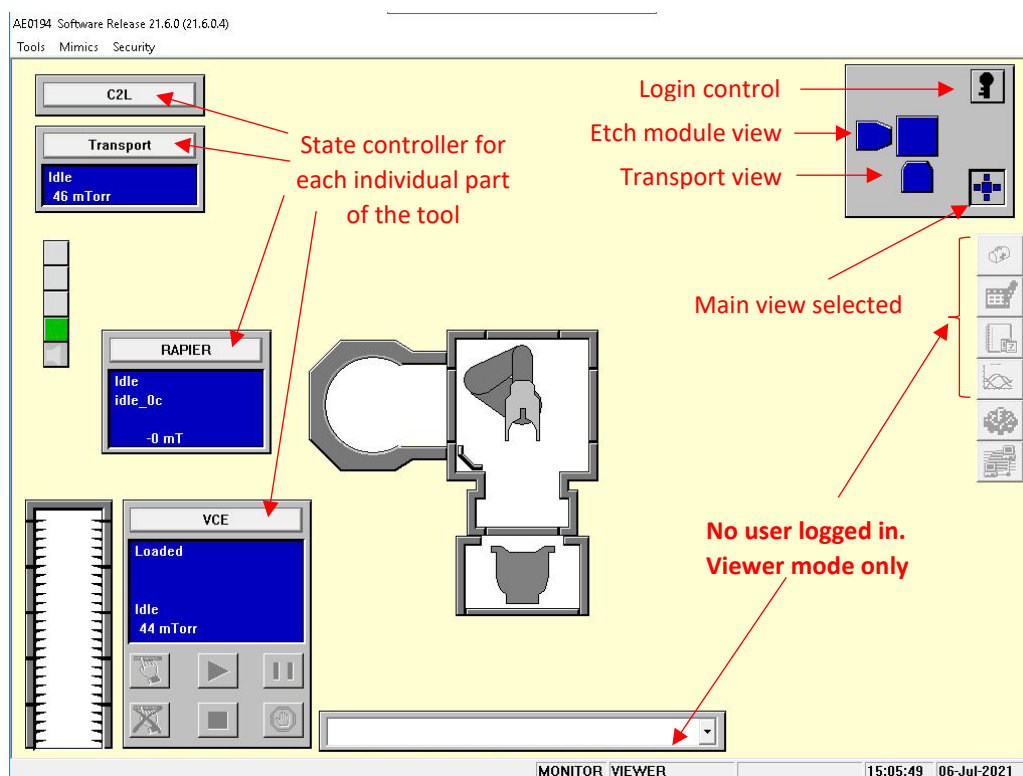
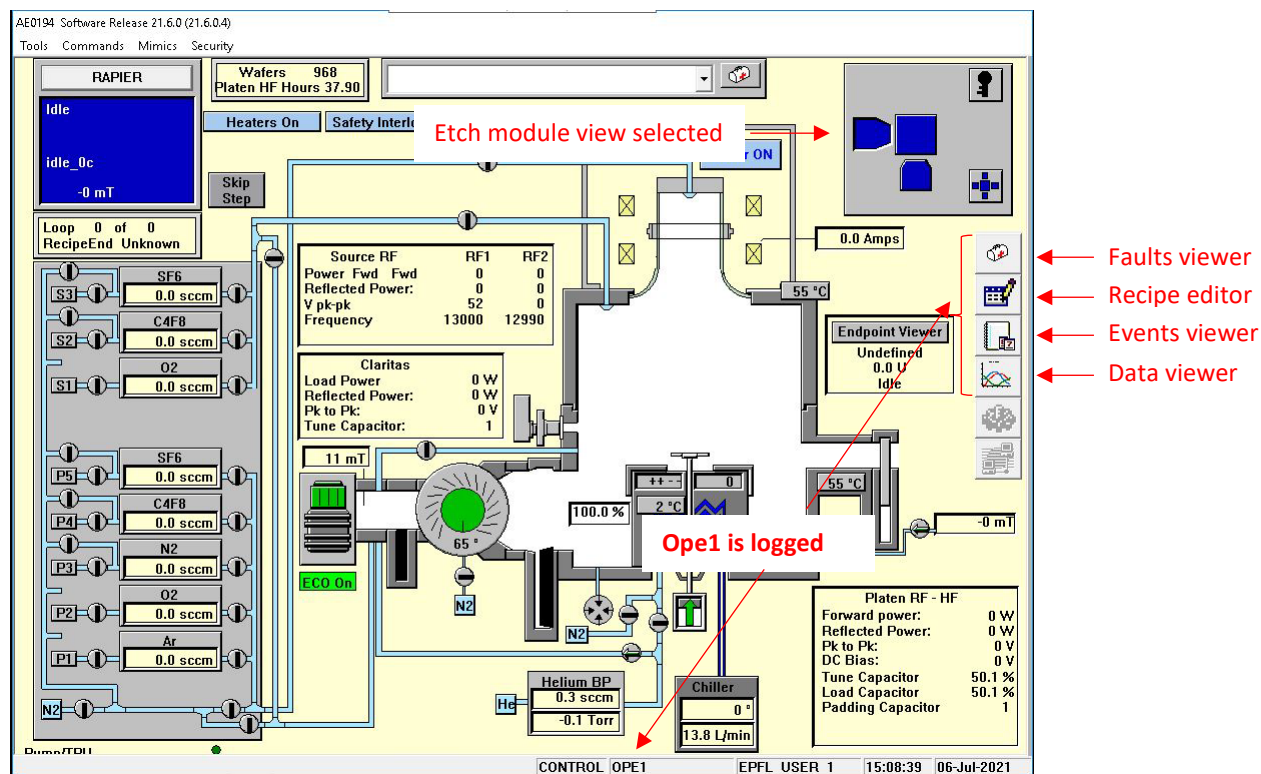


SPTS Rapier Silicon Etcher

Login, main view and control boxes

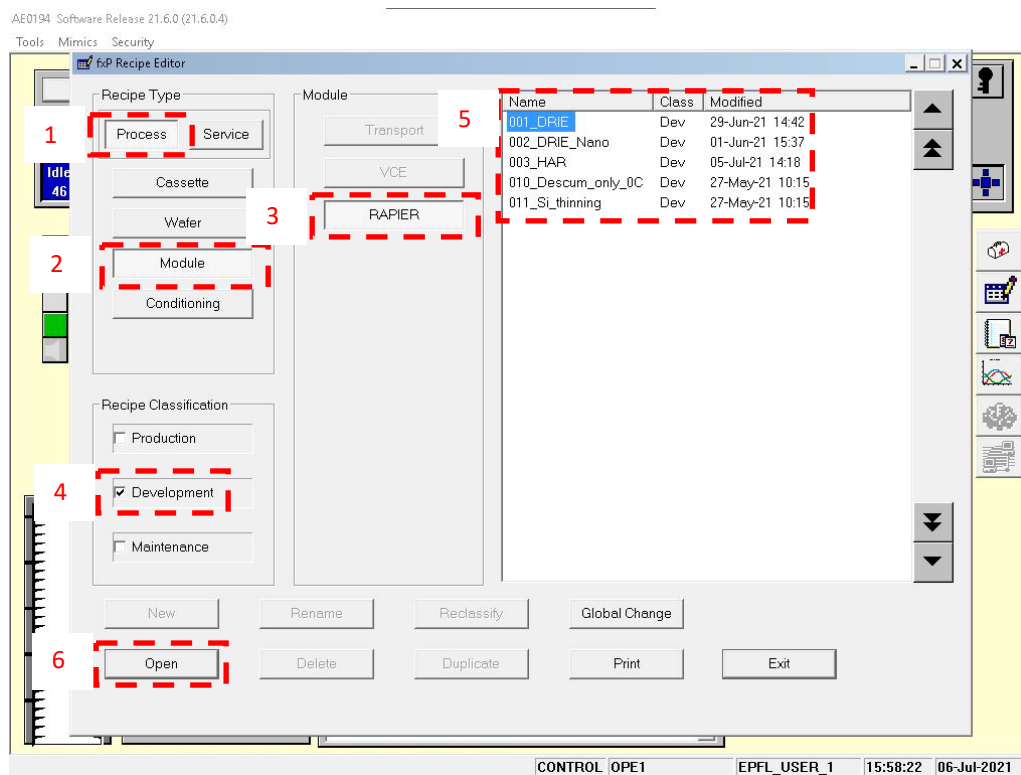
Log on software if necessary (auto logout after 30min) Login ID: 01
Password: 01

Select **main view** as starting point.



Recipe edition

Open the recipe editor, select **1 “Process”** & **2 “Module”** type recipe, **3 “Rapier”** module and **4 “Development”** classification to shorten the list with only recipes of interest. **5 Select your recipe** in the list and click **6 “Open”**.



For recipe names 00x_ (DRIE, HAR): ONLY modify the number of loops available at final step, do NOT edit process time in each step.

For recipe names 01x_: ONLY modify the process time of final step. These are continuous etching process so there's no loop number.

!!!! DO NOT Append/Insert/Copy/Delete Steps of recipes !!!!

“Save” and **“Exit”** until you reach software main view.

Process	Etch rates*	Remarks
DRIE	Trench 2um: 300nm/loop. Trench >200um: 800nm/loop.	If O ₂ descum step: initial PR removal of 10nm/sec. Notch on SOI <300nm. PR etch rate 6nm/loop. SiO ₂ etch rate 2.5nm/loop.
High Aspect Ratio (HAR)	Hole 10um: 200nm/loop. Trench 2um: 165nm/loop.	SiO ₂ hard mask required (2.5nm/loop). Last 300nm of mask not viable because of faceting.
DRIE-Nano	Trench 350nm: 150nm/loop.	For sub-microns patterns. Scallops <50nm. Depth limited to tens of um.
Oxide_RIE	SiO ₂ : 235nm/min Si ₃ N ₄ : 110nm/min	PR etch rate 170nm/min. Thin layers only (<1um) & O ₂ cleaning compulsory.
Wafer thinning	4.4 um/min.	Uniformity +/- 3.5%.

* etch rates as design dependent (total surface load as well as local CD). Etch rate typically reduces in time and with increasing aspect ratio of the structure (ARDE).

Module Recipe Editor [RAPIER\001_DRIE - Dev]

Version | General | Dechuck / Pump Out | Endpoint | Etch

Step Name		4	5	6
Platen LF Control Mode		Depb	Etchb 1	Etchb 2
Platen LF Capacitor Adjust		Automatic	Automatic	Automatic
Platen LF Tune Capacitor	%	50.0 ± 5 %	50.0 ± 5 %	50.0 ± 5 %
Platen LF Load Capacitor	%	50.0 ± 5 %	50.0 ± 5 %	50.0 ± 5 %
Platen LF Padding Capacitor		4	4	4
Platen LF Max Reflected	Watts	0	0	0
Platen LF Modulation Enabled		Enable	Enable	Enable
Platen LF Modulation Frequency	Hz	150	150	150
Platen LF Modulation Duty Cycle	%	5	5	5
Helium pressure	Torr	10.0 ± 20 %	10.0 ± 20 %	10.0 ± 20 %
Helium Flow Warning Level	sccm	8.0	8.0	8.0
Helium Flow Fault Level	sccm	12.0	12.0	12.0
Coil current	Amps	10.0 ± 25 %	10.0 ± 25 %	10.0 ± 25 %
Loop destination		0	0	4
Number of loops		0	0	550
Loop Variation Parameter		0.0	0.0	0.0
ESC Voltage	Volts	5000 ± 10 %	5000 ± 10 %	5000 ± 10 %
Gas Line Config		Flow	Flow	Flow
P1 Ar	sccm	0.0 ± 0 %	0.0 ± 0 %	0.0 ± 0 %
P2 O2	sccm	0.0 ± 0 %	0.0 ± 0 %	0.0 ± 0 %
P3 N2	sccm	0.0 ± 0 %	0.0 ± 0 %	0.0 ± 0 %
P4 C4F8	sccm	250.0 ± 20 %	1.0 ± 0 %	1.0 ± 0 %
P5 SF6	sccm	1.0 ± 0 %	250.0 ± 0 %	400.0 ± 20 %
S1 O2	sccm	0.0 ± 0 %	0.0 ± 0 %	0.0 ± 0 %
S2 C4F8	sccm	110.0 ± 0 %	1.0 ± 0 %	1.0 ± 0 %
S3 SF6	sccm	0.0 ± 0 %	0.0 ± 0 %	0.0 ± 0 %

Number of Steps: 6
Maximum Recipe Time: 3111.5
Estimated Recipe Time: 3111.5 Auto

Recipe steps:
Append
Insert
Copy Step
Paste Step
Delete

Copy As Image Save Save As Exit

For recipe names 00x_ (DRIE, HAR): ONLY modify the number of loops available at final step

!!!! DO NOT Append/Insert/Copy/Delete Steps of recipes !!!!

Module Recipe Editor [RAPIER\010_Descum_only_OC - Dev]

Version | General | Dechuck / Pump Out | Endpoint | Etch

Step Name		1	2	3
Process Time	Secs	2.0	2.0	30.0
Process Pressure	mTorr	30.0 ± 0 %	30.0 ± 0 %	30.0 ± 0 %
APC Setpoint Position	%	0.0	0.0	0.0
APC Mode		Automatic	Automatic	Automatic
Source 1 power	Watts	1500 ± 0 %	2000 ± 0 %	2500 ± 0 %
Source 1 AFT On		Disable	Enable	Enable
Source 1 AFT Frequency	KHz	13000	13500	13500
Source 1 RF Control Mode		Load	Load	Load
Source 2 power	Watts	500 ± 0 %	500 ± 0 %	500 ± 0 %
Source 2 AFT On		Disable	Enable	Enable
Source 2 AFT Frequency	KHz	12900	13500	13500
Source 2 RF Control Mode		Load	Load	Load
Platen Frequency		Low Freq	Low Freq	Low Freq
Platen HF Power	Watts	0.0 ± 0 %	0.0 ± 0 %	0.0 ± 0 %
Platen HF Capacitor Adjust		Preset	Automatic	Automatic
Platen HF Tune Capacitor	%	50.0 ± 5 %	50.0 ± 5 %	50.0 ± 5 %
Platen HF Load Capacitor	%	50.0 ± 5 %	50.0 ± 5 %	50.0 ± 5 %
Platen HF Padding Capacitor		4	4	4
Platen HF Control Mode		Load	Load	Load
Platen HF Modulation Enabled		Disable	Disable	Disable
Platen HF Modulation Frequency	Hz	1000	1000	1000
Platen HF Modulation Duty Cycle	%	50	50	50
Platen LF Power	Watts	0.0 ± 0 %	0.0 ± 0 %	172.0 ± 0 %
Platen LF Control Mode		Load	Load	Load
Platen LF Capacitor Adjust		Preset	Manual	Automatic
Platen LF Tune Capacitor	%	75.0 ± 5 %	75.0 ± 5 %	50.0 ± 5 %
Platen LF Load Capacitor	%	30.0 ± 5 %	30.0 ± 5 %	50.0 ± 5 %
Platen LF Padding Capacitor		4	4	4

Number of Steps: 3
Maximum Recipe Time: 81
Estimated Recipe Time: 81 Auto

Recipe steps:
Append
Insert
Copy Step
Paste Step
Delete

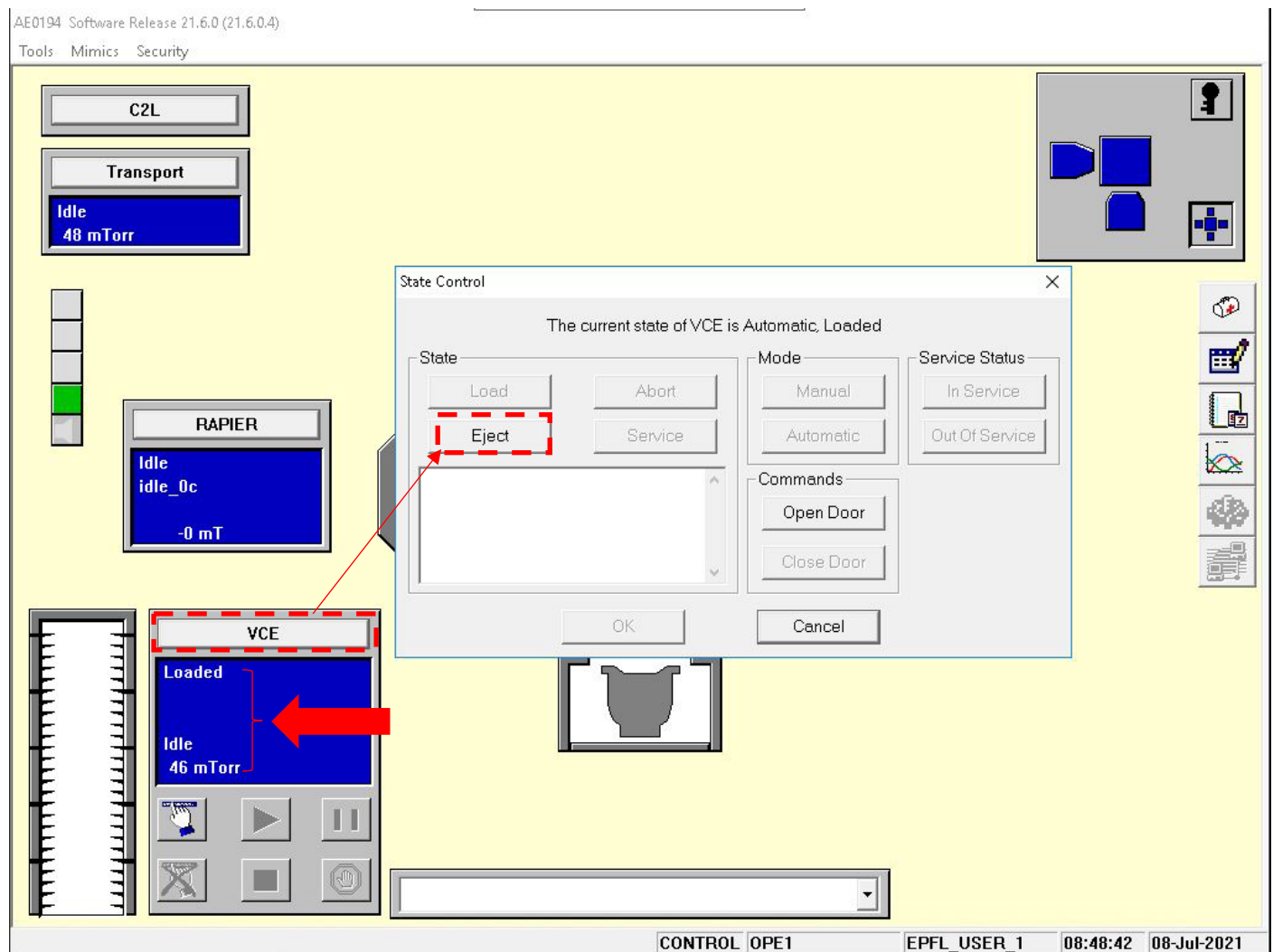
Copy As Image Save Save As Exit

For recipe names 01x_: modify the process time of final step

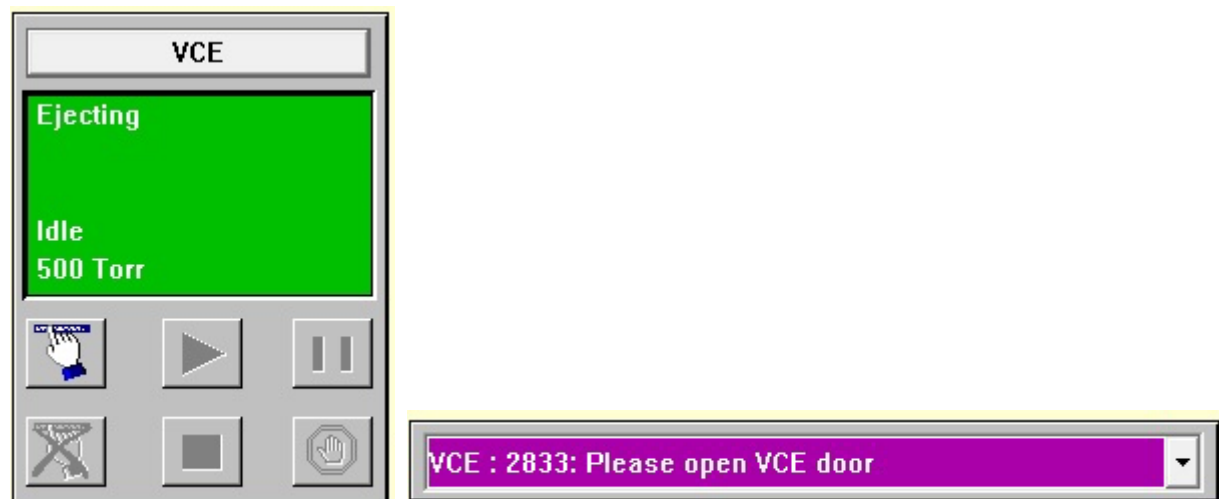
!!!! DO NOT Append/Insert/Copy/Delete Steps of recipes !!!!

Wafer loading and recipe start

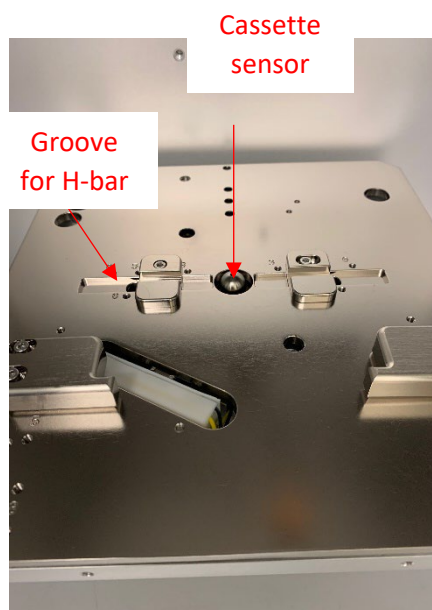
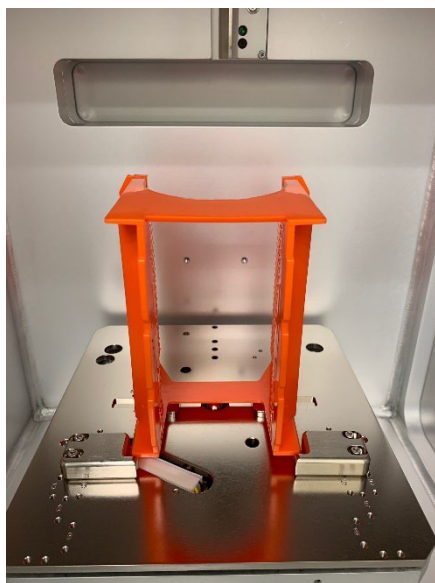
If the Vacuum Cassette Elevator **VCE** is under vacuum/loaded, open its **State Control** and click “**Eject**”, then “**OK**”.



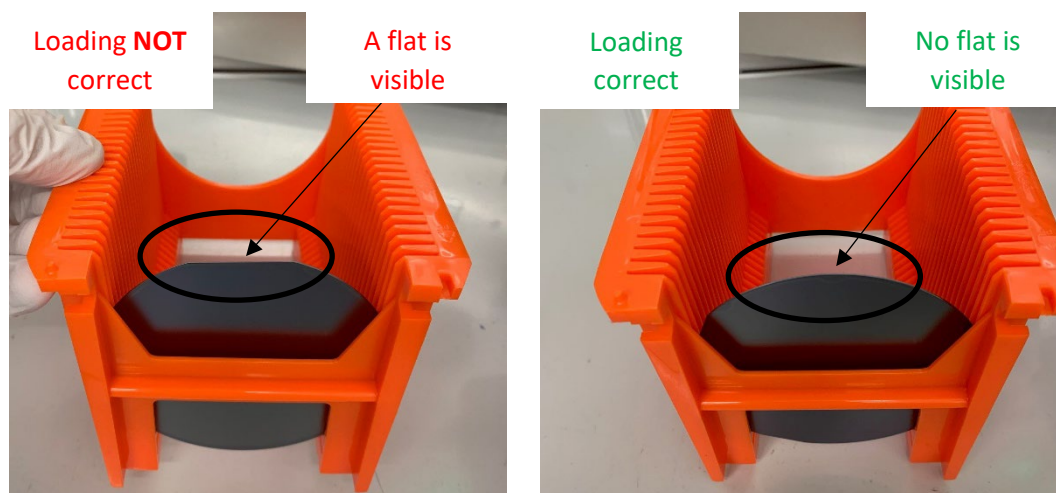
Wait for the VCE to confirm for door opening (1/8 turn counter-clockwise).



The cassette is positioned H-bar down, and at a fixed and calibrated position into a mechanical groove, pressing down on its presence sensor.




For correct optical detection of the wafer(s), the wafers must be loaded with no flat visible:



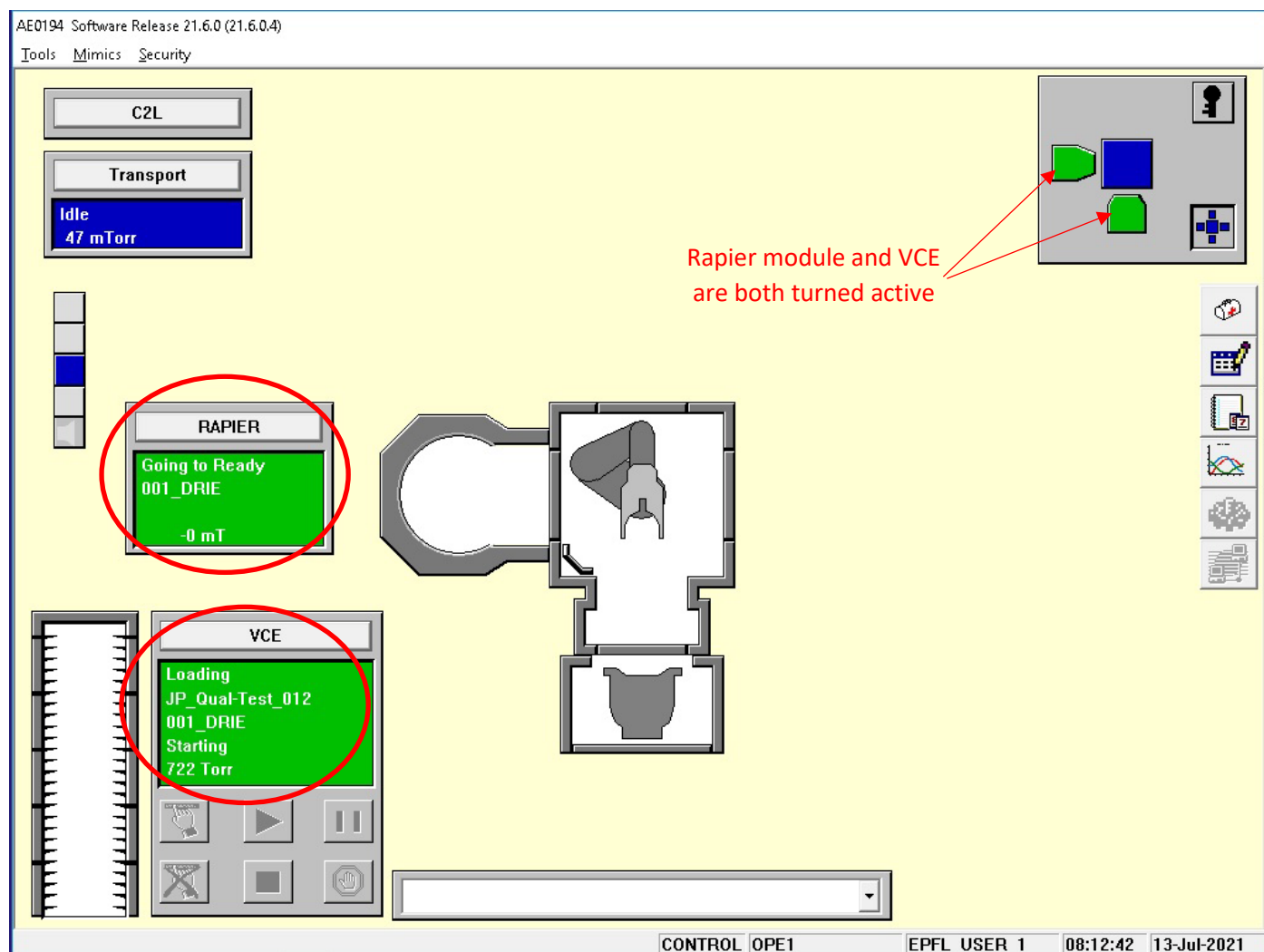
Place the cassette back in the **VCE** and lock the door (1/8 turn clockwise).

On the **VCE** control box, click  to **Select Cassette Recipe**.

Then press  and input a relevant **Lot ID**.

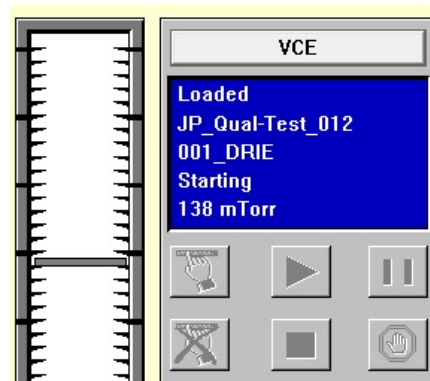
Finally **Confirm Recipe "START"**.

Rapier chamber will automatically go to **Ready state**, and **VCE** will **Load** the cassette.

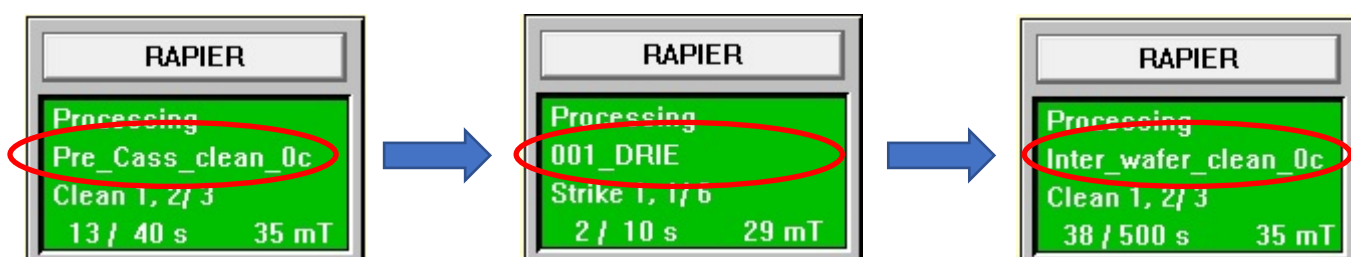


When **Loaded**, the **VCE** will show:

wafer(s) position(s)
Lot ID
Selected recipe

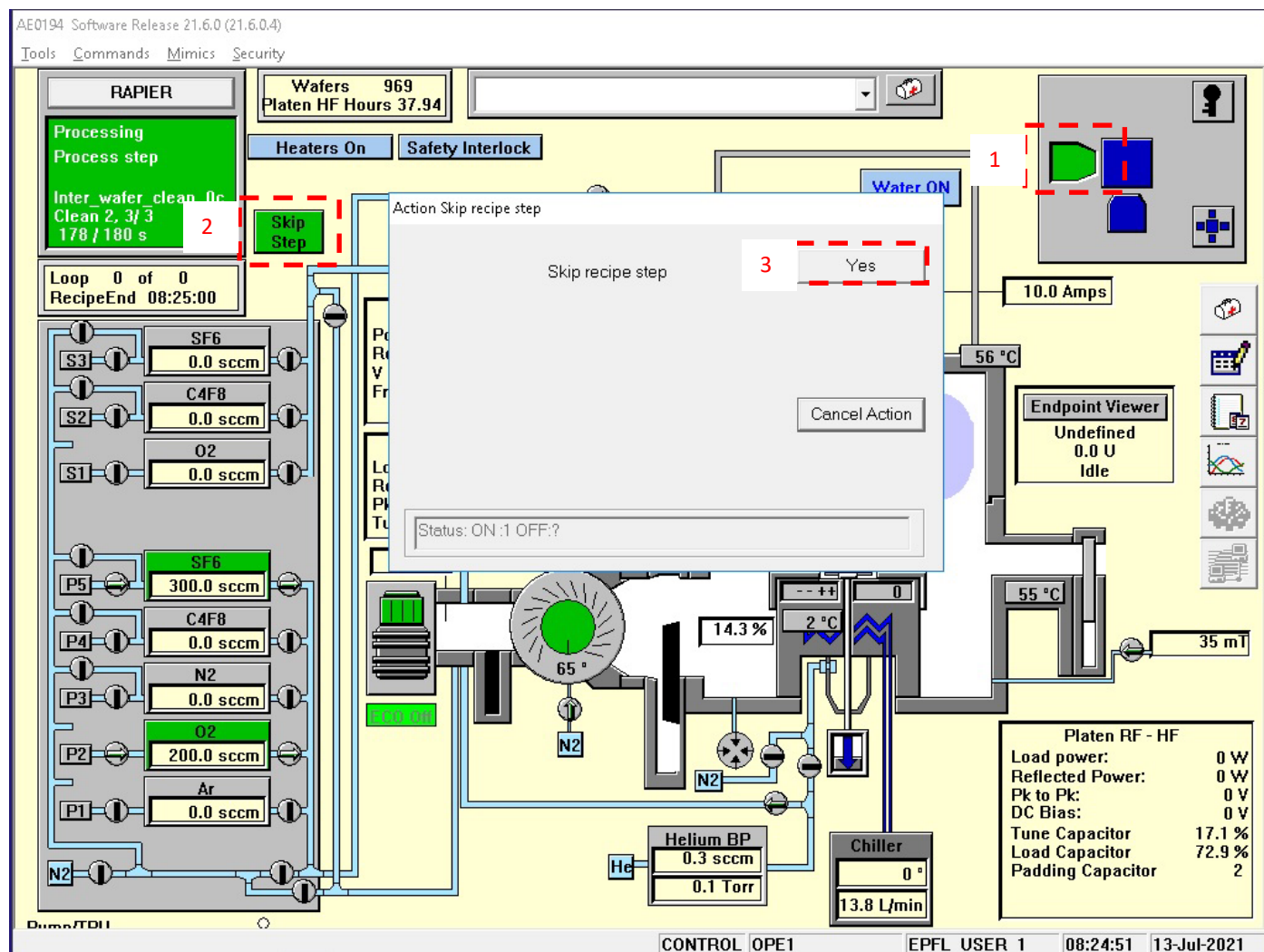


If applicable, pre-cassette, inter-wafer(s) and post-cassette cleaning/conditioning will automatically happen (wafer-less steps) in the **Rapier** chamber.



Anytime during process, it is possible to **Skip a Step**: from the main view, **1 Select etch module view**, click the **2 Skip Step** button, and **3 confirm the action**.

Skip Step is NOT advised to do on automatic pre-cassette, inter-wafer(s) and post-cassette cleaning/conditioning!



Wait for the **Rapier** module to be **Idle state** after process completion and for the **VCE** to confirm for door opening (1/8 turn counter-clockwise).



After collecting your wafers, place the cassette back in the **VCE** and in its appropriate position, and lock the door (1/8 turn clockwise).