**JAMES R. LARUS**

September 2020

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## Education

Ph.D. (Computer Science), University of California at Berkeley, May 1989. Thesis: *Restructuring Symbolic Programs for Concurrent Execution on Multiprocessors*. Advisor: Paul Hilfinger.

M.S. (Computer Science), University of California at Berkeley, December 1982. Thesis: *Glean: An Interactive Program Analysis System for Franz Lisp.* Advisor: Richard Fateman.

A.B. *magna cum laude* (Applied Mathematics), Harvard University, June 1980.

## Honors and Awards

1. 2018 Micro Test of Time Award, "Efficient Path Profiling," *29th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO 29)*.
1. Eurosys 2016 Test of Time Award, "Language Support for Fast and Reliable Message-based Communication in Singularity OS," *EuroSys 2006.*
2. IEEE Micro Top Picks 2015, "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services," *41st International Symposium on Computer Architecture (ISCA 14).*
3. Best Paper, SIGPLAN Research Highlights 2013, *2013 International Symposium on Code Generation and Optimization (CGO)*, "SIMD Parallelization of Applications that Traverse Irregular Data Structures."
4. Best Paper, *IFIPS Performance 2011*, "Join-Idle-Queue: A Novel Load Balancing Algorithm for Dynamically Scalable Web Services."
5. IEEE Software's 25th-Anniversary Top Picks, "Righting Software."
6. Most Influential Paper, *PLDI 1997*, "Exploiting Hardware Performance Counters with Flow and Context Sensitive Profiling."
7. ACM Fellow, 2006.
8. Best paper, *EuroSys 2006*, "Language Support for Fast and Reliable Message-based Communication in the Singularity OS."
9. Paper selected for *20 Years of PLDI*, 2003, "Improving Data-Flow Analysis with Path Profiling".
10. Most Innovative Paper, *PLDI '99*, "Whole Program Paths".
11. Paper selected for *25 Years of the International Symposia on Computer Architecture (Selected Papers)*, 1998, "Typhoon: A User-Level Shared-Memory System".
12. IBM Partnership Award, 1996.
13. National Science Foundation Young Investigator (NYI), 1993.
14. Best Paper, *ASPLOS V*, "Cooperative Shared Memory: Software and Hardware for Scalable Multiprocessors."
15. California Microelectronics Fellowship, 1985–87.
16. Harvard College Scholar, 1976–80.

## Academic and Industrial Experience

1. Dean, School of Computer and Communications Sciences, EPFL (École Polytechnique Fédérale de Lausanne), Lausanne Switzerland (October 2013 – )
2. Professor, School of Computer and Communications Sciences, EPFL (École Polytechnique Fédérale de Lausanne), Lausanne Switzerland (October 2013 – )
3. Principal Researcher, Microsoft Research, Redmond Washington (February 2012 – September 2013)
4. Director, eXtreme Computing Group (XCG), Microsoft Research (May 2008 – February 2012)
5. Research Area Manager, Microsoft Research, Redmond Washington (December 2005 – May 2008)
6. Assistant Director, Microsoft Research, Redmond Washington (December 2003 – September 2004)
7. Affiliated Associated Professor, Computer Science Department, University of Washington (January 2000 – 2005)
8. Senior Researcher, Microsoft Research, Redmond Washington (May 1998 – December 2005)
9. Visiting Researcher, Microsoft Research, Redmond Washington (August 1997 – July 1998)
10. Associate Professor, Computer Sciences Department, University of Wisconsin-Madison (June 1995 – July 1999)
11. Assistant Professor, Computer Sciences Department, University of Wisconsin-Madison (September 1989 – June 1995)
12. Research Assistant, Computer Science Division, University of California at Berkeley (September 1984 – April 1989)
13. Computer Scientist, Bolt Beranek and Newman, Cambridge, Massachusetts (September 1983 – August 1984)
14. Research Assistant, Computer Science Division, University of California at Berkeley (January 1982 – August 1983)
15. Software Engineer, General Systems Group, Cambridge, Massachusetts (June 1980 – June 1981)

## Professional Experience

1. Advisory Board, Beatdapp, 2020 –
2. Consultant: Franz, Inc., H3, IBM, Mercury Interactive, Inc., and TranSwitch, Inc.
3. Expert Witness: Fliesler, Dubb, Meyer & Lovejoy (Pure Software Inc. v. AIB Software, Inc.), Shneidman, Myers, Dowling, and Blumefield (Ackerman v. State of Wisconsin, DOA).

## Professional Society Membership

Association for Computing Machinery (Fellow)

## Editorial Boards

1. Guest Editor, Special Issue on PPoPP 15, *ACM Transactions on Parallel Computing,* March 2016.
2. Contributed and Review Articles Co-Chair, *Communications of the ACM (CACM*), July 2015 –.
3. Associate Editor, *ACM Transactions on Architecture and Code Optimization (TACO*), May 2015 –.
4. Contributed and Review Articles Editor, *Communications of the ACM (CACM*), November 2007 – July 2015.
5. Associate Editor, *Computer Architecture Letters,* IEEE Computer Society, September *2007 – 2011.*
6. Editorial board, *Software – Practice & Experience,* Wiley & Sons, August 2007 – October 2018.
7. Editorial board, *Open Software Engineering Journal,* Bentham Science Publishers, February 2007 – August 2014.

## Professional Boards

1. Academic Director, International Risk Governance Council Center (IRGC) at EPFL, 2019 –.
2. Executive Committee of Capital Markets and Technology Association, 2018 –.
3. Advisory Board, International Risk Governance Council Center (IRGC) at EPFL, 2018 –.
4. Advisory Board, Zurich Digital Festival, 2016 –.

5. Steering Committee of Swiss Data Science Center (SDSC) at EPFL and ETHZ, 2015 –.
6. Advisory Board, Huawei American Software Lab, 2014 – 2016.
7. Board member, Informatics Europe, 2016 – 2019.
8. Board member, Swiss Informatics Society Special Interest Group SIRA, 2014 –.

## Program Committees

*2.* ►General chair, *Architectural Support for Programming Languages and Operating Systems (ASPLOS 2020)*, Lausanne Switzerland, March 2020.

*3.* External review committee member, *Programming Languages Design and Implementation (PLDI '19)*, Phoenix AZ, June 2019.

*4.* External review committee member, *45th International Symposium on Computer Architecture (ISCA 2018)*, Los Angeles, CA, June 2018.

5. External review committee member, *Symposium on Principles and Practice of Parallel Programming (PPoPP 2014)*, Vienna, Austria, February 2018.
6. External review committee member, *Architectural Support for Programming Languages and Operating Systems (ASPLOS '18)*, Williamsburg, VA, March 2018.
7. Program committee member, *SOSP '15: 25th Symposium on Operating System Principles,* Monterey CA, October 2015.
8. Program committee member, *SNAPL: Inaugural Summit on Advances in Programming Languages,* Asilomar CA, May 2015.
9. ►Program committee chair, *19th Symposium on Principles and Practice of Parallel Programming (PPoPP 2014)*, Orlando Florida, February 2014.
10. Program committee member, *24th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2012)*, October 2012.
11. Program committee member, *High Integrity Language Technology: SIGAda Annual International Conference,* December 2012.
12. External review committee member, *Micro-45,* December 2012.
13. Program committee member, *SPLASH 2012 RACES Workshop on Relaxing Synchronization for Multicore and Manycore Scalability*, October 2012.
14. Program committee member, *USENIX HotPar 2012,* June 2012.
15. Program committee member, *2011 SIGPLAN Workshop on Memory Systems Performance and Correctness (MSPC 2011)*, co-located with PLDI, June 2011.
16. Program committee member, *2nd SIGOPS Asia-Pacific Workshop on Systems (APSys 2011)*, July 2011.
17. Program committee member, *2nd Workshop on Determinism and Correctness in Parallel Programming*, co-located with ASPLOS, March 2011.
18. Program committee member, *USENIX HotPar 2011,* May 2011.
19. Program committee member, *Programming Languages Design and Implementation (PLDI '11)*, June 2011.
20. Program committee member, *Architectural Support for Programming Languages and Operating Systems (ASPLOS '11)*, March 2011.
21. Program committee member, *Workshop on Concurrency for the Application Programmer*, co-located with SPLASH 2010, November 2010.
22. Program committee member, *ACM Symposium on Cloud Computing,* co-located with SIGMOD, June 2010.
23. Program committee member, *GreenMetrics 2010 Workshop*, co-located with SIGMETRICS, June 2010.
24. Program committee member, *6th Workshop on the Interaction between Operating System and Computer Architecture (WIOSCA 2010)*, co-located with ISCA 2010, June 2010.
25. External review committee, *ISCA 2010,* June 2010.

26. Program committee member, *USENIX HotPar 2010,* June 2010.
27. Program committee member, *EuroSys 2010*, April 2010.
28. Program committee member, *International Symposium on Code Generation and Optimization (CGO)*, March 2010.
29. Program committee member, *GreenMetrics 2009 Workshop*, in conjunction with SIGMETRICS/Performance 2009, June 2009.
30. Program committee member, *Fun Ideas and Thoughts (FIT)*, in conjunction with SIGPLAN PLDI, June 2009
31. Program committee member, *First Workshop on Asynchrony in the PGAS Programming Model (APGAS09)*, in conjunction with ICS, June 2009.
32. ► Program Co-Chair and Co-Organizer, *First USENIX Workshop on Hot Topics in Parallelism (HotPar '09)*, March 2009.
33. Program committee member, *ACM Symposium on Parallel Algorithms and Architectures (SPAA 08)*, June 2008.
34. ► Program Committee Chair, *Architectural Support for Programming Languages and Operating Systems (ASPLOS '08)*, 2008.
35. Program committee member, *Programming Language Design and Implementation (PLDI '07)*, June 2007.
36. Program committee member, *Workshop on Architectural and System for Improving Software Dependability, in conjunction with ASPLOS '06*, Oct. 2006.
37. Program committee member, *Workshop on Programming Models for Ubiquitous Parallelism,* in conjunction with PACT, Sept. 2006.
38. Program committee member, *Workshop on Transactional-Memory Workloads*, in conjunction with PLDI, June 2006.
39. Program committee member, *SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP)*, 2006.
40. Program committee member, *Seventh International Conference on Formal Engineering Methods (ICFEM 2005)*, November 2005.
41. Program committee member, *International Conference for Formal Engineering Methods (ICFEM 2004)*, November 2004.
42. Program committee member, *Parallel Architecture and Compilation Techniques (PACT 04)*, September 2004.
43. Program committee member, *Fourth Workshop on Runtime Verification (RV' 04)*, in conjunction with ETAPS, April 2004.
44. Program committee member, *Fifth International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI 04)*, in conjunction with POPL, January 2004.
45. Program committee member, *SIGPLAN Symposium on Principles and Practices of Parallel Programming (PPoPP 03)*, May 2003.
46. Program committee member, *International Symposium on Code Generation and Optimization, CGO-1*, March 2003.
47. Program committee member, *Tenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-X)*, October 2002.
48. Program committee member, *Second Workshop on Runtime Verification*, in conjunction with CAV, July 2002.
49. Program committee member, *International Conference on Software Engineering (ICSE 2003)*, May 2003.
50. Program committee member, *Workshop on Dynamic Program Monitoring and Analysis,* in conjunction with SAS, July 2001.
51. Program committee member, *International Conference on Parallel Architecture and Compilation Techniques (PACT 2001)*, September 2001.
52. Program committee member, *First SIGPLAN Workshop on Optimizations of Middleware and Distributed Systems*, in conjunction with PLDI, June 2001.
53. Program committee member, *Compiler Optimization meets Compiler Verification (COCV 2002)*, in conjunction with ETAPS, April 2002.

54. Program committee member, *SIGPLAN Symposium on Principles and Practices of Parallel Programming (PPoPP 2000)*, June 2000.
55. Program committee member, *2001 Static Analysis Symposium (SAS '01)*, July 2001.
56. Program committee member, *The Best of PLDI Collection, 1970–1996*.
57. Program committee member, *3rd Workshop on Feedback-Directed Optimization*, in conjunction with the 33rd Annual International Symposium on Microarchitecture (MICRO 33), December 2000.
58. Program committee member, *2nd Workshop on Feedback-Directed Optimization*, in conjunction with the 32nd Annual International Symposium on Microarchitecture (MICRO 32), November 1999.
59. Program committee member, *Workshop on Binary Translation*, in conjunction with the 32nd Annual International Symposium on Microarchitecture (MICRO 32), November 1999.
60. ► General Chair, *SIGPLAN Conference on Programming Language Design and Implementation (PLDI 2000)*, June 2000.
61. Program committee member, *SIGPLAN Conference on Programming Language Design and Implementation (PLDI 2000)*, June 2000.
62. Program committee member, *SIGPLAN Principles and Practices of Parallel Programming (PPoPP)*, May 1999.
63. Program committee member, *Fourth International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS'99)*, April 1999.
64. Program committee member, *Second USENIX Conference on Domain-Specific Languages*, October 1999.
65. Program committee member, *SIGPLAN '93 Conference on Programming Languages Design and Implementation (PLDI)*, June 1993.
66. Program committee member, *Twentieth Annual SIGPLAN-SIGACT Symposium on Principles of Programming Languages (POPL)*, January 1993.
67. Program committee member, *ACM Third Symposium on Principles and Practices of Parallel Programming (PPoPP)*, April 1991.
68. Program committee member, *SIGPLAN '91 Conference on Programming Languages Design and Implementation (PLDI)*, June 1991.

## Government Committees

1. Member, DARPA Information Science and Technology (ISAT) study group, August 2013 – 2016.
2. Committee member, *Advancing Software-Intensive Systems Producibility*, Computer Science and Telecommunications Board of the National Academies, 2006 (Final Report: *Critical Code: Software Producibility for Defense*, National Research Council, 2010).
3. Panel participant, *Workshop on Certifiably Dependable Software Systems*, Computer Science and Telecommunications Board of the National Academies, April 2004.
4. Committee member, *Evaluation Committee of the INRIA Program 2A: Software Engineering and Symbolic Computing*, October 2002.
5. Committee member, *Panel on Engineering for Complex System*, National Research Council of the National Academies, 2002.
6. Committee member, *Fundamentals of Computer Science*, Computer Science and Telecommunications Board of the National Academies, 2001. (Final Report: *Computer Science: Reflections on the Field*, National Research Council, 2004.)

## Organizing and Steering Committees

1. ASPLOS Steering Committee, March 2020 - .
2. Co-organizer (with Luis Ceze and Roxana Geambasu), *ISAT/DARPA Workshop on Future of Storage,* New York, New York, May 2016.

3. Co-organizer (with Luis Ceze), *ISAT/DARPA Workshop on Accuracy Trade-Offs Across the System Stack for Performance and Energy*, Orlando, FL, February 2014.
4. Steering committee, *Workshop on Advancing Computer Architecture Research: Popular Parallel Programming*, San Diego, CA, February 2010.
5. Steering committee, *Workshop on Programming Language Curricula*, Cambridge, MA, May 2008.
6. Organizing committee, *Workshop on Future Directions of Compiler Research*, Irvine, CA, February 2006.
7. Steering committee, *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XII)*, October 2006.
8. Co-Organizer, Workshop *on the Evaluation of Software Defect Detection Tools (Bugs 05)*, in conjunction with PLDI, June 2005.
9. Steering committee, *Feedback-Directed and Dynamic Optimization*.
10. Co-Organizer and Program Committee Chair, *Workshop on Compiler Support for System Software (WCSSS'99)*, May 1999.
11. Co-Organizer, *Workshop on Profile and Feedback-Directed Compilation*, October 1998.

## Other Professional Activities

1. Member, ACM Publications Board, 2020.
2. Member, IEEE CS Research Advisory Board, 2018.
3. Chair, Review Committee of the Faculty of Computer Science, Technion, Israel, 2018.
4. Judge, START Hack, St. Gallen, 2018.
5. Member, Most Influential Paper Selection Committee for PLDI 2007, 2017.
6. Member, VMware Systems Research Award Selection Committee, 2016–2018.
7. Member, ACM Fellow Selection Committee, 2016–2022.
8. Member, Cor Baayen Award Selection Committee (CBASC), 2016.
9. Judge, SIX Hackathon, Zurich 2015.
10. Member, DoE review panel, Exascale Operating and Runtime Systems, 2013.
11. Advisory Board, Computer Science and Engineering, University of California, Riverside, April 2012.
12. Member, NSF review panel, Expeditions in Computing, 2011.
13. Member, CRA CIFellows Selection Committee, 2011.
14. Member, CRA CIFellows Selection Committee, 2010.
15. Member, PLDI 2000 Best Paper Selection Committee, 2010.
16. Member, ACM Task Force on Membership, 2009.
17. Member, CRA CIFellows Selection Committee, 2009.
18. Visiting Committee, Harvard School of Engineering and Applied Sciences, April 2009.
19. ACM National Lecturer.
20. Member, NSF review panel, Programming Languages, February 1998.
21. Member, NSF review panel, Career Awards, December 1996.
22. Member, NSF review panel, Postdoctoral Research Associates, January 1995.
23. Member, NSF review panel, Research Initiation Awards, April 1991.

## Grants and Awards

1. 1998 Sun Microsystems: $100,000 cash grant to Wisconsin Wind Tunnel project.

2. 1997 Intel: $20,860 Equipment grant.
3. 1997 Sun Microsystems: $100,000 cash grant to Wisconsin Wind Tunnel project.
4. 1997 Sun Microsystems: $2,450,940 equipment grant to MIDSHIP project.
5. 1997 Hewlett-Packard: $175,337 equipment grant to departmental PC laboratory.
6. 1996 Sun Microsystems: $100,000 cash grant to Wisconsin Wind Tunnel project.
7. 1996 IBM: $79,605 cash and equipment as IBM Partnership Award.
8. 1996 Hewlett-Packard: $56,268 cash and equipment grant.
9. 1996 Microsoft: $100,000 cash grant to CS department.
10. 1996 National Science Foundation: $1,208,251 co-PI, Tornado: Fine-Grain Distributed Shared Memory for SMP Clusters.
11. 1996 National Science Foundation: $1,600,000 co-PD, CISE Research Infrastructure grant, *MIDSHIP: Managing Image Data for Scalable High Performance.*
12. 1995 IBM: $1,255,000 equipment grant to Wisconsin Wind Tunnel Project.
13. 1995 Portland Group: $90,000 software grant.
14. 1995 Hewlett-Packard: $62,338 cash and equipment grant.
15. 1994 Sun Microsystems: $74,780 Equipment grant to Wisconsin Wind Tunnel project.
16. 1994–1996 National Science Foundation: $224,896 co-PI, Cooperative Shared Memory and the Wisconsin Wind Tunnel (Supplement).
17. 1994–1997 DARPA: $2,371,525 co-PI, Blizzard and Paradyn: Infrastructure and Scalable Tools for Multi-Paradigm Parallel Computers.
18. 1993 Digital Equipment Corp.: $73,381 *Editing Program Executables*, NYI matching grant.
19. 1993–1996 DOE: $900,000 co-PI, The Parallel Programmer's Workbench: Programming Tools in Support of the Computational Sciences.
20. 1993–1998 National Science Foundation: $312,500 PI, NSF Young Investigator (NYI) Award. *Programming Massively Parallel Computers.*
21. 1993–1994 National Science Foundation: $39,861 PI, Software Capitalization Grant, *Editing Program Executables.*
22. 1993–1996 National Science Foundation: $1,428,308 co-PI, *Cooperative Shared Memory and the Wisconsin Wind Tunnel.*
23. 1992 Sun Microsystems: $18,095 equipment grant, *Tools for Optimal Profiling and Tracing.*
24. 1992–1993 NASA: $21,620 National Fellowship in Parallel Processing (to L. Huelsbergen), *Dynamic Program Parallelization.*
25. 1991–1993 National Science Foundation: $125,500 PI, *Parallel Symbolic Computation.*
26. 1991–1996 National Science Foundation: $2,000,000 Participating Faculty Member, Departmental Institutional Infrastructure grant, *PRISM-A Laboratory for Research in Future High-Performance Parallel Computing.*

## Books

1. Tim Harris, James Larus, Ravi Rajwar, *Transactional Memory: 2nd edition*, Morgan & Claypool Publishers, 2010.
2. James Larus, Ravi Rajwar, *Transactional Memory*, Morgan & Claypool Publishers, 2007.

## Journal Publications

1. James Larus, Luis Ceze, Karin Strauss, "ASPLOS Report," *IEEE Design & Test*, Vol. 37, No. 3, p. 119–123, June 2020.
2. Sheath DJ, Ruiz de Castañeda R, Bempong NE, Raviglione M, Machalaba C, Pepper MS, Vayena E, Ray N, Wernli D, Escher G, Grey F, Elger BS, Helbing D, Kleineberg KK, Beran D, Miranda JJ, Huffman MD, Hersch F, Andayi F, Thumbi SM, D'Acremont V, Hartley MA, Zinsstag J, Larus J, Rodríguez-Martínez M, Guerin PJ, Merson L, Ngyuen

VK, Rühli F, Geissbuler A, Salathé M, Bolon I, Boehme C, Berkley S, Valleron AJ, Keiser O, Kaiser L, Eckerle I, Utzinger J, Flahault A. Precision global health: a roadmap for augmented action. *Public Health and Emergency,* 2020.

3. James Larus, Chris Hankin, "Regulating Automated Decision Making," *Communications of the ACM (CACM),* Vol. 61, No. 8, pp. 5, August 2018.
4. James Larus, "Technical Perspective: A Simple, Elegant Approach to Non-numeric Parallelization**,"** *Communications of the ACM (CACM),* Vol. 60, No. 12, pp. 87, December 2017.
5. Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demmel, Hadi Esmaeilzadeh, Jeremy Fowers, Gopi PrashanthGopal, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, Joo-Young Kim, Sitaram Lanka, James Larus, Eric Peterson, Simon Pope, Aaron Smith, Jason Thong, Phillip Yi Xiao, Doug Burger, "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services," *Communications of the ACM (CACM,* Vol. 59, No. 11, pp. 10–22, November 2016.
6. James Larus, "The Power of Parallelizing Computations," *Communications of the ACM (CACM),* Vol. 59, No. 10, pp. 84–84, October 2015.
7. Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demmel, Hadi Esmaeilzadeh, Jeremy Fowers, Gopi PrashanthGopal, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, Joo-Young Kim, Sitaram Lanka, James Larus, Eric Peterson, Simon Pope, Aaron Smith, Jason Thong, Phillip Yi Xiao, Doug Burger, "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services," *IEEE Micro,* Vol. 35, No. 3, pp. 10-22, May/June 2015.
8. James Larus, "Programming Multicore Computers: Technical Perspective," *Communications of the ACM (CACM),* Vol. 58, No. 5, pp. 76–76, May 2015.
9. Daniel Reed, Dennis Gannon, James Larus, "Imaging the Future: Thoughts on Computing," *IEEE Computer*, Vol. 45, No. 1, pp. 25–30, January 2012.
10. Yi Lu, Qiaomin Xie, Gabriel Kliot, Alan Geller, James Larus, Albert Greenberg, "Join-Idle-Queue: A Novel Load Balancing Algorithm for Dynamically Scalable Web Services," *Performance Evaluation,* Vol. 68, No. 11, pp. 1056–1071, November 2011.
11. James Larus, Galen Hunt, "The Singularity System," *Communications of the ACM (CACM),* Vol. 53, No. 8, pp. 72–79, August 2010.
12. James Larus, "Spending Moore's Dividend," *Communications of the ACM (CACM)*, Vol. 52, No. 5, pp. 62–69, May 2009.
13. James Larus, "PL Research and Its Consequences on PL Curriculum," *SIGPLAN Notices*, Vol. 43, No. 11, pp. 84–86, November 2008.
14. James Larus, Christos Kozyrakis, "Transactional Memory," *Communications of the ACM (CACM)*, Vol. 51, No. 7, pp. 80–88, July 2008.
15. Galen Hunt, James Larus, "Singularity: Rethinking the Software Stack," *Operating Systems Review,* Vol. 41, No. 2, pp. 37–49, April 2007.
16. James Larus, Galen Hunt, and David Tarditi, "Singularity," *MSDN Magazine*, Vol. 21, No. 7, pp. 176, June 2006.
17. Herb Sutter, James Larus, "Software and the Concurrency Revolution," *ACM Queue,* Vol. 3, No. 7, pp. 54–62, September 2005.
18. James Larus, Thomas Ball, Manuvir Das, Rob DeLine, Manuel Fähndrich, Jon Pincus, Sriram Rajamani, Ramanathan Venkatapathy, "Righting Software," *IEEE Software*, Vol. 21, No. 3, pp. 92–100, May/June 2004.
    ► ***IEEE Software 25th-Anniversary Top Picks.***
19. Trishul Chilimbi, Mark Hill, and James Larus, "Making Pointer-Based Data Structures Cache Conscious," *IEEE Computer*, Vol. 33, Num. 12, pp. 67–74, December 2000.
20. Shubhendu Mukherjee, Steven Reinhardt, Babak Falsafi, Mike Litzkow, Mark Hill, David Wood, Steven Huss-Lederman, and James Larus, "Wisconsin Wind Tunnel II: A Fast, Portable Parallel Architecture Simulator," *IEEE Concurrency*, Vol. 8, No. 4, pp. 12–20, October 2000.
21. Thomas Ball, James Larus, "Using Paths to Measure, Explain, and Enhance Program Behavior," *IEEE Computer*, Vol. 33, No. 7, pp. 57–65, July 2000.

22. Satish Chandra, James Larus, Bradley Richards, "Teapot: A Domain-Specific Language for Writing Cache Coherence Protocols," *IEEE Transactions on Software Engineering*, Vol. 25, No. 3, pp. 317–334, May/June 1999.
23. Mark Hill, James Larus, and David Wood, "Portably Supporting Parallel Programming Languages," *IEEE Computer*, Vol. 28, No. 8, pp. 28–29, August 1995.
24. David Wood, Satish Chandra, Babak Falsafi, Mark Hill, James Larus, Alvin Lebeck, James Lewis, Shubhendu Mukherjee, Subbarao Palacharla, Steven Reinhardt, "Mechanisms for Cooperative Shared Memory," *CMG Transactions*, Issue 84, pp. 51–62, Spring 1994.
25. Thomas Ball and James Larus, "Optimally Profiling and Tracing Programs," *ACM Transactions on Programming Languages and Systems (TOPLAS)*, Vol. 16, No. 4, pp. 1319–1360, July 1994.
26. James Larus and Thomas Ball, "Rewriting Executable Files to Measure Program Behavior," *Software Practice & Experience*, Vol. 24, No. 2, pp. 197–218, February 1994.
27. James Larus, "Compiling for Shared-Memory and Message-Passing Computers," *ACM Letters on Programming Languages and Systems*, Vol. 2, No. 1–4, pp. 165–180, March–December 1993.
28. Mark Hill, James Larus, Steven Reinhardt, and David Wood, "Cooperative Shared Memory: Software and Hardware for Scalable Multiprocessors," *ACM Transactions on Computer Systems (TOCS)*, Vol. 11, No. 4, pp. 300–318, November 1993.
29. James Larus, "Efficient Program Tracing," *IEEE Computer*, Vol. 26, No. 5, pp. 52–61, May 1993.
30. James Larus, "Loop-Level Parallelism in Numeric and Symbolic Programs," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 4, No. 7, pp. 812–826, July 1993.
31. James Larus, "Compiling Lisp Programs for Parallel Execution," *Lisp and Symbolic Computation*, Vol. 4, No. 1, pp. 29–99, January 1991.
32. James Larus, "Abstract Execution: A Technique for Efficiently Tracing Programs," *Software–Practice & Experience*, Vol. 20, No. 12, pp. 1241–1258, December 1990.
33. Mark Hill and James Larus, "Cache Considerations for Programmers of Multiprocessors," *Communications of the ACM*, Vol. 18, No. 8, pp. 97–102, August 1990.
34. Benjamin Zorn, Kinson Ho, James Larus, Luigi Semenzato, and Paul Hilfinger, "Multiprocessing Extensions in SPUR Lisp," *IEEE Software*, pp. 41–49, July 1989.
35. Mark Hill, Susan Eggers, James Larus, et al., "Design Decisions in SPUR," IEEE *Computer*, Vol. 18, No. 11, pp. 8–24, November 1986.

## Prefaces, Collection, Special Issues

1. Carmela Troncoso, Mathias Payer, Jean-Pierre Hubaux, Marcel Salathe, James Larus, Wouter Lueks, Theresa Stadler, Apostolos Pyrgelis, Daniele Antonioli, Ludovic Barman, Sylvain Chatel, Kenneth Paterson, Srdjan Capkun, David Basin, Jan Beutel, Dennis Jackson, Marc Roeschlin, Patrick Leu, Bart Preneel, Nigel Smart, Aysajan Abidin, Seda Gurses, Michael Veale, Cas Cremers, Michael Backes, Nils Ole Tippenhauer, Reuben Binns, Ciro Cattuto, Alain Barrat, Dario Fiore, Manuel Barbosa, Rui Oliveira, and Jose Pereira, "Decentralized Privacy-Preserving Proximity Tracing," IEEE Computer Society Bulletin of the Technical Committee on Data Engineering, Special Issue on Data Technologies Behind Digital Contact Tracing for COVID19, Vol. 43, No. 2, June 2020.
2. Claude Kirchner, James Larus, "Ethics in Research - Introduction," Ercim News, pp. 4, January 2019.
3. James Larus, Dennis Gannon, "Multicore Computing and Scientific Discovery," in Tony Hey, Stewart Tansley, and Kristin Tolle, eds., *The Fourth Paradigm: Data-Intensive Scientific Discovery,* Microsoft Research 2009.
4. James Larus, Preface to Andreas Zeller, *Why Programs Fail: A Guide to Systematic Debugging*, Morgan Kaufmann, 2005.
5. James Larus, Preface to Michael Scott, *Programming Language Pragmatics*, Morgan Kaufmann, 2005.
6. James Larus, Brad Richards, Guhan Viswanathan, "Parallel Programming in C**: A Large-Grain Data-Parallel Programming Language," in Gregory V. Wilson and Paul Lu, eds., *Parallel Programming Using C++*, MIT Press, 1996

7. Steven Reinhardt, Mark Hill, James Larus, Alvin Lebeck, James Lewis, David Wood, "The Wisconsin Wind Tunnel: Virtual Prototyping of Parallel Computers," in Laxmi Bhuyan and Xiaodong Zhang, eds., *Multiprocessor Performance Measurement and Evaluation*, IEEE Computer Society Press, 1994.
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## Patents

1. Burger; Douglas, Larus; James, Putnam; Andrew, Gray; Jan, Parallel decision tree processor architecture, U.S Patent 10,332,008, June 25, 2019.
2. Belady; Christian, Larus; James, Reed; Danny, Borgs; Christian, Chayes; Jennifer, Lobel; Ilan, Menache; Ishai, Nazerzadeh; Hamid, Jain; Navendu, *Data center system that accommodates episodic computation*, U.S Patent 9,886,316, February 6, 2018.
3. He; Yuxiong, Elnikety; Sameh, Larus; James, Yan; Chenyu, *Scheduling execution requests to allow partial results*, U.S Patent 9,817,698, November 14, 2017.
4. Meijer; Henricus, Gates, III; William, Flake; Gary, Bergstraesser; Thomas, Blinn; Arnold, Brumme; Christopher, Cheng; Lili, Connolly; Michael, Glasser; Daniel, Gounares; Alexander, Larus; James, MacLaurin; Matthew, Mishra;, Mital; Amit, Snyder, Jr.; Ira, Zaner-Godsey; Melora, *Transformations for virtual guest representation*, U.S Patent 9,746,912, August 29, 2017.

5. Steven Maillet, Michael Hall, James Larus, Jeremiah C. Spradlin, *Memory manager with enhanced application metadata*, U.S. Patent 9,558,040, January 31, 2017.
6. Jan Graym Timothy L Harris, James Larus, Burton Smith, *Cache metadata for accelerating software transactional memory*, U.S. Patent 8,898,652, November 25, 2014.
7. Hunt; Galen, Larus; James, Gounares; Alexander, Endres; Raymond, *Secure and stable hosting of third-party extensions to web services*, U.S. Patent 8,849,968, September 30, 2014.
8. Christian Belady, James Larus, Danny Reed, Christian Borgs, Jennifer Chayes, Ilan Lobel, Ishai Menache, Hamid Nazerzadeh, Navendu Jain, *Data center system that accommodates episodic computation*, U.S. Patent 8,849,469, September 2014.
9. Gray; Jan, Harris; Timothy, Larus; James, Smith; Burton, *Cache metadata for implementing bounded transactional memory*, U.S. Patent 8,849,469, August 19, 2014.
10. Larus; James, Harris; Timothy, Marathe; Virendra, *Lightweight transactional memory for data parallel programming*, U.S. Patent 8,806,495, August 14, 2014.
11. Meijer; Henricus, Flake; Gary, Blinn; Arnold, Bolosky; William, Cheng; Lili, Connolly; Michael, Gounares; Alexander, Larus; James, MacLaurin; Matthew, Mishra; Debi, Mital; Amit, Snyder, Jr.; Ira, Treadwell, III; David, *Determination of optimized location for services and data*, U.S. Patent 8,719,143, May 6, 2014.
12. Meijer; Henricus Johannes Maria, Gates, III; William H., Ozzie; Raymond E., Flake; Gary W., Bergstraesser; Thomas F., Blinn; Arnold N., Brumme; Christopher W., Cheng; Lili, Dani; Nishant V., Glasser; Daniel S., Gounares; Alexander G., Hunt; Galen C., Larus; James R., MacLaurin; Matthew B., Mishra; Debi P., Mital; Amit, Snyder, Jr.; Ira L., Thekkath; Chandramohan A., *Remote Provisioning of Information Technology*, U.S. Patent 8,402,110, March 2013.
13. Gray; Jan, Harris; Timothy, Larus; James, Smith; Burton, *Cache Metadata Identifiers for Isolation and Sharing*, U.S. Patent 8,225,297, July 2012.
14. Jain; Navendu, Williams; Charles, Larus; James, Reed; Dan, *Energy-aware Server Management*, U.S. Patent 8,225,119, July 2012.
15. Burger; Doug, Larus; James, Strauss; Karin, Condit; Jeremy, *Managing Memory Faults*, U.S. Patent 8,201,024, June 2012.
16. Hunt; Galen C, Larus; James R., Fahndrich; Manuel A, Hodson; Orion, Tarditi; David R., Spear; Michael, Carbin; Michael, Levi; Steven P., Steensgaard; Bjame, *Configuration of isolated extensions and device drivers*, U.S. Patent 8,074,231, December 2011.
17. Hunt; Galen C, Larus; James R., Fahndrich; Manuel, Steensgaard; Bjarne, Tarditi; David R., Zill; Brian, *Kernel Interface with Categorized Kernel Objects*, U.S. Patent 8,032,898, October 2011.
18. Hunt; Galen C., Larus; James R., DeTreville; John D., Wobber; Edward P., Abadi; Martin, Jones; Michael B., Chilimbi; Trishul, *Operating-system Process Construction*, U.S. Patent 8,020,141, September 2011.
19. Gates, III; William H., Flake; Gary W., Bolosky; William J., Dani; Nishant V., Glasser; Daniel S., Gounares; Alexander G., Larus; James R., MacLaurin; Matthew B., Meijer; Henricus Johannes Maria, *Hardware Architecture for Cloud Services*, U.S. Patent 8,014,308, September 2011.
20. Gates, III; William H., Flake; Gary W., Gounares; Alexander G., Bergstraesser; Thomas F., Blinn; Arnold N., Brumme; Christopher W., Cheng; Lili, Connolly; Michael, Glasser; Daniel S., Larus; James R., MacLaurin; Matthew B., Meijer; Henricus Johannes Maria, Mishra; Debi P., Mital; Amit, Snyder, Jr.; Ira L., Zaner-Godsey; Melora, *Virtual Entertainment*, U.S. Patent 8,012,023, September 2011.
21. Jan Gray, Timothy L. Harris, James Larus, Burton Smith, *Software Accessible Cache Metadata*, U.S. Patent 8,001,538, August 2011.
22. Ozzie; Raymond, Gates, III; William, Flake; Gary, Bergstraesser; Thomas, Blinn; Arnold, Brumme; Christopher, Cheng; Lili, Connolly; Michael, Dani; Nishant, Glasgow; Dane, Glasser; Daniel, Gounares; Alexander, Larus; James, MacLaurin; Matthew, Meijer; Henricus, Mishra; Debi, Mital; Amit, Snyder, Jr.; Ira, Thekkath; A, Treadwell, III; David, Zaner-Godsey; Melora, *Personal Data Mining*, U.S. Patent 7,930,197, April 2011.
23. Hunt; Galen C, Hawblitzel; Chris K., Larus; James R., Fahndrich; Manuel A, Aiken; Mark, *Process isolation using protection domains*, U.S. Patent 7,882,317, February 2011.

24. Meijer; Henricus Johannes Maria, Bergstraesser; Thomas F., Brumme; Christopher W, Cheng; Lili, Gounares; Alexander G., Larus; James R., Mishra; Debi P., Snyder, Jr.; Ira L., *Resource Standardization in an Off-premise Environment*, U.S. Patent 7,797,453, September 2010.

25. Hunt; Galen, Larus; James, DeTreville; John, Wobber; Edward, Abadi; Martin, Jones; Michael, Chilimbi; Trishul, Operating system process identification, Patent 7,788,637, August 2010.

26. Meijer; Henricus Johannes Maria, Gates, III; William H., Ozzie; Raymond E., Flake; Gary W., Cheng; Lili, Dani; Nishant V., Glasser; Daniel S., Gounares; Alexander G., Larus; James R., Mishra; Debi P., Mital; Amit, Snyder, Jr.; Ira L., Thekkath; Chandramohan A., *State Reflection*, U.S. Patent 7,716,280, May 2010.

27. Cheng; Lili, Flake; Gary W., Gounares; Alexander G., Larus; James R., MacLaurin; Matthew B., Ozzie; Raymond E., Bergstraesser; Thomas F., Blinn; Arnold N., Brumme; Christopher W., Connolly; Michael, Glasser; Daniel S., Meijer; Henricus Johannes Maria, Mishra; Debi P., Zaner-Godsey; Melora, *Machine Learning System for Analyzing and Establishing Tagging Trends Based on Convergence Criteria*, U.S. Patent 7,716,150, May 2010.

28. Rehof; Jakob, Larus; James R., Rajamani; Sriram K., *Programming Model to Detect Deadlocks in Concurrent Programs*, U.S. Patent 7,703,077, April 2010.

29. Hunt; Galen C., Larus; James R., DeTreville; John D., Jones; Michael B., Chilimbi; Trishul A., *Inter-process Interference Elimination*, U.S. Patent 7,694,300, April 2010.

30. Larus; James R., Rajamani; Sriram K., Rehof; Jakob, *Contracts and Futures in an Asynchronous Programming Language*, U.S. Patent 7,694,276, April 2010.

31. Ozzie; Raymond E., Gates, III; William H., Flake; Gary W., Bergstraesser; Thomas F., Blinn; Arnold N., Bolosky; William J., Brumme; Christopher W., Cheng; Lili, Connolly; Michael, Glasgow; Dane A., Glasser; Daniel S., Gounares; Alexander G., Larus; James R., MacLaurin; Matthew B., Meijer; Henricus Johannes Maria, Mishra; Debi P., Mital; Amit, Snyder, Jr.; Ira L., Thekkath; Chandramohan A., Zaner-Godsey; Melora, *Dynamic Environment Evaluation and Service Adjustment Based on Multiple User Profiles Including Data Classification and Information Sharing with Authorized Other Users*, U.S. Patent 7,689,524, March 2010.

32. Gates, III; William H., Flake; Gary W., Larus; James R., Mishra; Debi P., Thekkath; Chandramohan A., Ozzie; Raymond E., Cheng; Lili, Dani; Nishant V., Glasser; Daniel S., Gounares; Alexander G., Meijer; Henricus Johannes Maria, Mital; Amit, Snyder, Jr.; Ira L., State Replication, U.S. Patent 7,680,908, March 2010.

33. Henricus Johannes Maria Meijer, William H. Gates, III, Raymond E. Ozzie, Gary W. Flake, Thomas F. Bergstraesser, Arnold N. Blinn, Christopher W. Brumme, Lili Cheng, Michael Connolly, Nishant V. Dani, Dane A. Glasgow, Daniel S. Glasser, Alexander G. Gounares, James R. Larus, Matthew B. MacLaurin, Debi P. Mishra, Amit Mital, Ira L. Snyder, Jr., Chandramohan A. Thekkath, David R. Treadwell, III, and Melora Zaner-Godsey, *Recommendation System that Identifies a Valuable User Action by Mining Data Supplied by a Plurality of Users to Find a Correlation that Suggests One or More Actions for Notification*, U.S. Patent 7,657,493, February 2010.

34. Henricus Johannes Maria Meijer, Raymond E. Ozzie, Gary W. Flake, Thomas F. Bergstraesser, Arnold N. Blinn, Christopher W. Brumme, Michael Connolly, Dane A. Glasgow, Alexander G. Gounares, Galen C. Hunt, James R. Larus, Matthew B. MacLaurin, and David R. Treadwell, III, *Operating system with Corrective Action Service and Isolation*, U.S. Patent 7,647,522, January 2010.

35. Galen C. Hunt, James R. Larus, Manuel Fahndrich, Edward P. Wobber, Martin Abadi, and John D. DeTreville, *Inter-process Communications Employing Bi-directional Message Conduits*, U.S. Patent 7,600,232, January 2010.

36. Galen C. Hunt, Thomas Roeder, James R. Larus, Manuel Fahndrich, John D. DeTreville, Steven P. Levi, Benjamin Zorn, Wolfgang Grieskamp, *Self-Describing Artifacts and Application Abstractions*, U.S. Patent 7,451,435, November 2008.

37. James Larus, *Virtual Machine for Operating N-core Application on M-core Processor*, U.S. Patent 7,406,407, July 2008.

38. Michael Parkes, James Larus, *Method and System for Performing a Task on a Computer*, U.S. Patent 7,137,116, November 2006.

39. James Larus, Robert Davidson, Trishul Chilimbi, *Field Reordering to Optimize Cache Utilization*, United States Patent 6,360,361, March 2002.

40. Trishul Chilimbi, James Larus, Robert Davidson, *Data Structure Partitioning to Optimize Cache Utilization*, United States Patent 6,330,556, December 2001.

41. James Larus, *Whole Program Path Profiling*, United States Patent 6,327,699, December 2001.

42. Trishul Chilimbi, James Larus, *Data Structure Partitioning with Garbage Collection to Optimize Cache Utilization*, United States Patent 6,321,240, November 2001.

## Widely Distributed Software

PP – A path profiling tool.

EEL – An executable editing library.

QP/QPT – A program profiler and tracing system that uses the Ball & Larus's optimal profiling algorithm.

SPIM – An instruction-level simulator for the MIPS R2000.

AE – A compiler-based program tracing system.

mh-e – A mail system front-end for GNU emacs.

## Keynote Talks

1. "Protein Clustering: Parallelizing an Expensive, Irregular Computation," *Workshop on Accelerator Architecture in Computational Biology and Bioinformatics (AACBB 2020),* San Diego, CA, March 2020.
2. "Is AI Different?" *An Insightful Farewell to the Dean's Team,* TU Wein, Vienna, Austria, December 2019.
3. "Caches Are Not Your Friend: Programming Non-Volatile Memory," *SYSTOR 2019 Conference,* Haifa Israel, June 2019.
4. "It's the End of the World as We Know It," *HiPEAC 2015 Conference, 2015,* Amsterdam, Netherlands, January 2015.
5. —, Compiler *Architecture and Tools Conference, 2014,* Haifa, Israel, December 2014.
6. "Look Up! Your Future is in the Cloud," *34th ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI '13)*, Seattle, WA, June 2013.
7. "It's the End of the World as We Know It (And I Feel Fine)," *Middleware 2012,* Montreal, Canada, December 2012.
8. —, *Runtime Verification 2012 (RV 12),* Istanbul, Turkey, September 2012.
9. —, *Swedish Multicore Day*, Stockholm, Sweden, September 2012.
10. "The Cloud Will Change Everything," *EcoCloud Opening*, EPFL, Lausanne, Switzerland, May 2011.
11. —, *Sixteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2011)*, March 2011.
12. "Programming the Cloud," *11th International Symposium on High-Performance Computer Architecture (HPCA) and 16th SIGPLAN Annual Symposium on Principles and Practice of Parallel Programming (PPoPP)*, February 2011.
13. "Programming Clouds," *International Conference on Compiler Construction (CC '10),* Paphos, Cyprus, March 2010.
14. "Multicore and Cloud Computing – Time to Start Afresh," *High Confidence Software and Systems*, Baltimore, MD, May 2009.
15. "The Real Value of Testing," *International Symposium on Software Testing and Analysis (ISSTA 2008),* Seattle, WA, July 2008.
16. "Is Architecture the Solution?," *First Workshop on Architectural and System Support for Improving Software Dependability (ASID)*, at International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XII), San Jose, CA, October 2006.
17. "Abolish Run-time Systems: The Operating System Should Control the Execution Environment," *Second International Conference on Virtual Execution Environments*, Ottawa, Canada, June 2006.
18. "Building Dependable Software," *I & C Research Day*, EPFL (Ecole Polytechnique Fédérale de Lausanne), June 2005.
19. —, *Eleventh International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-XI)*, Boston MA, October 2004.
20. "Righting Software: Tools to Improve Software Development," *Third Annual Southeastern Software Engineering Conference*, Huntsville AL, March 2004.

21. "Why Write Real Software (in a University)?," *3rd Annual Workshop on Computer Architecture Education (WCAE3)*, San Antonio, Texas, February 1997.

## Invited Talks

1. "Regulating Artificial Intelligence? Reflecting on Several International Recommendations," *Vienna Workshop on Digital Humanism*, Vienna Austria, April 2019.
2. "Programming NVM," *SPLASH-I at SPLASH 2018*, Boston MA, November 2018.
3. "Computational Thinking is for Everyone," *Informatics Europe Pre-Summit Workshop for Deans and Department Heads*, Lisbon, October 2017.
4. "Tom Was Right: Integration is Hard," *Tom (Reps) at 60*, at SAS 2016, Edinburgh, September 2016.
5. "Catapult the Masses," *Workshop on Reconfigurable Computing for the Masses, Really?* FPL'15, London, September 2015.
6. "What Happened to the Promise of Software Tools?," *Software Correctness and Reliability Workshop*, ETH Zurich, October 2014.
7. "Tune, Rewrite, Reinvent," *Microsoft Research Faculty Summit Workshop: Approaching the End of Moore's Law: Time to Reinvent the System Stack?* Microsoft Research, July 2014.
8. "Tech Transfer of Software Tools," High Confidence Software and Systems Conference (HCSS), May 2012.
9. "It's the End of the World as We Know It (And I Feel Fine)," *DARPA/ISAT Workshop: Advancing Computer Systems without Technology Progress*, March 2012.
10. "Orleans: Cloud Programming for Everyone," *Barcelona Multicore Workshop*, November 2011.
11. "The Cloud Will Change Everything," *Microsoft Research Cloud Futures Workshop*, June 2011.
12. —, AMD, April 2011.
13. "Cloud Programming," *Microsoft Faculty Summit*, July 2010.
14. —, *16th Monterey Workshop on Modeling, Development and Verification of Adaptive Computer Systems*, April 2010.
15. "Should We Fear Concurrency?," *Workshop on Advancing Computer Architecture Research (ACAR)*, February 2010.
16. "Programming Clouds," *First Mysore-Park Workshop on Building and Programming the Cloud*, Mysore India, January 2010.
17. "Hardware Can Make Data Center Software Simpler and More Robust," *Workshop on Architectural Concerns in Large Datacenters*, ISCA 2009, Austin, TX, June 2009.
18. "Singularity: Designing Better Software," *International Conference on Computer-Aided Verification (CAV 08)*, Princeton NJ, July 2008.
19. "Spending Moore's Dividend," *Workshop on Exploiting Concurrency: Efficiency and Correctness (EC^2)*, at CAV 2008, Princeton NJ, July 2008.
20. "It is the Software, Stupid," *Presentation to the Computer Science Technical Board panel on Sustaining Growth in Computing Performance*, San Jose, CA, December 2007.
21. "Challenges in Compiler Technology for Software Reliability and Productivity," *Workshop on Future Directions for Compiler Research and Education*, February 2007.
22. "Can Architecture Enhance Verifiability? The Singularity Project at Microsoft Research," *Seventh International Conference on Verification, Model Checking and Abstract Interpretation*, Charleston, SC, January 2006.
23. "Building Dependable Software," *Microsoft Academic Days,* Silicon Valley, San Jose, CA, October 2004.
24. "Software Matters," *Presentation to the Computer Science Technical Board panel on Certifiably Dependable Software*, Washington DC, October 2004.
25. "Righting Software: Tools to Improve Software Development," *German-American Frontiers of Engineering Symposium*, National Academy of Engineering, April 2004.

26. "Righting Software: Tools to Improve Software Development," *Microsoft Faculty Summit & Microsoft European Faculty Summit*, July 2003.
27. "Programs Follow Paths," *IEEE International Conference on Computer Languages (ICCL '98)*, May 1998.
28. "Introduction to Java," *WILS World '97 Conference*, Madison WI, May 1997.
29. "A Case for Custom Coherence Protocols," *IBM Research 50th Anniversary Symposium on Parallel Computing*, IBM Tokyo Research Laboratory, Tokyo Japan, March 1996.
30. "Tempest: A Substrate for Portable Parallel Programs," Plenary talk, *Seventeenth International Conference on Boundary Elements (BEM 17)*, Madison WI, July 1995.
31. "LCM: Memory System Support for Parallel Language Implementation," *Parallel Object Oriented Methods & Applications (POOMA)*, Santa Fe, New Mexico, December 1994.
32. "Compiling for Shared-Memory and Message-Passing Computers," *DIMACS Workshop on Models, Architectures, and Technologies for Parallel Computation*, Rutgers University, September 1993.
33. "CICO: A Practical Shared-Memory Programming Performance Model," *Workshop on Portability and Performance for Parallel Processing*, Southampton, England, July 1993.
34. "Compilers: Catching Up With Computer Architecture," *IBM Rochester*, June 1993.
35. "C**: A Large-Grain, Object-Oriented, Data-Parallel Programming Language," *Fifth Workshop on Languages and Compilers for Parallel Computers*, New Haven CT, August 1992.
36. "Parallelism in Numeric and Symbolic Programs," *Workshop on Compilers for Parallel Machines*, Paris, France, December 1990.
37. —, *Third Workshop on Languages and Compilers for Parallel Computers*, Irvine, CA, August 1990.
38. —, *Workshop on Parallelization in the Presence of Pointers*, Leesburg, VA, March 1990.
39. "Parallel Lisp for SPUR," *Asilomar Microcomputer Workshop*, Asilomar, CA, 1985.

## Informal Presentations at Symposia, Workshops, and Tutorials

1. "Why AI?," Meeting on Precision Global Health, Rockefeller Foundation Bellagio Italy, November 2017.
2. Panelist, "It's time: academic systems venues should require authors to make their code and data publicly available; those that do not will be held to a higher standard," *ASPLOS 2015*, Istanbul Turkey, March 2015.
3. Panelist, "Discussion on industry vs. government funding for data center research," *Workshop on Exascale Evaluation and Research Techniques (EXERT)*, at ASPLOS 2011, Santa Anna, CA March 2011.
4. Debater, "There is a free lunch: you can have strong parallel safety guarantees with little programmer effort," *Workshop on Deterministic Multiprocessing and Parallel Programming*, University of Washington, November 2009.
5. Panelist, "Teach Parallel Panel," *Supercomputing '09,* Portland, OR, November 2009.
6. Panelist, "Cloud Computing Challenges and Realities," *5th Workshop on the Interaction between Operating System and Computer Architecture (WIOSCA 09)*, at ISCA 2009, Austin, TX, June 2009.
7. Panelist, "Memory Systems Panel," *Workshop on Memory Systems Performance and Correctness*, ASPLOS '08, Seattle, WA, March 2008.
8. "Reconsidering Transactional Memory," *Dagstuhl Seminar*, September 2007.
9. Panelist, "Corezilla: Build and Tame the Multicore Beast," *44th Design Automation Conference (DAC),* June 2007.
10. "What do Bell Bottoms, Peace Signs, and Computer Architecture Have in Common?," Wild and Crazy Idea Session, at *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XII),*San Jose, CA, October 2006.
11. "Software Challenges in Nanoscale Technologies," *CRA Workshop on Grand Challenges in Architecture*, December 2005.
12. "It's the Software, Stupid," *Workshop on Transactional Memory*, April 2005.
13. "The End of Compiler Research," *Dagstuhl Vision Seminar*, August 2003.

14. "Cache-Conscious Compilation: Can Compilers Hack It?," *Dagstuhl Seminar*, September 2000.
15. Tutorial: "Parallel Programming Languages," *SIGPLAN '93 Conference on Programming Language Design and Implementation (PLDI)*, June 1993.
16. Panelist: "SPUR Retrospective," *ONR/NSF/DARPA Workshop on Research in Experimental Computer Science*, October 1991.
17. Tutorial: "Parallel Lisp," *SIGPLAN '91 Conference on Programming Language Design and Implementation (PLDI)*, June 1991.
18. Panelist: "Problems and Issues in Parallel C Programming," *SIGPLAN Principles and Practice of Parallel Programming (PPoPP)*, April 1991.

## Distinguished Lectures

1. "Programming NVM," IST/INESC-ID Distinguished Lecture, IST, Lisbon Portugal, October 2019.
2. "Programming NVM," Informatics Colloquium, Sorbonne University, Paris France, October 2018.
3. "It's the End of the World as We Know It (And I Feel Fine)," University of Chicago, October 2015.
4. "Look Up! Your Future is in the Cloud," Distinguished Lecture, Cray Distinguished Speaker Series, University of Minnesota, Minneapolis, MN, February 2014.
5. "Programming the Cloud," *Gerard Salton Memorial Lecture*, Cornell University, November 2010.
6. "Spending Moore's Dividend," Distinguished Lecture, University of California at Davis, May 2009.
7. —, Distinguished Lecture, Texas A&M University, February 2009.
8. "The Real Value of Testing," Distinguished Lecture, Information Trust Institute, University of Illinois at Urbana Champagne, January 2009.
9. "Singularity: Rethinking the Software Stack," Distinguished Lecture, University of Pennsylvania, November 2006.
10. "Singularity Overview," Distinguished Lecture, University of Illinois at Urbana Champagne, January 2006.
11. —, Distinguished Colloquium, University of California at Berkeley, November 2005.
12. "Building Dependable Software," Distinguished Lecture, Rice University, October 2004.
13. "Righting Software: Tools to Improve Software Development," Distinguished Colloquium, University of Maryland, November 2003.
14. "A New Generation of Systematic Programming Tools," Distinguished Lecturer, University of Pittsburgh, October 2002.
15. —, Distinguished Lecture, University of California, Berkeley, March 2002.

## Lectures at Universities and Research Institute

1. "It's the End of the World as We Know It (And I Feel Fine)," IBM Research Zurich, September 2015.
2. "What Happened to the Promise of Software Tools?", UC Berkeley, November 2014.
3. "Technology Trends and Research Opportunities," ETH Zurich, May 2014.
4. "Orleans: Cloud Programming for Everyone," IBM Research, March 2013.
5. "It's the End of the World as We Know It (And I Feel Fine)," EPFL, Lausanne, Switzerland, September 2012.
6. "The Cloud Will Change Everything," University of California, Riverside, April 2012.
7. "Orleans: Cloud Computing for the Masses," Bell Laboratories, September 2011.
8. —, Harvard University, September 2011.
9. "Orleans: A Platform for Cloud Computing," Harvard University, November 2009.
10. "Spending Moore's Dividend," University of Texas, Austin, February 2009.
11. —, Carnegie-Mellon, April 2008.

12. “Singularity: Rethinking the Software Stack,” University of Chicago, January 2008.
13. —, University of Texas at Austin, November 2007.
14. —, Rice University, March 2007.
15. “Singularity Overview,” University of Wisconsin Computer Architecture Colloquia, November 2005.
16. “Righting Software: Tools to Improve Software Development,” Ecole Nationale Supérieure d´Electronique et de Radioélectricité de Bordeaux, July 2003.
17. “A New Generation of Systematic Programming Tools,” Universitat Politècnica de Catalunya, Barcelona Spain, October 2002.
18. —, University of Wisconsin—Madison, May 2002.
19. “Using Cohort Scheduling to Enhance Server Performance,” Compaq Systems Research Center, June 2001.
20. —, University of Washington, April 2001.
21. “Enhanced Server Performance with Staged Server,” University of California, Berkeley, October 2000.
22. —, University of Wisconsin, Madison, October 2000.
23. “Whole Program Paths,” University of Maryland, October 1999.
24. —, CMU, March 1999.
25. “Fast Out-of-Order Processor Simulation,” University of Washington, April 1998.
26. “Cache-Conscious Data Structures,” University of Washington, January 1998.
27. “Efficient Path Profiling,” Silicon Graphics, May 1997.
28. —, University of California, Berkeley, May 1997.
29. —, Sun Microsystems, April 1997.
30. —, University of California, San Diego, April 1997.
31. —, University of Toronto and IBM Toronto, March 1997.
32. —, Microsoft Research Laboratory, February 1997.
33. —, Hewlett Packard Research Laboratory, August 1996.
34. “EEL: Machine-Independent Executable Editing,” Intel Corporation, September 1996.
35. —, Princeton University, April 1996.
36. —, Sun Microsystems, December 1995.
37. —, Microsoft Research, June 1995.
38. “Tempest: A Substrate for Portable Parallel Programs,” University of Wisconsin-Milwaukee, November 1995.
39. —, University of Washington, June 1995.
40. —, University of Massachusetts, April 1995.
41. —, Harvard University, April 1995.
42. “Tempest: User-Level Shared Memory,” Rice University, March 1994.
43. —, University of Texas, March 1994.
44. —, University of Maryland, March 1994.
45. “EEL: A Library for Editing Program Executables,” AT&T Bell Laboratories, Naperville, December 1993.
46. “Cooperative Shared Memory and the Wisconsin Wind Tunnel,” IBM Hawthorne Research Laboratory, July 1993.
47. —, Los Alamos National Laboratory, June 1993.
48. —, University of California, Santa Barbara, February 1993.
49. —, Duke University, January 1993.

50. —, Washington University, December 1992.
51. —, Princeton University, December 1992.
52. —, Carnegie-Mellon University, November 1992.
53. —, University of Colorado, September 1992.
54. —, University of Washington, September 1992.
55. "Optimally Profiling and Tracing Programs," Rutgers University, August 1992.
56. —, University of Texas at Austin, January 1992.
57. —, Yale University, October 1991.
58. —, Stanford University, August 1991.
59. "Parallelism in Numeric and Symbolic Programs," University of California at Berkeley, August 1991.
60. —, AT&T Bell Laboratories, Murray Hill, August 1991.
61. —, Hewlett-Packard Laboratories, April 1991.
62. —, Center for Supercomputing Research and Development, University of Illinois, November 1990.
63. —, MIT, June 1990.
64. —, IBM Hawthorne Research Laboratory, June 1990.
65. "Restructuring Symbolic Programs for Concurrent Execution on Multiprocessors," University of California at Berkeley, February 1989.
66. —, IBM Hawthorne Research Laboratory, July 1988.
67. "Restructuring Symbolic Programs for Concurrent Execution on Multiprocessors," (Interview talk) Stanford University, February 1989.
68. —, University of Washington, March 1989.
69. —, Princeton University, March 1989.
70. —, University of Maryland, March 1989.
71. —, MIT, March 1989.
72. —, Yale University, March 1989.
73. —, CMU, March 1989.
74. —, University of Wisconsin-Madison, April 1989.

## Videos

1. Orleans: A Framework for Scalable Client+Cloud Computing, Channel 9 video, December 2010.
2. Singularity III: Revenge of the SIP, Channel 9 video, August 2006.
3. Singularity Revisited, Channel 9 video, December 2005.
4. Singularity: A Research OS Written in C#, Channel 9 video, May 2005.

## Teaching Experience

2013–, Full Professor: EPFL.

2000, Visiting Associate Professor: University of Washington.

1995–1998, Associate Professor: University of Wisconsin-Madison.

1989–1995, Assistant Professor: University of Wisconsin-Madison.

1985–1986, Instructor: Franz Inc., Berkeley, California.

1981, Teaching Assistant: University of California at Berkeley.

1980–1981, Head Teaching Assistant: Harvard University.

1979–1980, Teaching Assistant: Harvard University.

## PhD Students

1. Stuart Byma, PhD EPF "Parallel and Scalable Bioinformatics,", May 2020.
2. Glenn Ammons, PhD Univ. Wisconsin, "Strauss: A Specification Miner," April 2003 (supervised by Ras Bodik).
3. Eric Schnarr, PhD Univ. Wisconsin, "Applying Programming Language Implementation Techniques To Processor Simulation," December 2000 (supervised by Prof. Mark Hill).
4. Trishul Chilimbi, PhD Univ. Wisconsin, "Cache-Conscious Data Structures," June 1999.
5. Satish Chandra, PhD Univ. Wisconsin, "Software Techniques for Customizable Distributed Shared Memory," October 1997 (winner: 1998 UW Computer Sciences Graduate Student Research Award)
6. Guhan Viswanathan, PhD Univ. Wisconsin, "New Techniques for Compiling Data Parallel Languages," September 1996.
7. Brad Richards, PhD Univ. Wisconsin, "Memory Systems for Parallel Programming," August 1996.
8. Lorenz Huelsbergen, PhD Univ. Wisconsin, "Dynamic Language Parallelization," August 1993.

## Master Students

1. Charles Parzy-Turlat, "Sampling-based Profiling for GraalVM Native Image," September 2020.
2. Thierry Treyer, "Scaling Memoro for Industry Workloads," July 2020.
3. Natalija Gucevska, "Historical data error detection and classification," April 2019.
4. Ismail Imani, "ESSOP Administration Tool," August 2018.
5. Enea Bell, "SITAONAIR Data Integration Platform: Microservices, Configuration Management, Build and Deployment Pipeline," April 2018.
6. Alexandros Sympetheros, "Collecting insights from a large codebase to ensure high software quality," September 2017.
7. Marc Schär, "SITAONAIR Test Agents," August 2016.
8. Laurent Weingart, "Mobile Identity," April 2016.
9. Kevin Gilliéron, "Unification of Computer Security Web Services," April 2016.
10. Liansheng Hua, "Compile-Time Obfuscation for Code Renewability," August 2015.

## Civic Service

Lakeside School Parent Technology Advisory Committee, 2003 – 2010.

Search committee, Islander Middle School Principal, Mercer Island School District, April 2001.