TCL Student Projects Spring 2026

VLSI / Digital Design Related Projects

Your ideas

If you have your own ideas for a project, please contact us:

TCL-projects main page

These two pages summarize the types of work carried out by PhD students in our lab:

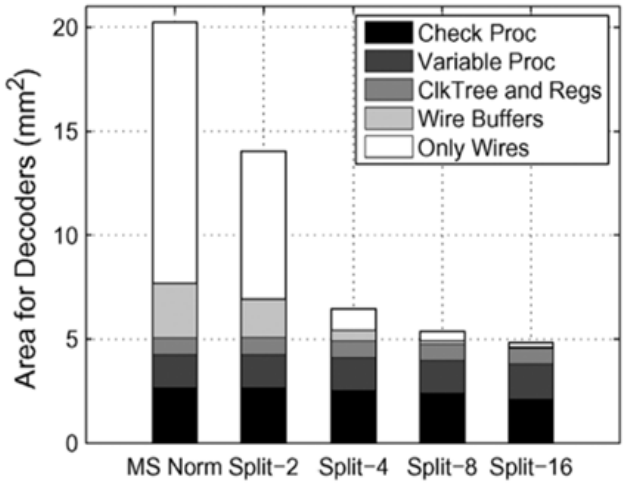
Integrated Circuit and FPGA

Wireless communication and sensing

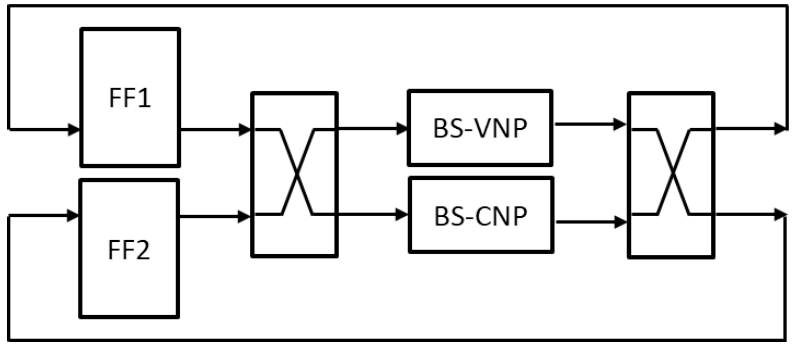
The following slides present the ideas and project proposals we currently have.

Routing-Congestion Analysis for Efficient Belief Propagation (BP) Decoders

- **Motivation**
  - Even for fixed-code decoders, the wiring network dominates area, timing closure difficulty, and power consumption, while the actual compute logic occupies **only a small portion of the die**.
  - Emerging compute-in-memory(CIM) based bit-serial BP architectures as well as advanced technology node further reduce the logic area, which **shifts the bottleneck almost entirely to interconnect**.



- **Objective**
  - Compare routing behavior between different architectures to identify bottlenecks and scaling limits.
  - Evaluate how wire congestion affects area, power, and delay, and derive guidelines for scalable interconnect-aware BP decoder.



- **Type of work:**
  - RTL development (VHDL/Verilog)
  - Semi-custom placement and routing

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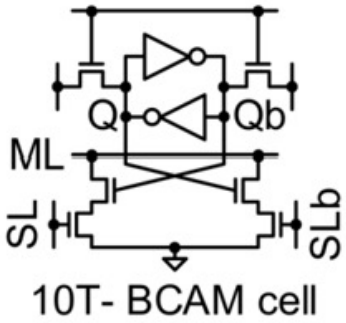
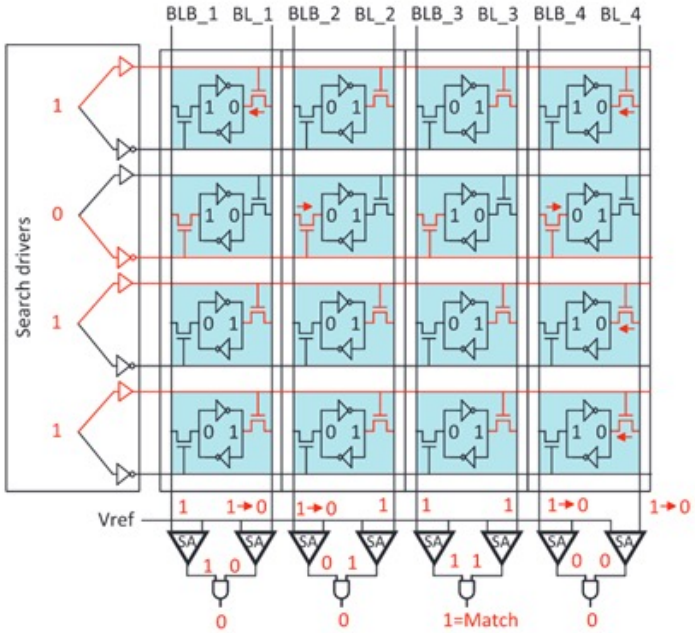
An Energy-Efficient and Compact Content-Addressable Memory (CAM)

- **Motivation**
  - Conventional SRAM-based CAM implementations typically require **10T** bitcell to support reliable match operations.
  - While compact CAM bitcells (**<6T**) significantly reduce area, they suffer from **large static power** due to direct conduction paths between "stored-0" and "stored-1" conditions during comparison.
- **Objective**
  - Design and simulate a novel compact CAM bitcell with improved static leakage characteristics.
  - Achieve fast match-line evaluation suitable for high-speed searching and column-wire writing.
  - Validate the design under PVT variations and mismatch.
- **Type of work (1~2 students):**
  - Full-custom schematic design
  - Full-custom layout design



10T- BCAM cell



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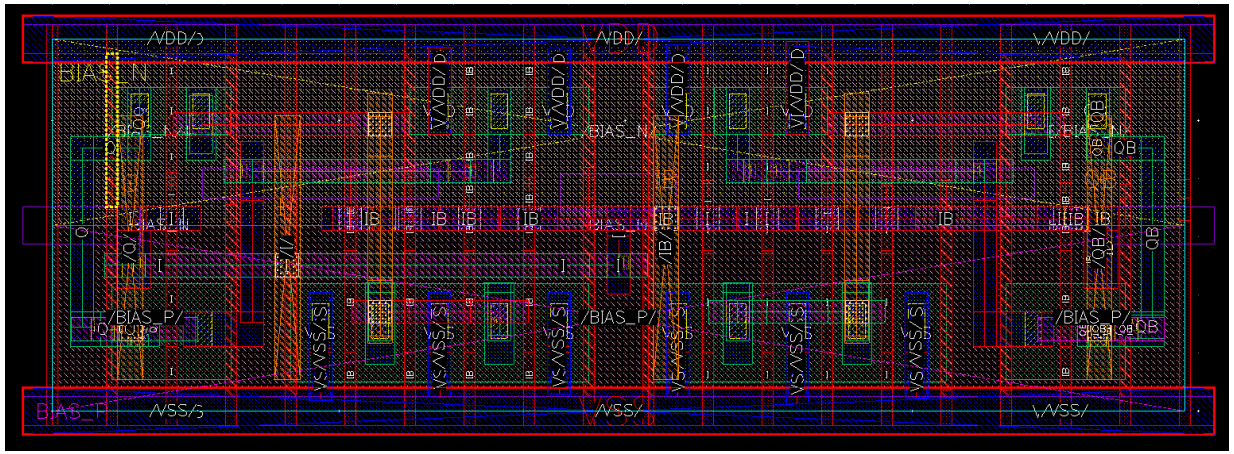
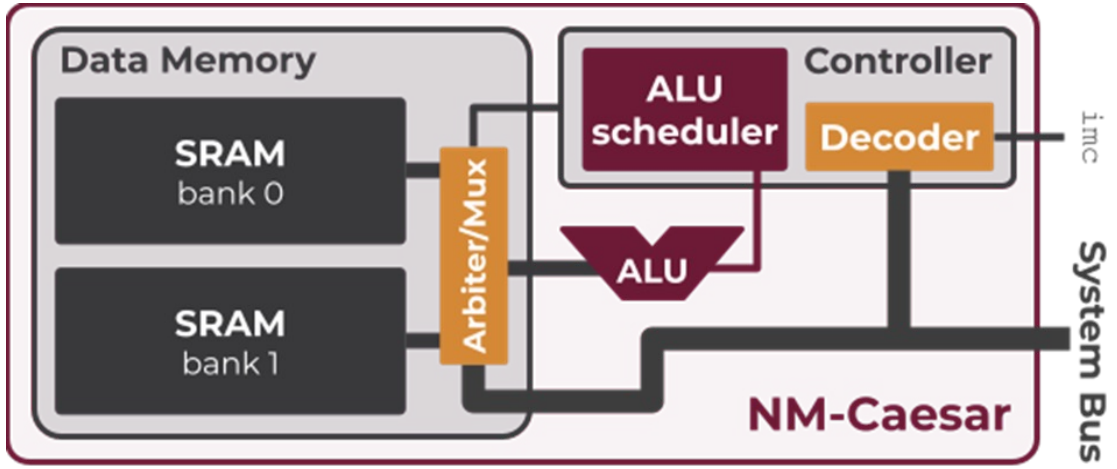
Ultra-low power standard-cells library optimization for AO systems

- **Motivation**
  - Conventional CMOS are highly power hungry + require high design effort to lower their consumption (voltage scaling, clock-gating, reversed body biasing)
  - DPTLSL, a Leakage-Suppression Logic developed at TCL, is a promising logic family to reduce leakage current for low-frequency circuits
- **Objectives:**
  - **Characterize and optimize cells/circuit architecture** for a Leakage-Suppression Logic family (DPTLSL) allowing low-leakage and reliable operations at circuit level (FIR filter).
  - Comparison with a standard CMOS library
- **Type of work:**
  - Cell characterization on Virtuoso
  - Spice and PEX simulation
  - Python development



Near-Memory Computing (NMC) architecture optimization

- **Motivation**
  - One of the main nowadays SoCs performance and energy limitations reside in the memory bandwidth of Von Neuman systems
  - Bring computation into or close to the memory subsystem to use the bandwidth more efficiently and leverage data reutilization: Near-Memory Computing
- **Objectives:**
  - **Improve NM-Caesar RTL to make it configurable** (memory size, nb of banks)
  - Optimize + **Highlights Energy/Area/Performance trade-offs**
- **Type of work:**
  - RTL development
  - Post-synthesis simulation
  - Energy/Performance extraction



Morphological filter circuit optimization

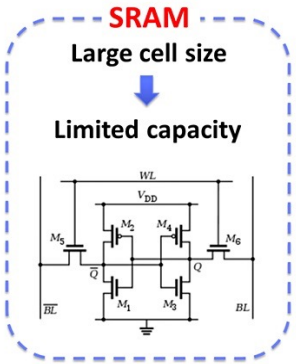
- **Motivation**
  - Morphological filters (erosion, dilation, opening, closing) are widely used as lightweight, robust pre-processing for edge devices: noise removal, shape extraction and contrast enhancement.
  - Circuit-level optimization unlocks orders-of-magnitude improvements in power, area, and throughput compared with software or general-purpose processors.
- **Objectives:**
  - Starting **from the MF python description, design 3 different circuit architectures** (iterative, pipelined, unrolled)
  - Compare and **extract post-synthesis PPA (Performance-Power-Area)**
- **Type of work:**
  - RTL development
  - Post-synthesis simulation
  - Energy/Performance extraction

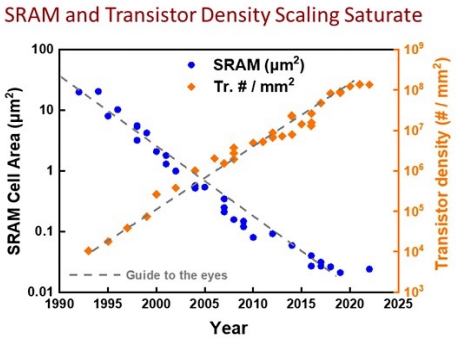
Image after segmentation | Image after segmentation and morphological processing [1]

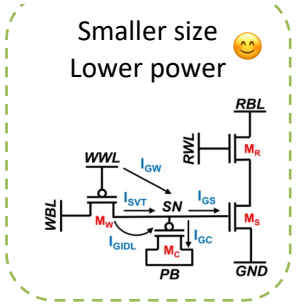
[1] https://towardsdatascience.com/understanding-morphological-image-processing-and-its-operations-7bcf1ed11756/

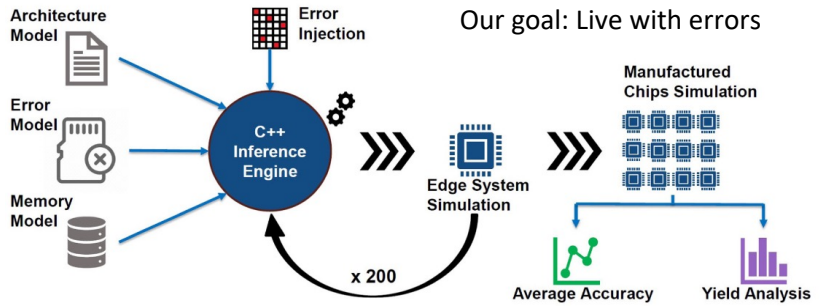
Approximate Computing on GC-eDRAM

- **Motivation**
  - GC-eDRAM has better area & power efficiency, but prone to random data loss due to limited data retention time
  - Some applications (e.g. neural network, error correction codes) are less sensitive to injected errors [1][2]
- **Objective**
  - Explore the algorithms that can live with errors
  - Build a model to obtain the algorithm accuracy, system power
- **Type of work:**
  - Modelling with Python/C(++)
  - Additional exploration with VHDL/Verilog









Our goal: Live with errors

[1] F. Ponzina, M. Peón-Quirós, A. Burg, and D. Atienza, "E2CNNs: Ensembles of Convolutional Neural Networks to Improve Robustness Against Memory Errors in Edge-Computing Devices," IEEE Transactions on Computers, vol. 70, no. 8, pp. 1199–1212, Aug. 2021, doi: 10.1109/TC.2021.3061086.

[2] F. Tu, W. Wu, S. Yin, L. Liu, and S. Wei, "RANA: Towards Efficient Neural Acceleration with Refresh-Optimized Embedded DRAM," in 2018 ACM/IEEE 45th Annual International Symposium on Computer Architecture (ISCA), June 2018, pp. 340–352. doi: 10.1109/ISCA.2018.00037.

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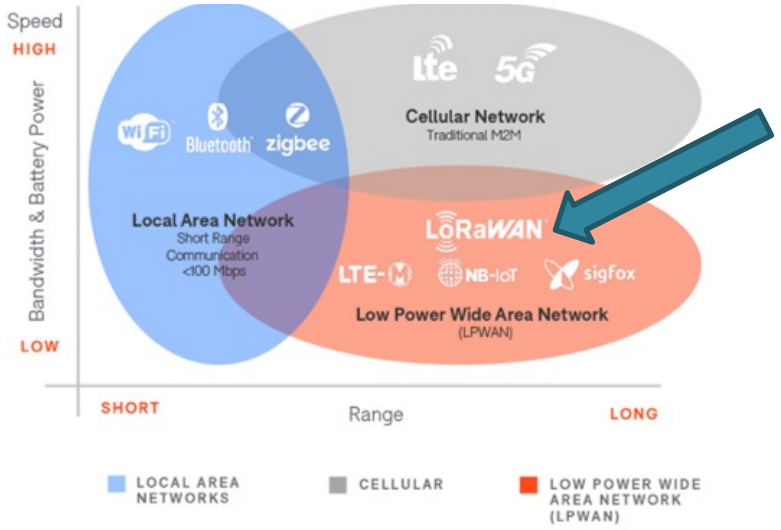
Telecommunications Related Projects

LoRa Software-Defined Radio Evaluation

- **Motivation**
  - We have developed a software-defined radio (SDR) implementation of LoRa, a low-power wide-area technology
  - Experimental evaluation would increase the impact of the opensource implementation (GitHub link)

- **Objective**
  - Evaluate the error rate performance of the SDR implementation
  - Compare with commercial hardware implementations

- **Type of work**
  - C++/Python programming
  - Experimental evaluation using SDRs



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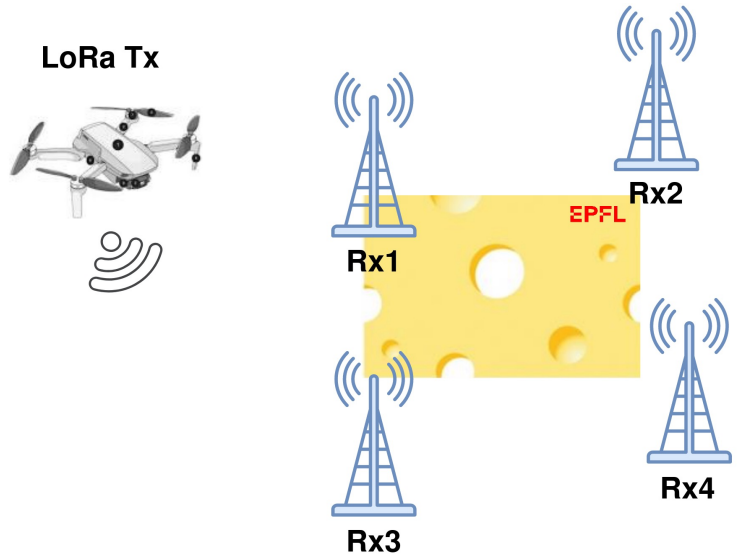
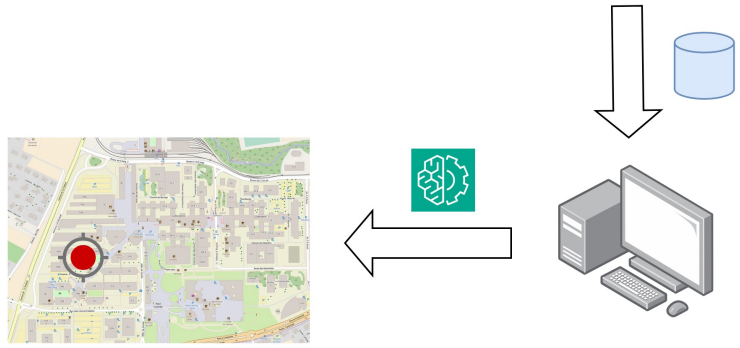
ML-Based Drone Localization with LoRa

- **Motivation**
  - LoRa excels at low-power and long-range communication, however its built-in localization accuracy is relatively weak.
  - Machine learning (ML) could help identify patterns from noisy RSSI/SNR signals to achieve better localization performance.
  - We have approx. 75k drone measurements taken around EPFL which transmits data towards 4 gateways scattered around the campus.



- **Objectives**
  - Implement ML-based models to estimate drone location.
  - Evaluate their performance & robustness in LoRa-based IoT systems.

- **Type of work**
  - Python, Machine learning, Algorithms



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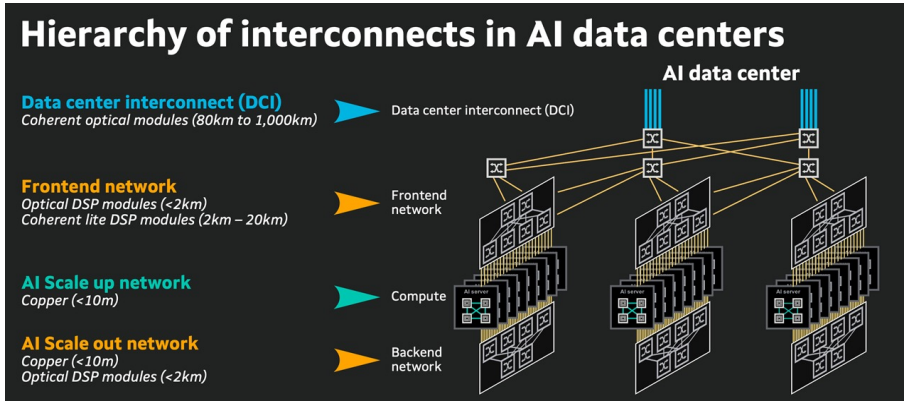
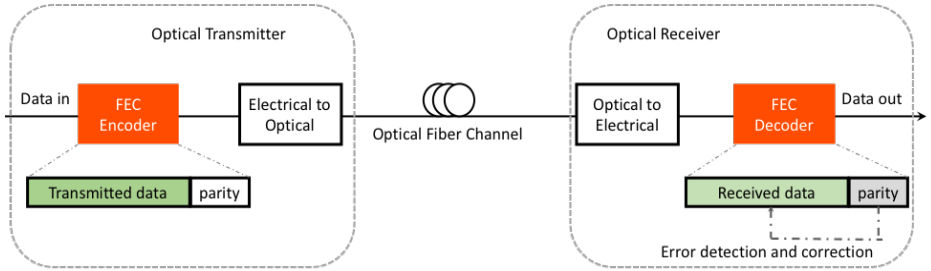
Forward Error Correction for Optical Communication

- **Motivation**
  - Optical communication is widely adopted in AI data center network
  - Forward error correction (FEC) is the essential part to ensure the correctness of transmitted data
- **Objective**
  - Explore FEC decoding algorithms that can meet optical communication standard
  - Reduce the complexity of the decoding algorithms
  - (Optional: Decoder implementation)
- **Type of work:**
  - Math: work with probabilities
  - Software simulation: Python/C(++)
  - Additional exploration with VHDL/Verilog





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Thank you for your attention!