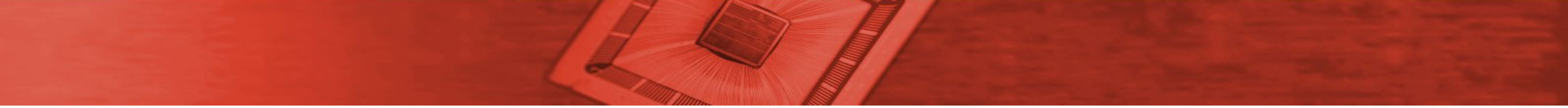


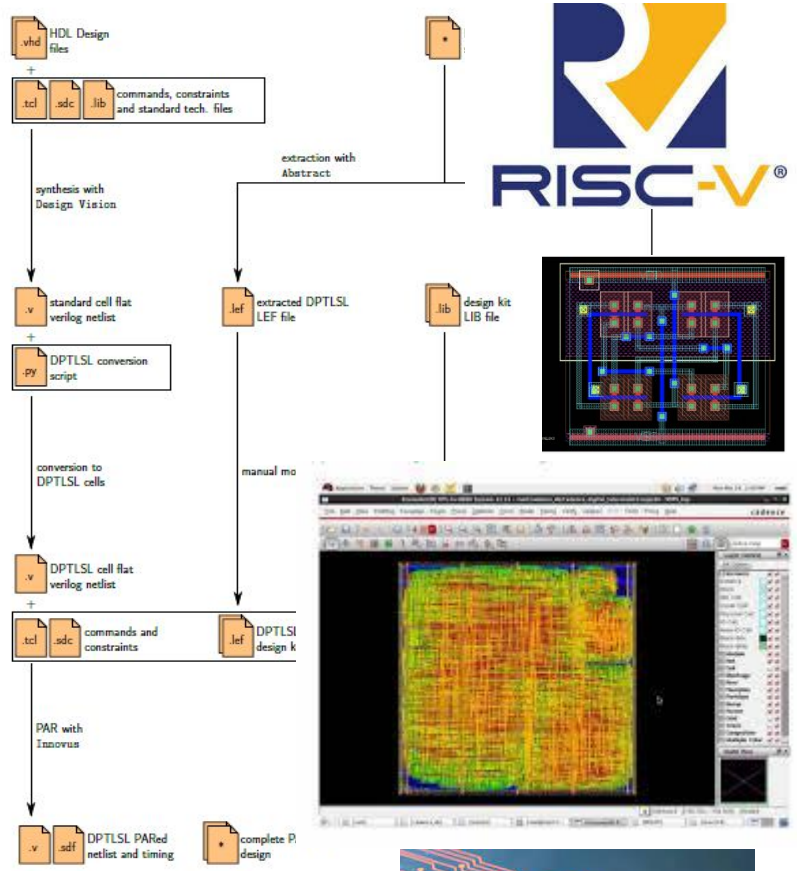
TCL Student Projects

Andreas Burg
Telecommunications Circuits Laboratory

EPFL

DPTLSL RISC-V System-On-Chip

- Motivation
  - X-HEEP is a configurable and heterogeneous RISC-V microcontroller.
  - We want to make a very small version of the X-HEEP (CPU+1 memory bank + GPIOs) and synthesize it with a custom std-cells library with differential logic
  - There is no differential logic synthesizer available
- Tasks/Objectives:
  - Create a very tiny version of X-HEEP
  - make a post-synthesis netlist with differential logic standard cells.
  - Make a model of such standard cells (3 to 4 gates) in Verilog
  - Verify that post-synthesis netlist works by running a simple test.
  - ***Bonus***: The post-synthesis netlist post-processing is made using the yosys open-source synthesizer
- Type of work: HDL development (20%), synthesis and PnR flow (60%), verification (20%).
- Prerequisites: Verilog, TCL, DC, Innovus common UI



davide.schiavone@epfl.ch
clement.chone@epfl.ch

chip2chip serial-link for RISC-V Microcontrollers

- Motivation
  - X-HEEP is a configurable and heterogeneous RISC-V microcontroller.
  - We want to integrate a chip2chip IP to make two X-HEEP communicate by means of memory mapped read/write operations
- Tasks/Objectives:
  - Understand how the serial-link IP (https://github.com/pulp-platform/serial_link) work and how to connect it to X-HEEP, including the bridge to translate the X-HEEP bus to AXI
  - Extend the current Pynq-Z2 FPGA support by including the serial-link
  - Deploy the new X-HEEP on two different FPGAs and write a C test to exchange data between the 2 microcontrollers.
- Type of work: HDL development (70%), FPGA flow (10%), verification (20%).
- Prerequisites: SVerilog, RTL, FPGA

davide.schiavone@epfl.ch

Design automation of in-memory computing

- Motivation
  - In memory computing (IMC) is a promising research line being explored in EPFL
  - The BLADE IMC architecture has been designed and taped-out in 65nm with a specific configuration
  - We would like to automate its design first in 65nm for arbitrary configurations, and later for various technologies.
- Tasks/Objectives:
  - Start from an existing IMC design
  - Automate the design of a memory decoder for IMC (innovus)
  - Automate the design of a local memory controller for IMC (innovus)
  - Depending on the outcomes, explore with open source PnR tools
- Type of work: HDL development (40%), synthesis and PnR flow (40%), automation of the flow from configuration to GDS (20%).
- Prerequisites: VHDL, TCL, Innovus common UI, Python

Alexandre.levisse@epfl.ch
clement.chone@epfl.ch

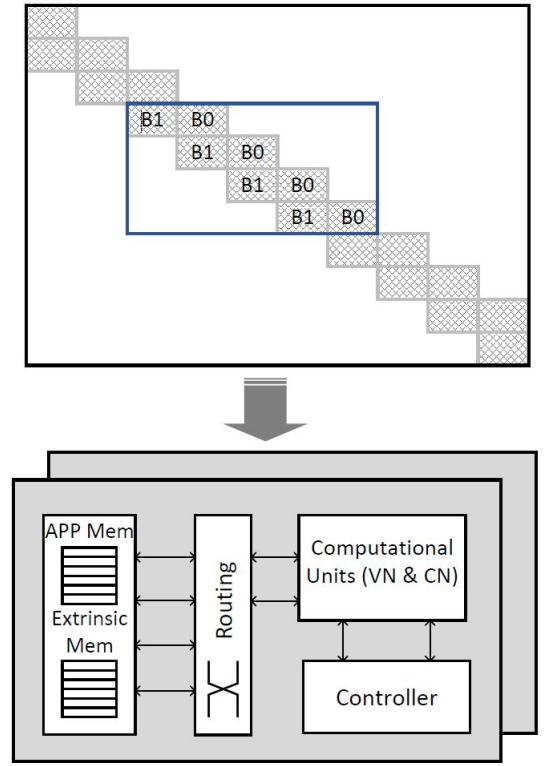
Characterization of an in-memory computing on Silicon

- Motivation
  - In memory computing (IMC) is a promising research line being explored in EPFL
  - Two configurations of the BLADE IMC architecture have been designed and taped-out in 65nm in 2023.
  - We would like to characterize the two architectures in various voltage/temperature conditions.
- Tasks/Objectives:
  - Understand the designs sent for fabrication
  - Understand how to use the board and how to write test programs
  - Characterize the memory, verify its functionality and extract metrics
  - participate in the writing of a publication
- Type of work: learning about the circuit and architecture (20%) C programming (30%), on-board characterization (30%), data analysis and visualization (20%)
- Prerequisites: Python, C code, Verilog, circuit schematic and layout, matlab

Alexandre.levisse@epfl.ch
clement.chone@epfl.ch

Decoder with Bit-Flipping Post-Processing for 6G wireless

- Motivation
  - 6G wireless needs a more powerful decoder
  - T/P of >100Gbps, area efficiency of 10-100Gbps/mm2, power of 1pJ/bit
  - Bit-flipping offers low-complexity post-processing to balance between the quantization overhead and error-rate in a 6G decoder
- Tasks/Objectives:
  - Familiarize yourself with the provided decoder and classical flipping algorithms
  - Develop bit-flipping decoding and design the hardware architecture
  - Implement the architecture in VHDL and verify
  - Benchmark and optimize the design
- Type of work: MATLAB or C++ (40%), hardware architecture (30%), HDL implementation (30%)
- Prerequisits: VHDL, MATLAB or C++

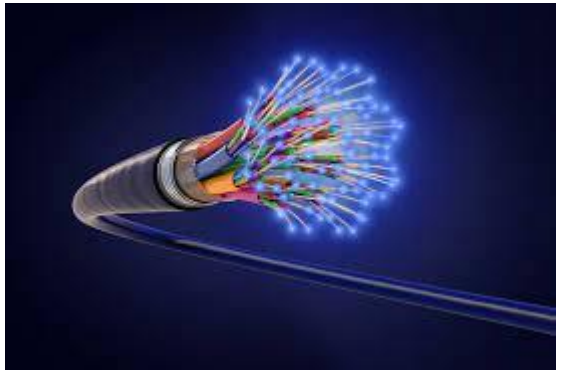


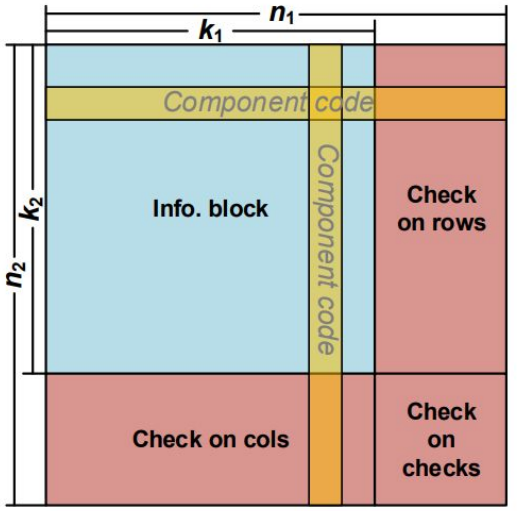
Yuqing Ren: yuqing.ren@epfl.ch
Yifei Shen: yifei.shen@epfl.ch

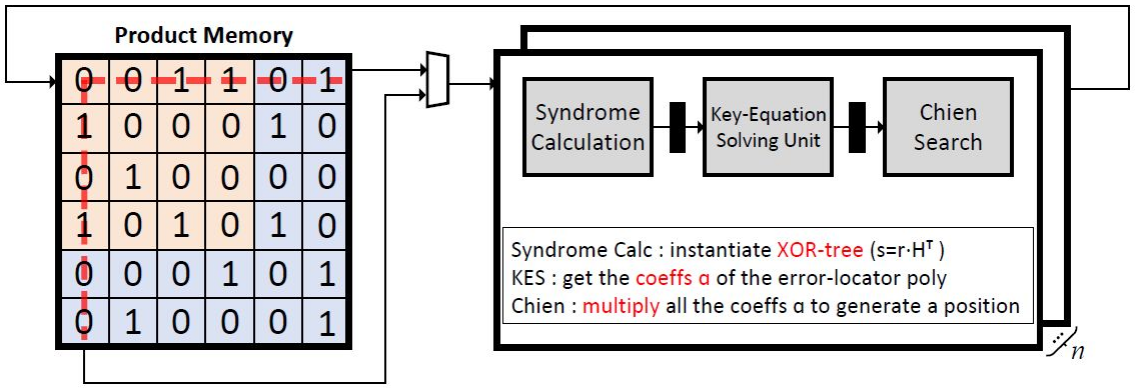
High-Throughput Hard-Decision Decoder for Optical Communications

Yuqing Ren: yuqing.ren@epfl.ch
Yifei Shen: yifei.shen@epfl.ch

- Optical fiber standards 400G-ZR, 800G-ZR
  - High throughput of 400G – 800G
  - Coding design of two-dimensional parity checks
  - Low-complexity iterative hard-decision decoding (e.g., IBDD)
- Tasks/Objectives:
  - Familiarize yourself with the basic IBDD decoder
  - Develop a low-complexity IBDD architecture
  - Implement the architecture in VHDL and verify
  - Benchmark and optimize the design
- Type of work: MATLAB or C++ (20%), hardware architecture (40%), HDL implementation (40%)
- Prerequisits: VHDL, MATLAB or C++



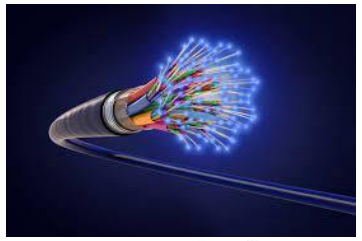


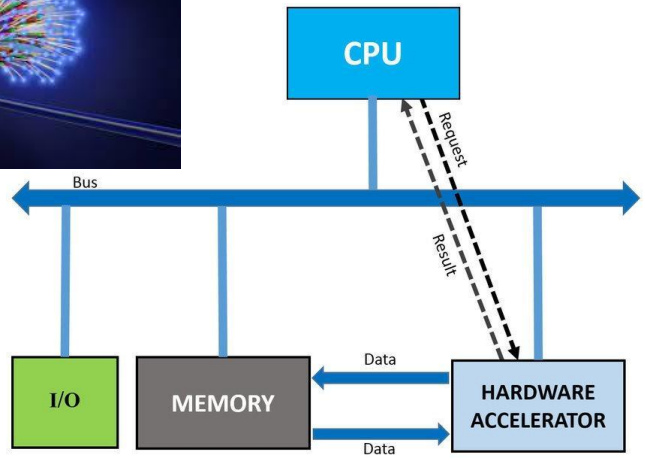


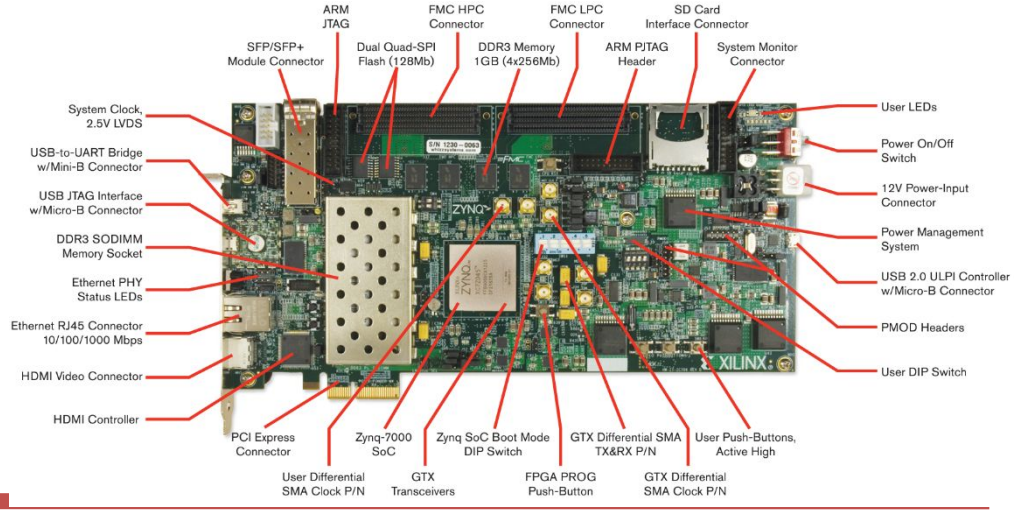
Test Platform of Error-Correction Decoders on FPGA SoC

Yuqing Ren: yuqing.ren@epfl.ch
Andreas Kristensen: andreas.kristensen@epfl.ch

- Motivation
  - FPGA SoCs allow for the hardware to be reprogrammed and configured as needed, offers flexibility in testing various types of decoders (like 5G, 6G, optical fiber)
  - Compared to traditional ASIC, FPGA SoCs enable faster prototype development by simply reconfiguring the FPGA
  - Hardware acceleration, faster than software simulations
- Tasks/Objectives:
  - Familiarize yourself with provided FPGA board and basic decoder
  - Configure I/O, Bus, communications between CPU and FPGA
  - Implement the test platform on FPGA SoC and verify
  - Benchmark and optimize the design
- Type of work: digital architecture design (25%), HDL implementation (50%), programming (25%)
- Prerequisits: VHDL, embedded systems



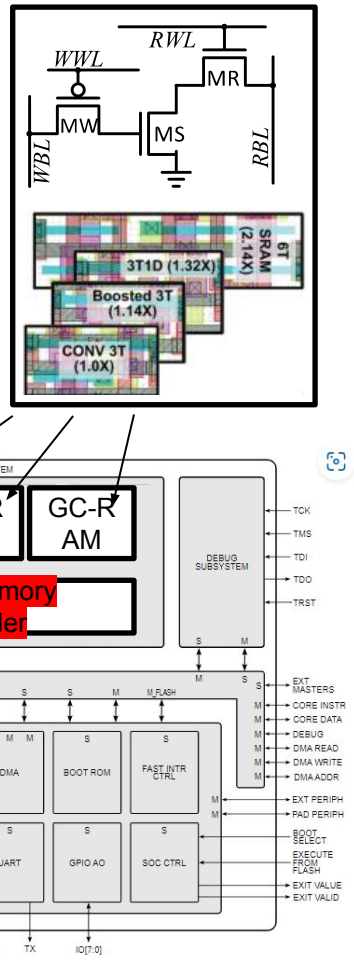




GC-RAM Controller for X-HEEP

- Integration of GC-RAM into X-HEEP platform
  - Memory controller for dynamic GC-RAM
  - Handle refresh and access multiplexing
  - Perform error detection and correction
- Tasks/Objectives:
  - Set up X-HEEP working environment
  - Familiarize yourself with the bus protocol
  - Develop a memory controller architecture
  - Implement the architecture in VHDL and verify
  - Benchmark and optimize the design
- Type of work: digital architecture design (25%), HDL implementation (50%), programming (25%)
- Prerequisits: VHDL, embedded systems

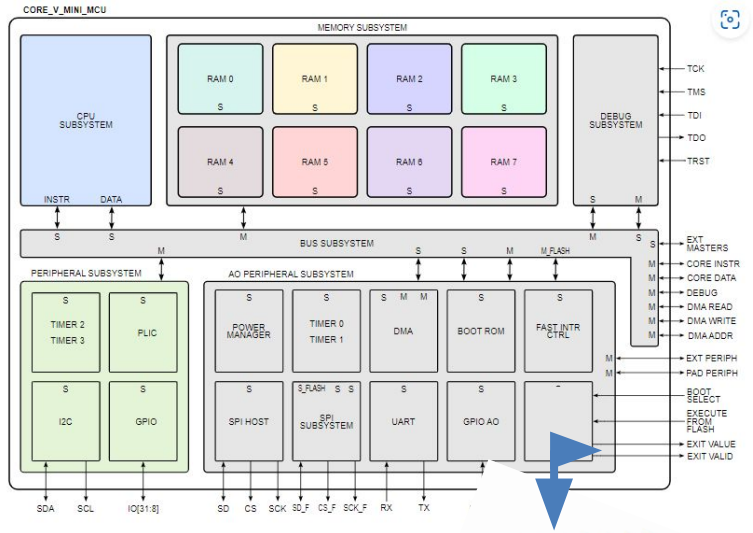
GC-RAM is a more dense, but dynamic form of storage that benefits from a smart memory controller that handles refresh operation and interfaces to a system bus

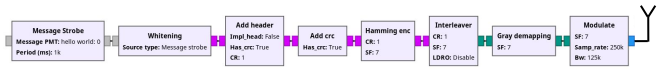


Andreas Burg: andreas.burg@epfl.ch

Design of a Wireless Modem for IoT

- Background
  - LoRa is a communication standard for ULP IoT nodes
  - Relatively simple Physical Layer with super simple TX and a rather simple RX
- Tasks/Objectives:
  - Familiarize yourself with the LoRa physical layer DSP
  - Implement a golden model for the LoRa TX (including FixedP)
  - Develop an architecture for a LoRa transmitter
  - Implement the architecture in VHDL and realize a bus interface
  - Test your system on an FPGA
- Type of work: algorithm & golden model (25%), architecture design & optimization (25%) HDL implementation (25%), SW (25%)
- Prerequisits: VHDL, interest in algorithm/architecture co-design, possibly some communications background



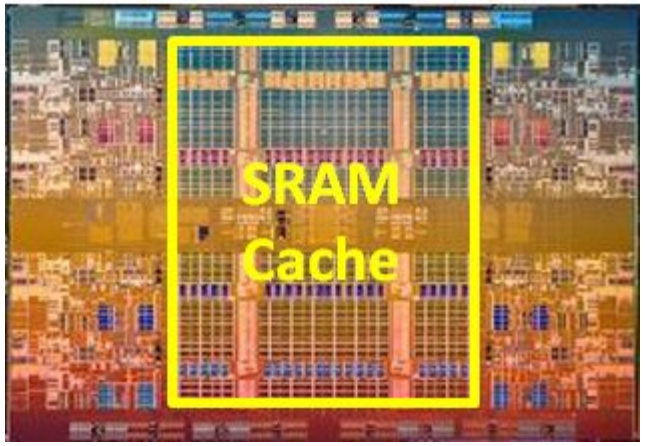


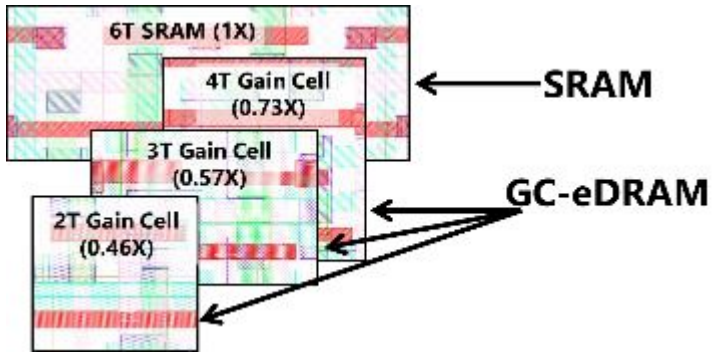
Andreas Burg: andreas.burg@epfl.ch

Test of the fabricated GC-eDRAM chip

- Motivation
  - There is an increasing need for **on-chip embedded memories** as they offer high-speed data movement between the processing units and the memory.
  - Embedded memories constitute **over 50% of the area** and power consumption of many computing systems.
  - We develop GC-eDRAM for an **alternative to SRAM** to:
    - Increase area density.
    - Lower power consumption.
    - Enable dual port operation.
  - We fabricated several chips with GC-eDRAM macro and they need a extensive characterization in the lab enviroment.
- Tasks/Objectives:
  - Perform a communication between computer and fabricated chip
  - Perform various analysis (temperature, voltage scaling, frequency sweep, and …) on the lab environment
  - Compare results with the CAD environment simulations.
- Prerequisites
  - Intermediate level programing languages (Python, VHDL, and C)

Intel 8 core Xeon X7560

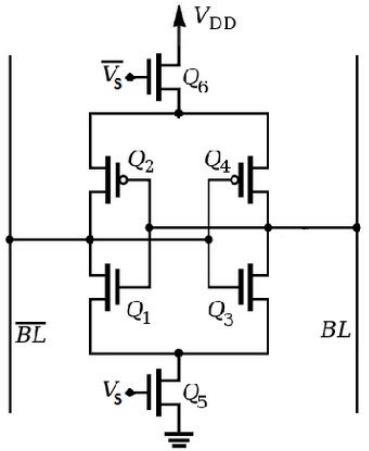




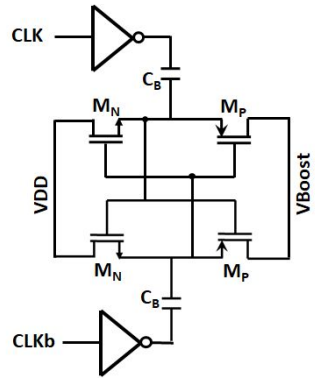
Andac Yigit : halil.yigit@epfl.ch

Improving blocks of the GC-eDRAM in 28nm FDSOI Process

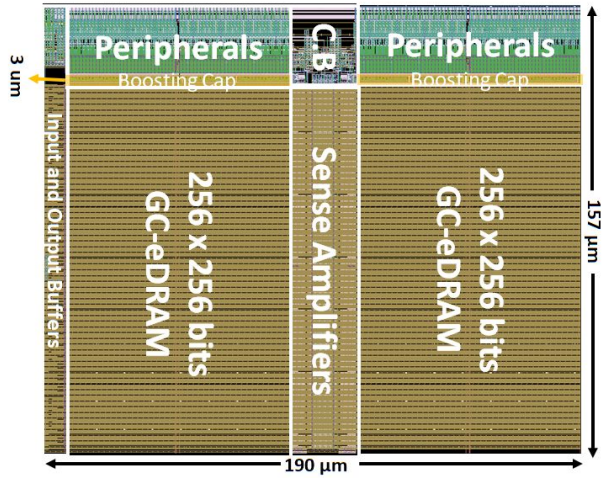
- Motivation
  - Improve the GC-eDRAM macro with new analog blocks to extend the data retention time.
  - Design full-custom analog circuits in advanced technology nodes.
  - Developing new ideas for power management and asist-techniques for memory circuits.
- Tasks/Objectives:
  - Making analysis on a existing block to understand requirement for the design.
  - Design of the desired block at the virtuoso.
  - Simulation of the design block with a GC-eDRAM macro.
  - Drawing layout of the designed block.
  - Post-layout optimization of the designed block.
- Prerequisites
  - Analog circuit design knowledge.
  - Intermediate level virtuoso usage.



Sense-Amplifier



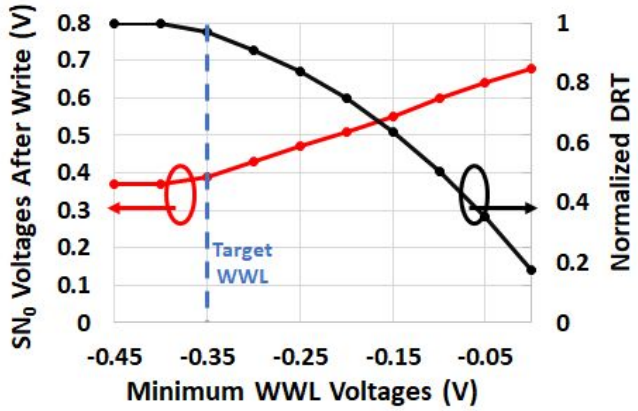
Charge-Pump

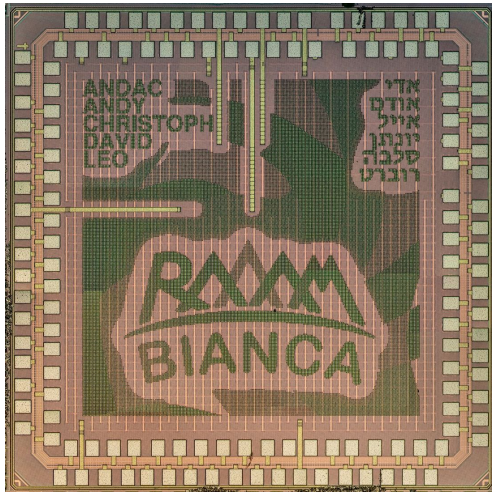


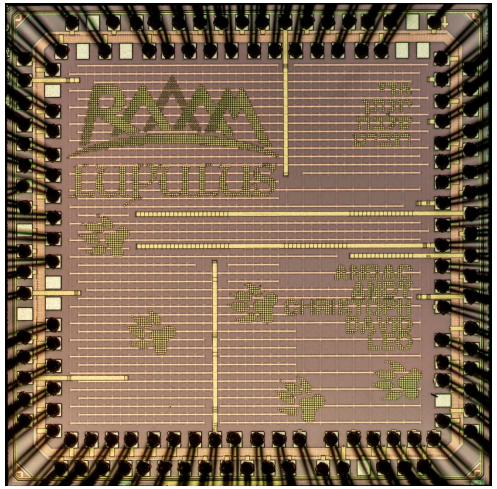
Andac Yigit : halil.yigit@epfl.ch

Designing Analog Blocks for the GC-eDRAM at 16nm FINFET

- Motivation
  - Get involved with the new generation GC-eDRAM macro design on 16nm technology.
  - Designing well-known blocks (ADC and voltage buffers) for the characterization of the macro.
  - Make an adaptive, self calibrating macros according to the environmental variations.
- Tasks/Objectives:
  - Literature research on the selected block.
  - Design of the desired block at the virtuoso.
  - Drawing layout of the designed block.
  - Post-layout optimization of the designed block.
- Prerequisites
  - Analog and digital circuit design knowledge.
  - Intermediate level virtuoso usage.



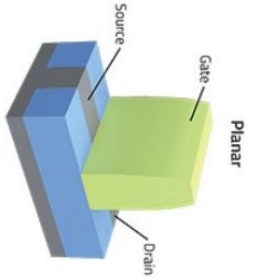


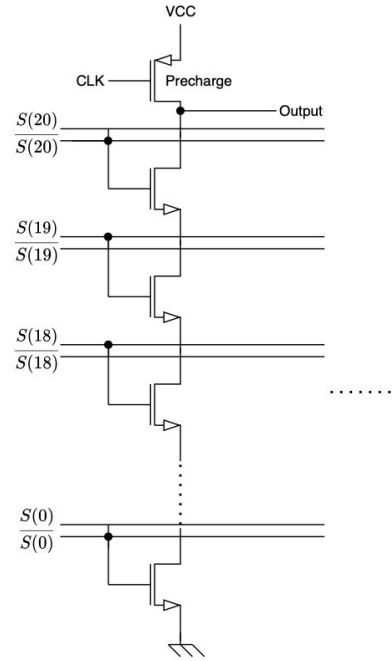


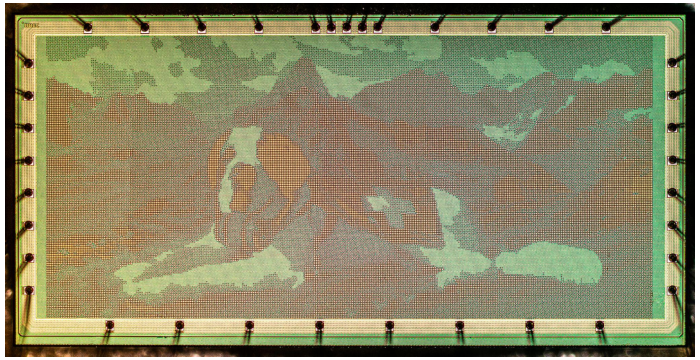
Andac Yigit : halil.yigit@epfl.ch

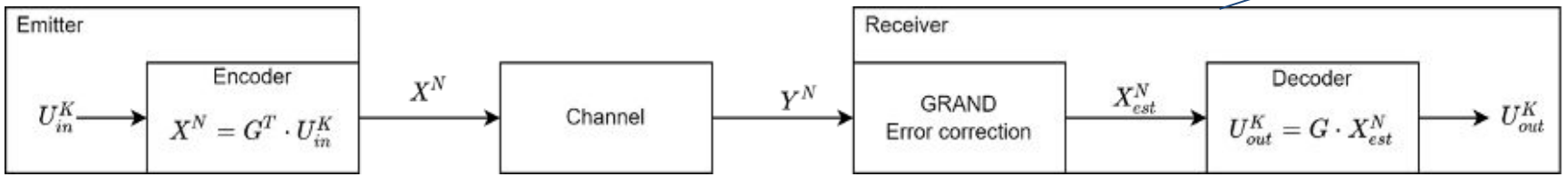
Designing a decoder in 16nm FinFet

- Motivation
  - A digital message is prone of errors. GRAND (an algorithm), decodes a received message by comparing it to all possibilities of inverting bits → Requires a lot of computation (341503 for a message of 127 bits to correct 3 errors).
  - A first chip (65 nm) for proof of concept has been done
  - Participate on 1st projects in 16nm of the lab
- Tasks/Objectives:
  - Implement a full-custom implementation of the decoder using dynamic logic, in-memory computation style in 16nm FinFet
  - Automatisation of layout generation with python scripts
- Type of work:
  - Full-custom Digital design
  - HDL (verilog, sv or vhdl) and python





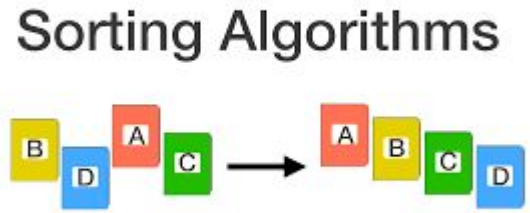


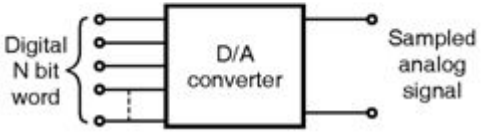


Ludovic Blanc: ludovic.blanc@epfl.ch

Mixed signal compute block

- Motivation
  - In the field of telecommunications, particularly in 5G/6G, algorithms must operate at extremely high speeds.
  - When a digital block, like a sorter, becomes a bottleneck, the common approach is to redesign it using full-custom techniques. However, if this proves inadequate, further optimization can be explored through a mixed-signal approach.
  - This represents a novel approach to circuit design.
- Tasks/Objectives:
  - The objective is to design blocks for analog sorters, encompassing DACs and comparators, while ensuring compatibility with standard cell dimensions.
- Type of work:
  - digital and analog design
  - Cadence tools, possibility of doing hdl and python

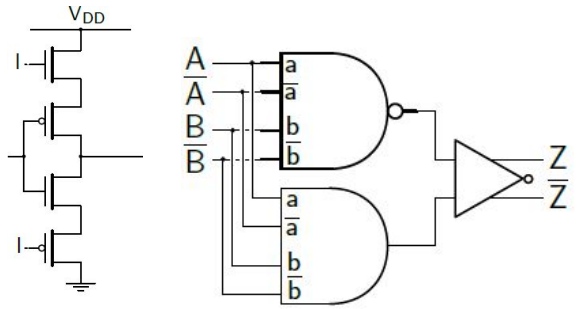


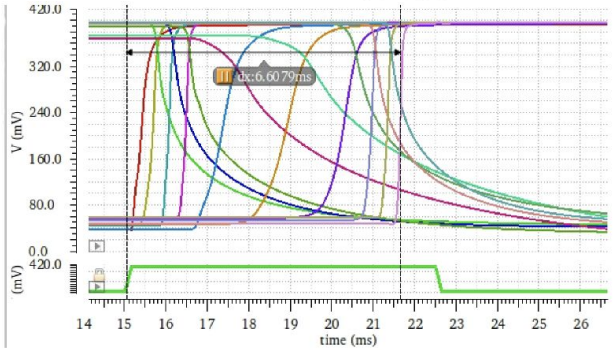


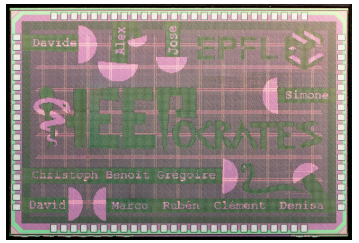
Ludovic Blanc: ludovic.blanc@epfl.ch

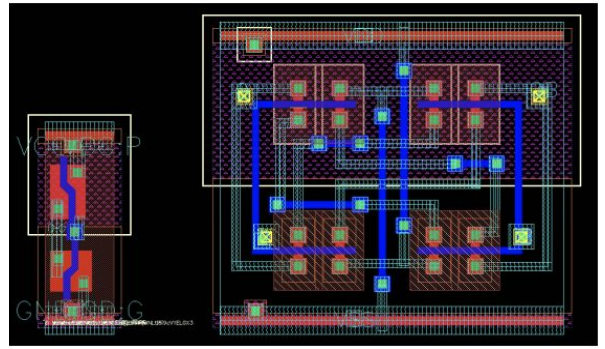
Designing a Leakage Suppression SRAM / ROM in 16nm FinFET

- Motivation
  - Low power circuits spend the vast majority of the time in deep sleep modes in order to achieve the battery life required for their task
  - When to wake up the chip? -> Dedicated small always on logic which can sample sensor data and decide whether to start up the full design
    - Leakage suppression logic can massively reduce the leakage of the always-on circuit if a hit on the circuit speed is acceptable
    - Many algorithms require Memory which might contribute a significant share of the always on logic power
- Tasks/Objectives:
  - Literature research on leakage suppression logic
  - Evaluate the feasibility of leakage suppression on a memory macro
  - Characterize the speed and leakage
  - Design a bitcell array with leakage suppression
- Prerequisites:
  - Analog and digital knowledge, designing and simulating hierarchical designs in Virtuoso



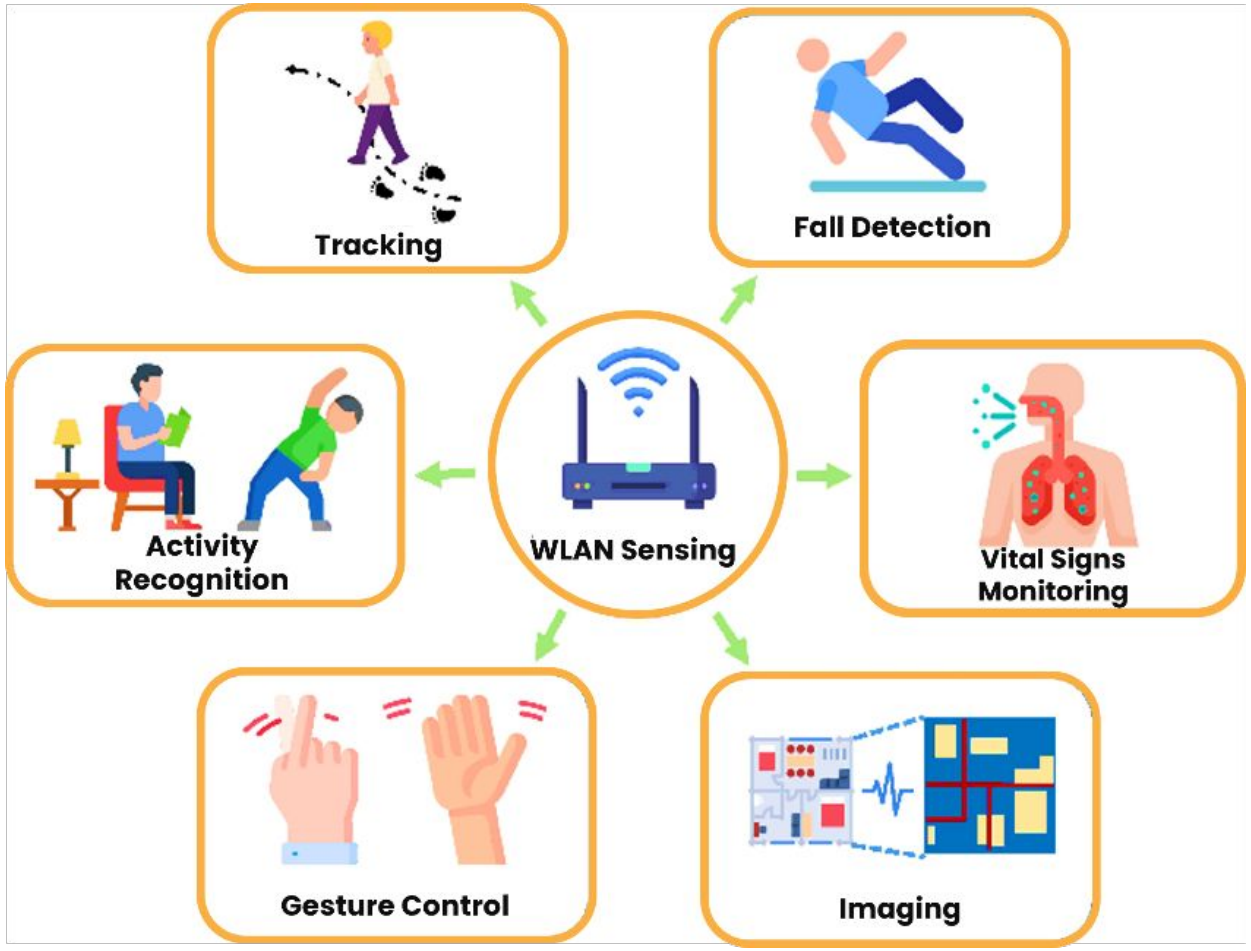






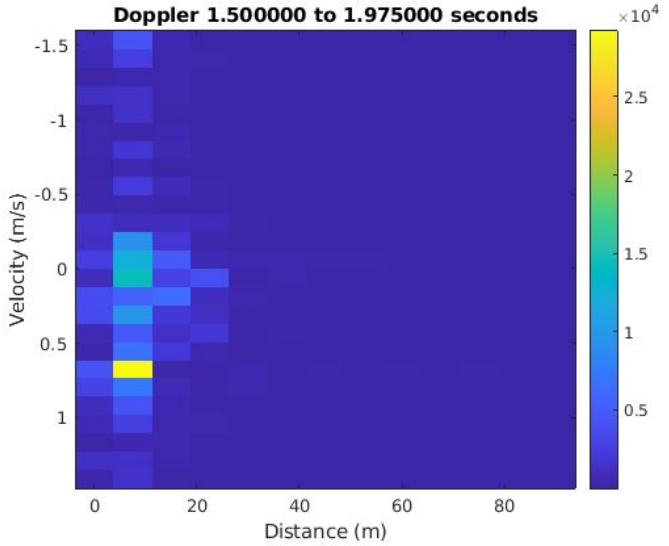
Christoph Müller, christoph.mueller@epfl.ch

Environment sensing with wireless signals



Project 1: Localization and User Activity Detection

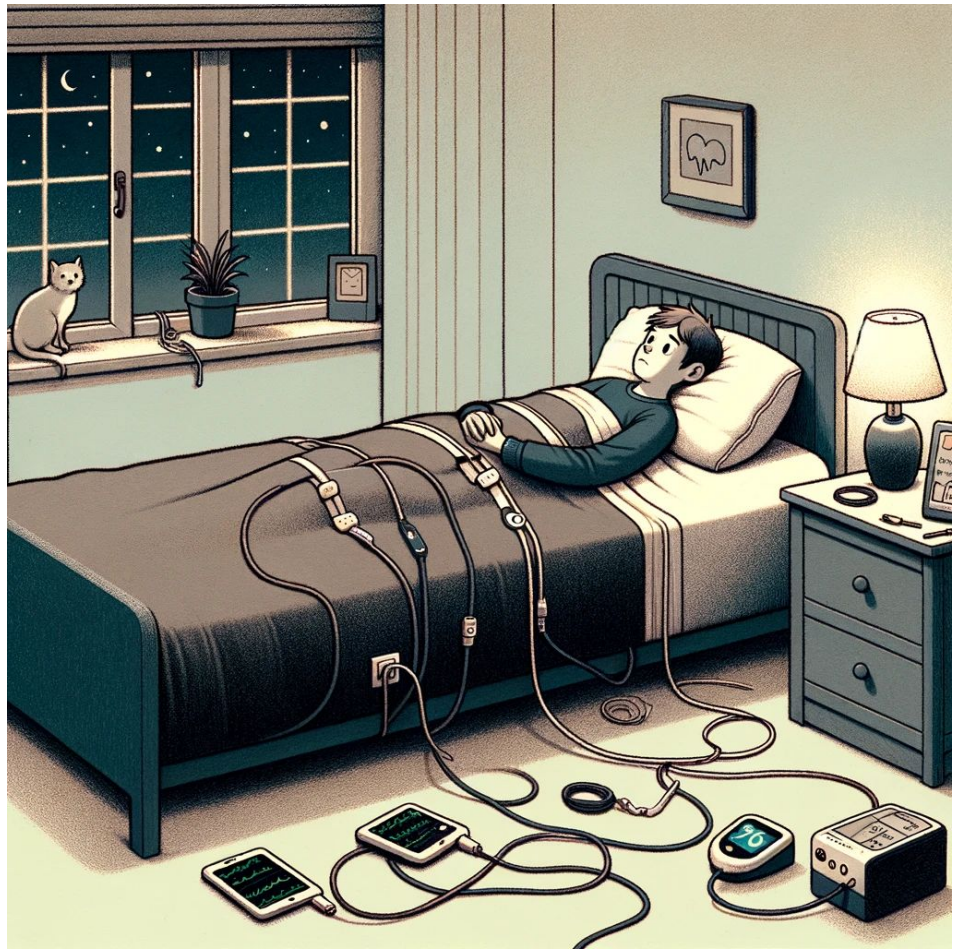
- Motivation
  - Current methods for activity detection and localization require the use of cameras (intrusive) or wearables (restrictive)
  - The received wireless signal varies depending on where people are and what they are doing
- Tasks/Objectives:
  - Collect and label data for different classes of activity in different locations
  - Develop pre-processing steps and models for classification and/or localization
  - Present a system that can detect different classes of user activity, room state and localization based on Wi-Fi signals.
- Prerequisites:
  - Signal processing, MATLAB/Python, machine learning is a plus



Andreas Kristensen: andreas.kristensen@epfl.ch

Project 2: Vital-Signs Estimation

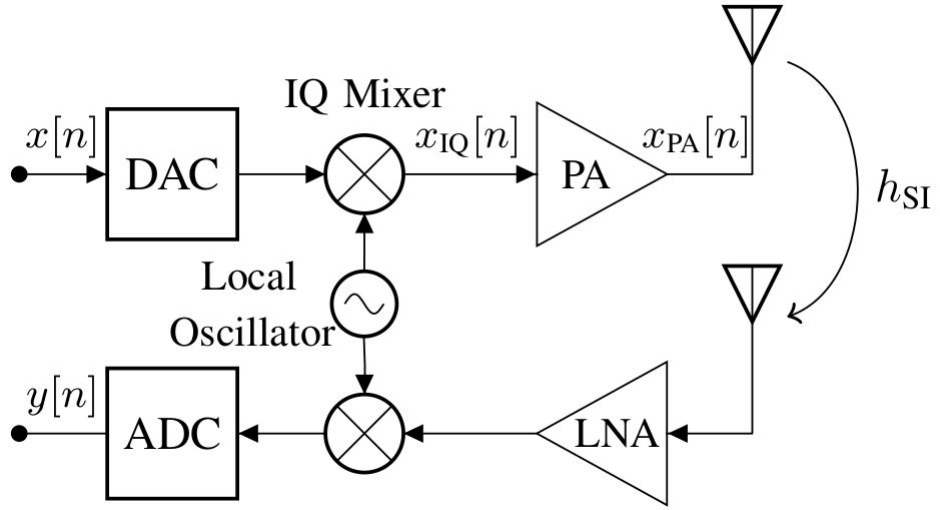
- Motivation
  - Current methods for vital-signs estimation rely on the use of a lot of hardware that can be specially very invasive for breathing monitoring
  - The movements from breathing and heart-beats can be detected from the reflected wireless signals
- Tasks/Objectives:
  - Collect data with varying breathing rates in different scenarios
  - Develop pre-processing steps and models for estimation in various scenarios (short/long distances etc.)
  - Present a system to detect breathing of one or multiple people in different scenarios
- Prerequisites:
  - Signal processing, MATLAB/Python, machine learning is a plus

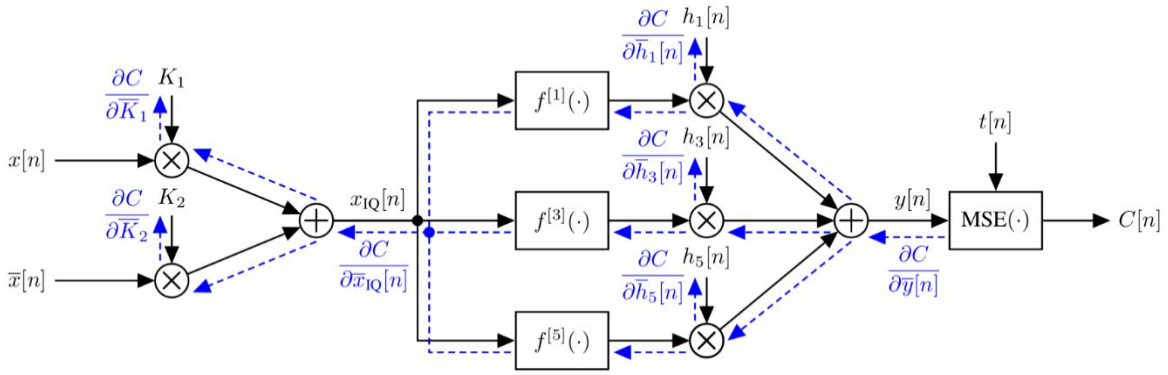


Andreas Kristensen: andreas.kristensen@epfl.ch

Project 3: Hardware and Machine Learning for Enhancing Wi-Fi Radar

- Motivation
  - A Wi-Fi router that transmits and receives its own signal mostly sees the signal from the transmit antenna instead of the reflections of the environment
  - You can cancel out this signal in various ways:
    - Transmit a cancellation signal (hardware and machine learning)
    - Post-process the received signal (machine learning)
- Tasks/Objectives:
  - Define a model to implement for the cancellation, e.g., a neural network
  - Implement a quantized version of the canceller in PyTorch/Tensorflow
  - Design, implement, and test canceller in a real system
- Prerequisites:
  - VHDL/Verilog/Systemverilog, C, Python, ML/NNs (a plus, but not mandatory)

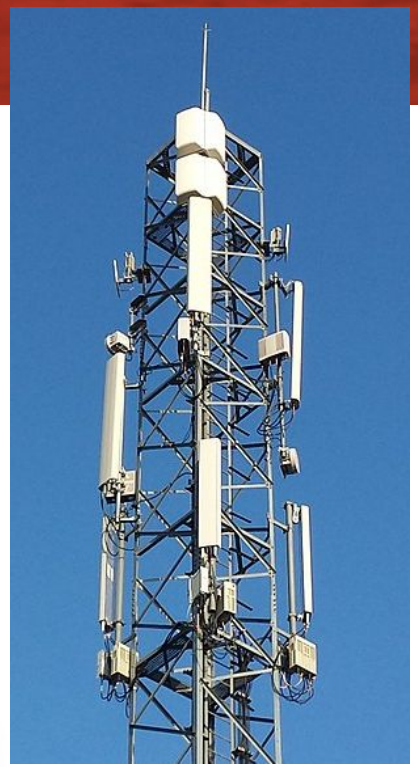




Andreas Kristensen: andreas.kristensen@epfl.ch

Project 4: 4G LTE Localization

- **Topic:**
  - Adapt and employ an open-source 4G software radio suite to gather channel state information from LTE signals
  - Localize device or device free target with channel state information
- **Tasks/Objectives:**
  - Enable stable data collection from LTE link
  - OFDM frame structures for LTE
  - Read and processing channel state information
- **Type of work:** 70% C/C++, 30% python
- **Pre-requisites:** C++



CSI

weather, traffic, location…

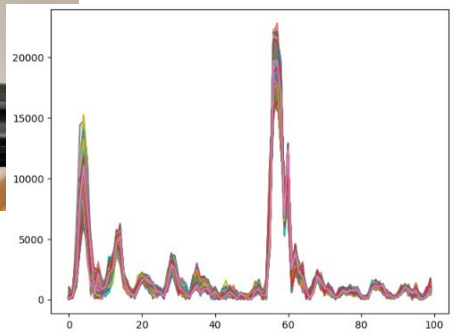
Contact: Sitian LI (sitian.li@epfl.ch)

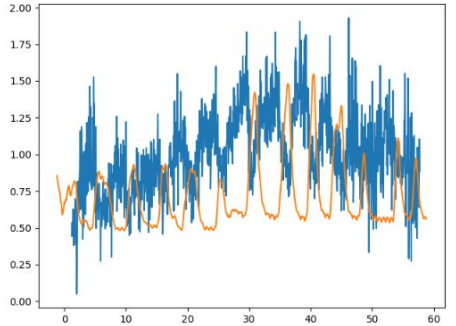
Project 5: UWB Environment and Human Activity Sensing

- **Topic:**
  - Sensing environments (vital signs, human activities) with UWB/WiFi signals
  - Collect and process channel estimations to retrieve environment/activity information

- **Tasks/Objectives:**
  - Synchronize/align channel impulse responses
  - Preprocessing

- **Type of work:** 50% Algorithm, 40% python, 10% C/C++
- **Pre-requisites:** Digital signal processing, Wireless communication basics, Machine learning as a plus

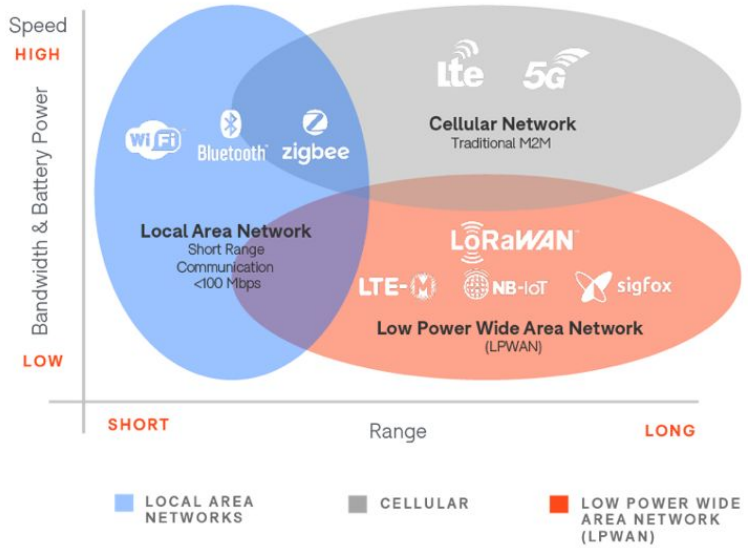




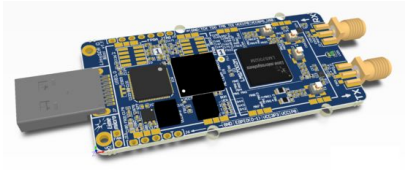
Contact: Sitian LI (sitian.li@epfl.ch)

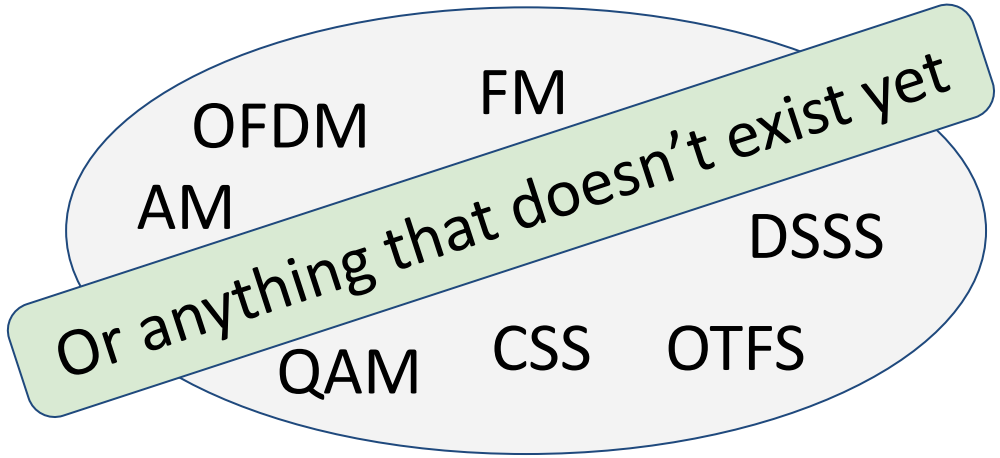
Low-power Wide-area Networks (LPWAN)

- **Low-power, long-range, low-rate** technologies have many application for monitoring/controlling large IoT systems
- Due to their popularity, those networks face multiple challenges caused by densification
- We want to **create useful tools** for the research community to study LPWANs
- **Software-defined radios** are very powerful devices allowing for quick prototyping.



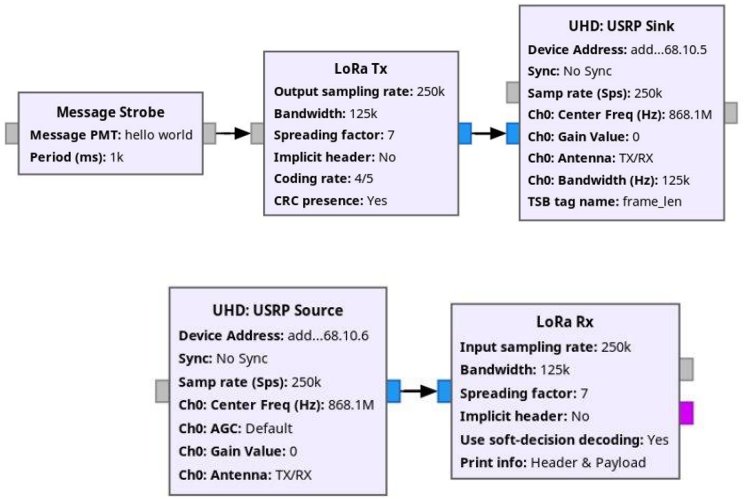
GNURadio
THE FREE & OPEN SOFTWARE RADIO ECOSYSTEM

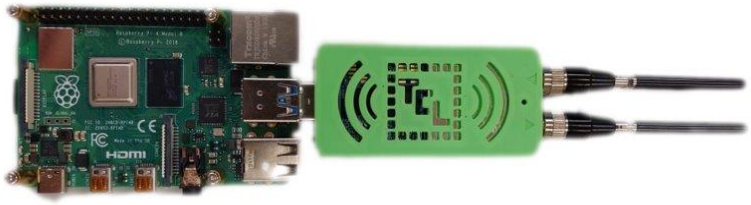




Project 1: LoRa Transceiver Optimization and Evaluation

- **Motivations:**
  - We have an **open-source implementation** of a LoRa transceiver
  - 15’000 visitors and 2’000 clones last year
  - Improvement to the repository helps both the research community and radio enthusiasts to use it
- **Tasks/Objectives:**
  - **Characterize the current system** in terms of memory footprint, computational load and performance
  - **Add features** to the [public repository]



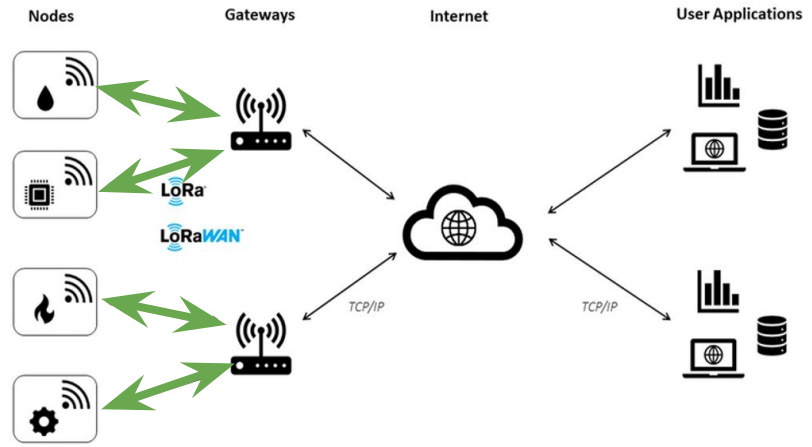


- **Type of work:** 60% C++, 20% GNURadio, 20% Measurements
- **Pre-requisits:** C++, Wireless communication basics

Contact: joachim.tapparel@epfl.ch

Project 2: LoRaWAN for SDR

- **Motivations:**
  - Our implementation only supports the physical layer of LoRa
  - We want to **add LoRaWAN support** using open-source libraries.
- **Tasks/Objectives:**
  - Familiarize with GNU Radio, a popular software defined radio programming framework
  - **Create an interface** between an existing MAC layer library to our LoRa transceiver



- **Type of work:** 80% C++, 20% GNURadio
- **Pre-requisits:** C++

THE THINGS NETWORK

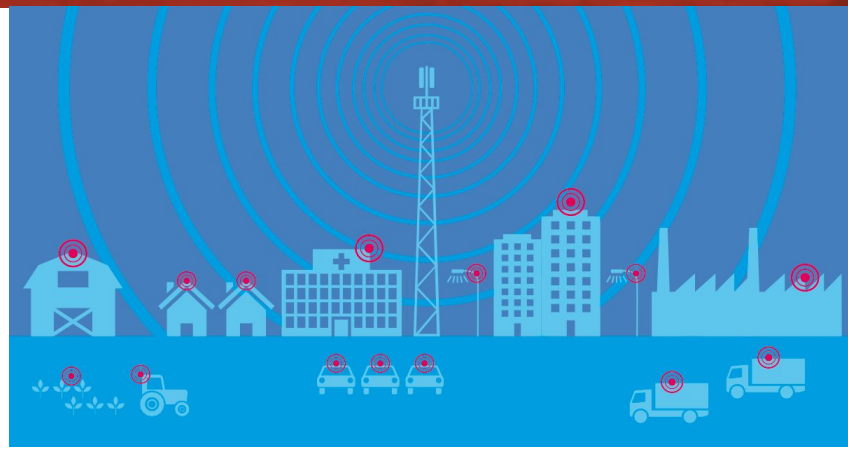
Contact: joachim.tapparel@epfl.ch

Project 3: Implementing a Mioty Transceiver

- **Motivations:**
  - Mioty is an **open technology** standard for LPWAN
  - We want to build **the first open-source SDR** implementation

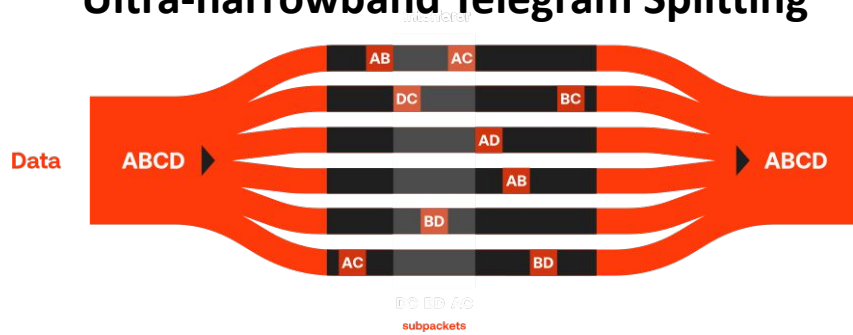
- **Tasks/Objectives:**
  - Familiarize with the technology specifications
  - Implement a simple mioty transceiver
  - Verify compatibility with commercial radio chips

- **Type of work:** 60% C++, 20% GNURadio, 20% datasheet
- **Pre-requisits:** C++, Wireless communication basics



mioty

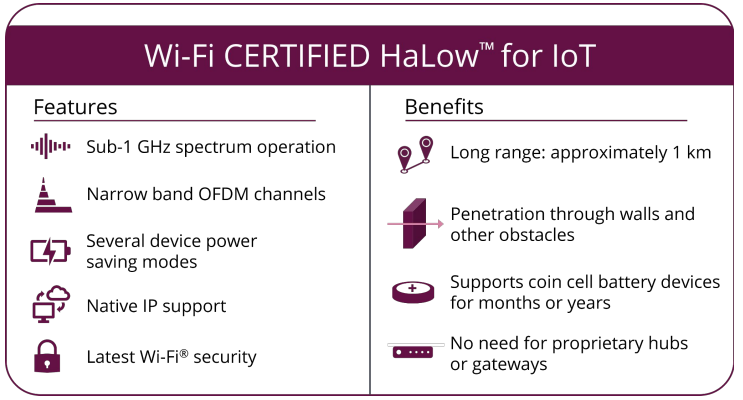
Ultra-narrowband Telegram Splitting

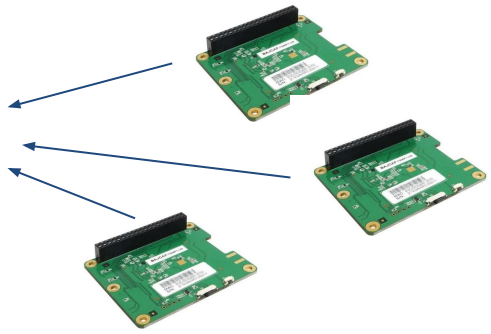


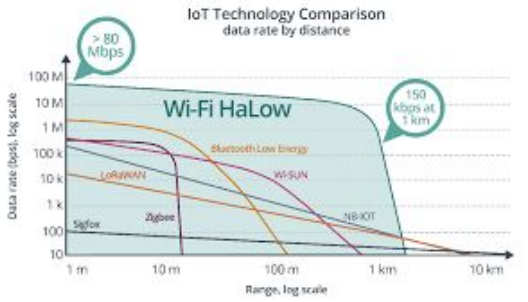
Contact: joachim.tapparel@epfl.ch

Project 4: Characterizing the New WiFi HaLow

- **Motivations:**
  - WiFi HaLow is a new version of WiFi specifically for IoT
  - It supports very long range and ULP consumption with WiFi
  - Brand new chipsets have recently been delivered, but their performance under CH regulations is unclear
- **Tasks/Objectives:** **Set up the first WiFi HaLow network in Switzerland and characterize its performance**
  - Familiarize with the technology and the available boards
  - Set up a test environment (first in CH) for characterizing the performance and power of WiFi HaLow at EPFL
  - Define a test plan to characterize WiFi performance and power
  - Conduct measurements in and around EPFL and write a report
- **Type of work:** 50% System design, 25% Software, 25% measurements
- **Pre-requisits:** Interest in embedded hardware and IoT wireless on a system level (no specific algorithm know-how required)







Contact: andreas.burg@epfl.ch