Design and Development of a 1 MW Test Setup for Medium-Frequency Transformers

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Project Type: Bachelor Semester Project
Official Start Date: 16.02.2026
Submission of Final Report: June, 2026
Presentations at Group Meeting: Mid-term and Final Presentations (dates TBD)
Delivery of project results: Design files, simulation files, source code of software, and report.

Context, Background, and Motivation:

The Power Electronics Laboratory is currently involved in several research projects regarding the design of high-power **medium-frequency transformers** (**MFTs**) for **medium-voltage** (**MV**) **solid-state transformers** (**SSTs**). To validate the electromagnetic and thermal design, the electric machines must be tested in a condition that mimics the actual operation of the SST. In addition, the operation must be compatible with the laboratory infrastructure and its constraints. Therefore, to test a **1-MW MFT** that will be operating in an SST with fixed voltage gain (a.k.a., a resonant DC transformer, DCT), a test setup will be developed. The system uses the concept of power circulation: the nominal power is circulated through the controlled operation of a converter connected in a loop, while an external power supply (connected to the lab infrastructure) supplies the unavoidable electrical losses. This allows us to test the high-power MFT without putting excessive strain on the electrical grid of the EPFL campus that will hinder its stability. The peculiar aspect of this test setup is that the device under test (DUT, i.e., the MFT) has a non-unitary turn ratio of 3.3; this introduces the need for a step-down converter in the power-circulation loop.

Project Objectives:

Design and simulate the test setup for an MFT for a DCT stepping up 1 kV DC to 3.3 kV DC. Fig. 1 illustrates the concept of the system. The test setup is connected through a high-voltage diode to a power supply system that is present in the lab. The test setup is composed of an H-bridge inverter connected to a 1kV DC bus, a resonant capacitor, the MFT under test, a diode rectifier attached to a 3.3 kV DC-link, and a non-isolated step-down DC-DC converter; the latter allows for the controlled circulation of a 1-MW power in the test setup. Ultimately, the main tasks of the work are:

1. Understanding the operation of the different parts of the test setup.
2. Simulation of the converters and test setup as a whole, considering the main hardware and control aspects.
3. Design of the components of the test setup, including the sizing of the components and high-level thermal design.
4. Development and validation of a basic control software on an industrial-grade controller, also thanks to a real-time hardware-in-the-loop (RT-HIL) platform, both available in the lab.
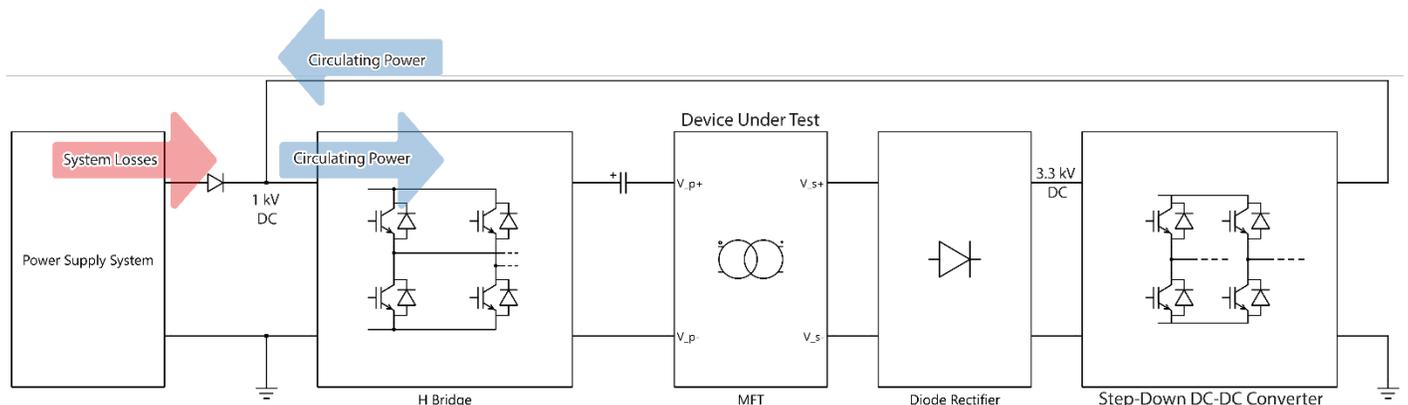

Figure 1. Diagram of the test setup, showing only the main elements of the power hardware.

Prerequisite knowledge:

1.   Basics of power electronic converters
2.   Basics of Plexim PLECS simulation software

Available equipment:

All the equipment required to fulfill the project's goals is available in the lab.

Methodology and foreseen steps of the project:

1.   Understanding the operation of a fixed-frequency LLC and preparing its PLECS simulation model
2.   Understanding the operation of the step-down DC-DC converter and preparing its PLECS simulation model
3.   Understanding the operation of the whole test setup and preparing its simulation
4.   Hardware design of the main elements of the test setup and validation through simulations
5.   Implementation of the offline simulation model on the RT-HIL system based on Plexim RT-Box.
6.   Implementing the basic operation of the test setup on an industrial-grade controller with code generation in MATLAB Simulink and testing it with the RT-HIL system

Student gains:

1.   Skills in the simulation of high-power converters
2.   Knowledge of the main design elements of a high-power MV converter
3.   Hands-on knowledge of the control concepts for high-power MV converters
4.   Hands-on knowledge of code generation on an industrial-grade controller
5.   Hands-on knowledge of testing control software with the RT-HIL approach

References:

Will be provided as needed.