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ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

Vertically Stacked Gate-All-Around Silicon Nanowire Field Effect Transistor Arrays

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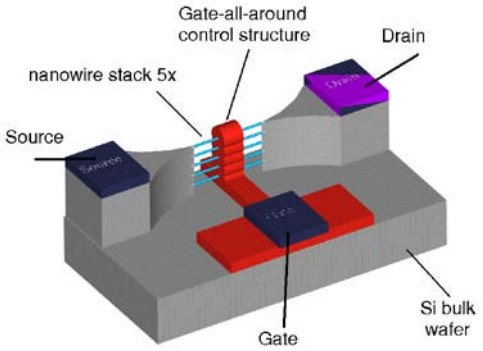
Presentation

Since the invention of integrated circuit technology, tremendous improvement in terms of performance and density have been achieved. In this sense, Dennard's rules of scaling have dominated the evolution of complementary metal oxide semiconductor design, fulfilling the dictation of Moore's law for more than 40 years. However, the last technology nodes do show additional problems for scaling, which relate to several issues, such as large static power consumption, short channel effects, drain induced barrier lowering, increased access resistance as well as more pronounced variability and reliability. Today's solid state research tries to counterbalance these effects by means of different approaches. On the one hand there is the introduction of novel channel materials, such as SiGe or GaAs, together with high-k dielectrics. On the other hand novel device concepts, such as multi-gate configurations with nanowire channels are studied.

Goal

This project targets the realization of novel architectures based on vertically stacked silicon nanowire (SiNW) arrays. The functionality of SiNW devices will be investigated by experimental characterization of as fabricated prototypes. The SiNW channel configuration concept is compatible with a wide range of solid-state devices, thus making possible to combine different circuit domains though the same SiNW technology. This increased versatility of vertically-stacked SiNWs will be addressed at circuit level, for architectures that would get the full advantage of the introduced functionalities.



Concept drawing of vertically stacked gate-all-around silicon nanowire field effect transistor.

Publication:

"Fabrication and Characterization of Vertically Stacked Gate-All-Around Si Nanowire FET Arrays", Davide Sacchetto, Haykel Ben-Jamaa, Yusuf Leblebici, Giovanni De Micheli, in ESSDERC '09