Synchronization and Signal Integrity in 3-D ICs

Contact person: **Hu Xu** (hu.xu@epfl.ch)

Keywords: *VLSI, 3-D ICs, clock distribution networks, process variations, signal integrity*

Presentation:

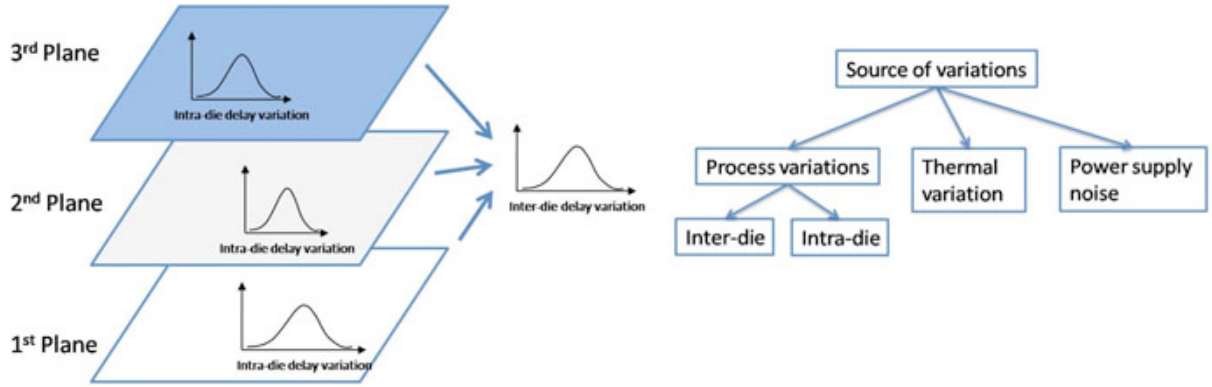
Three-dimensional integration is a novel design paradigm with great potential to fundamentally advance the computational functionality of modern integrated systems. Reliable communication is an important requirement for 3-D circuits. To implement reliable communication within these systems, synchronization issues and on-chip signal integrity of 3-D ICs are investigated.

In very deep sub-micrometer technologies, higher clock frequencies and the variability of the interconnect delay complicate the design of clock distribution networks. Different sources of variations are illustrated in figure. Considering the important synchronization issue, the reduced interconnect latency in 3-D ICs can be exploited to either relax the clock skew constraints or further increase the speed of a circuit. A careful compromise between the two approaches can, nevertheless, be a better solution to avoid timing failures while delivering higher (yet not the highest) performance as compared to a 2-D circuit. Since 3-D clock distribution networks span multiple planes, the variation of the clock delay and skew differs from 2-D circuits. The variations within one plane and among different planes simultaneously affect the performance of 3-D clock distribution networks, as illustrated in figure. To accurately model and reduce this variability is an important task for the design of robust 3-D clock distribution networks.

In addition, specific noise sources within integrated circuits have grown in importance in establishing signal integrity (SI) as a significant design objective. In 3-D integrated systems, the crosstalk in vertical direction and signal attenuation are two important factors affecting SI. The work in this area will include exploration of the efficiency of vertical interconnection approaches for 3-D ICs and the development of design techniques which efficiently mitigate the signal attenuation and minimize crosstalk noise.

Goal:

For the synchronization issue of 3-D ICs, we focus on the analysis of the variability and the performance of 3-D clock distribution networks. Our work is dedicated to the statistical modeling for 3-D interconnect delay and clock skew and the development of related CAD tools. The objective is to provide analysis models and design tools which contribute to the development of high-performance and reliable synchronization networks for 3-D ICs. For the on-chip signal integrity problem, our work aims at providing innovative interconnect design techniques and developing multi-objective buffer insertion techniques all for 3-D circuits.



Publications:

H. Xu, V. Pavlidis, and G. De Micheli, "Process-Induced Skew Variations for Scaled 2-D and 3-D ICs," IEEE/ACM 12th International Workshop on System Level Interconnect Prediction (SLIP), to appear.

H. Xu, V. Pavlidis, and G. De Micheli, "Repeater Insertion Techniques for 3-D Interconnects," Electronic Workshop Digest of DATE 2010 Workshop on 3D Integration, pp. 41-44, March, 2010.

H. Xu, V. Pavlidis, and G. De Micheli, "Repeater Insertion for Two-Terminal Nets in 3-D ICs," Proceedings of 4th International ICST Conference on Nano-Networks, pp. 141-150, Oct., 2009.