Design Methods and Tools for Application Specific Network-on-Chip Synthesis

Contact person: **Ciprian Seiculescu** (ciprian.seiculescu@epfl.ch)

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Presentation:

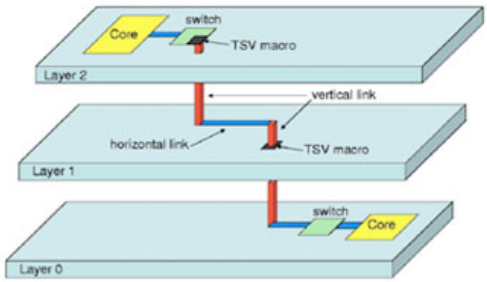
Three-dimensional integrated circuits are a promising approach to address the integration challenges faced by current Systems on Chips (SoCs). Designing an efficient Network on Chip (NoC) interconnect for a 3D SoC that not only meets the application performance constraints, but also the constraints imposed by the 3D technology, is a significant challenge.

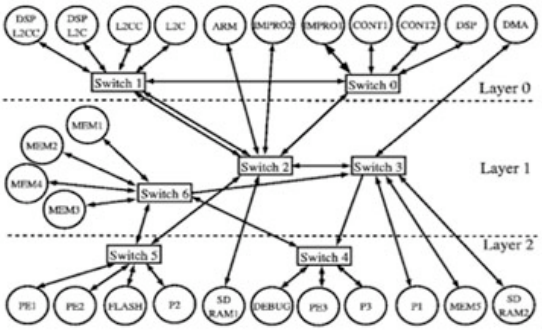
Some of the advantages of 3D integration are due to a smaller footprint of a 3D-IC than a comparative 2D implementation. The long horizontal wires in a 2D design can be replaced by shorter and more efficient vertical wires, leading to lower interconnect delay and power consumption. Wafer-to-wafer bonding technology, where the vertical interconnects are implemented by using Through Silicon Vias (TSVs), is one of the popular choices for 3D integration and it is the technology which is targeted in this project.

The interconnects for 3D have evolved from simple vertical links connecting buses in different 3D layers to a more scalable Network on Chip (NoC) solution. NoCs consists of switches and links and use circuit or packet switching to transfer data through the system. NoCs are a necessity for 3D chips, as they are modular, provide configurable parallelism and can control the number of TSVs required across layers. Building a custom application-specific NoC topology will be instrumental in pushing 3D NoC technology in industrial designs. However designing application specific NoC has been shown to be challenging in 2D systems as well and 3D integration poses some additional challenges.

Goal:

We look at different aspects of designing application specific NoCs. Our goals are to develop algorithms for the design automation of application specific NoC topology synthesis. We consider synthesis for 3D-ICs and in the presence of voltage islands. Other directions that we are considering is to provide QoS guarantees (hard Real-Time Latency bounds on latency) in best effort NoC, through the adequate construction of the topology and to tackle the problems related to memory controller sharing in NoCs (bottle-neck traffic to hot module).





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