

# **Network on Chip Emulation on FPGA**

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# **Presentation**

This project has as a first goal to provide a functional validation of the X-pipes Network-on-Chip (NoC) by synthesizing a X-pipes NoC on FPGA. We used a Virtex II Pro FPGA (2VP20) with 2 Million gates.

In addition to the functional validation, we used a hard-core processor (Power PC)

available on the FPGA to control an emulation platform. This emulation platform includes some components which inject traffic into the NoC and some components which collect the traffic and perform its analysis. Those components are fully controllable by the processor with an OPB (On-chip Peripheral Bus) interconnect thru which the processor can access some registers of those components. Thanks to this mixed Hw/Sw platform, a single design on the FPGA can emulate a NoC with various traffic patterns and can collect a wide range of statistics.

This novel approach of collecting statistics about on-chip interconnect is a way to acquire statistics about latency of packets, for instance, at very high speed. Indeed, our emulation platform runs four orders of magnitude faster than traditional simulators.

#### ECL H m o a **Monitor** a u n y r lte **Emulation** Platform d arr W t o OPB Control i l a to IB S r 0 Filter e 0 n Power PO Network Traffic Generator f to be IB 1 Emulated t C file w (Device a Traffic receptor under a Compiled y test) r e e Layer

## **Future Directions**

Using FPGA also gives us the opportunity to run real multimedia applications. As a first step, we will include in our design some processors, which run benchmarks applications. It will provide a multi-processor emulator, which uses Xpipes NoC. As a second step, we will include in the emulation platform the possibility to plug I/Os like a keyboard or a video output. Using

those I/Os, we will be able to run multimedia application avoiding the use of benchmarks.



### **Publications**

N.Genko, D.Atienza, G. De Micheli et al. "A Complete Network-on-Chip Emulation Framework" Proc. of IEEE DATE 2005 p246-251.

N.Genko, D.Atienza, G. De Micheli et al "A Novel Approach for Network-on-Chip Emulation" Proc. of ISCAS 2005.

N.Genko, D.Atienza, G. De Micheli et al "NoC Emulation on FPGA: HW/SW Synergy for NoC Features Exploration" Proc. of ParCo 2005.

#### Links:

Xpipes Network-on-Chip: http://www-micrel.deis.unibo.it/sitonew/research/index.html#NoC