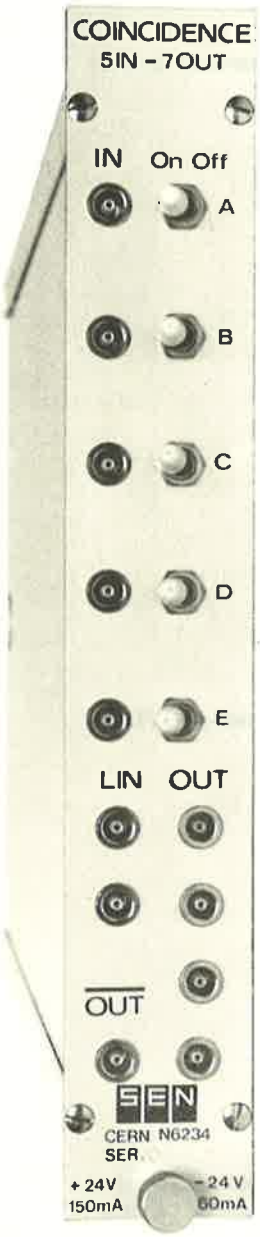
SEN
ELECTRONIQUE



COINCIDENCE, 5 IN-7 OUT CERN N 6234

Purpose

Outputs are produced when coinciding signals are applied to the activated inputs.

Logic pulses are required for coincidence operation, complementary logic pulses for anti-coincidence operation.

General Features

The coincidence, which is built in a single-width NIM-module, has five inputs. Each of them can be activated by front-panel switches.

Two linear or overlap outputs and five standardized outputs (4 OUT + 1 $\overline{\text{OUT}}$) are provided.

The amplitude of the output signals conforms to the NIM standard for fast logic levels.

The width of the linear outputs is equal to the input width or overlap.

The width of the standardized outputs is fixed.

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1211 GENÈVE 13 - SUISSE/SWITZERLAND - 31, Av. Ernest-Pictet - Tél. (022) 44 29 40 - Télex 23359 - Câbles SENELECTRON

SPECIFICATIONS

INPUT

Number	5
Impedance	50 ohms
Reflections	In "On" State : ⩽ 20%, (capacitive) In "Off" State : ⩽ 15%, (inductive)
Voltage	Logic, – 800 mV for coincidence. Complementary logic for anti-coincidence.
Width	Minimum width or overlap (at minimum input "I" level = – 12 mA) to produce outputs. LIN : For singles ⩽ 2.0 ns. For 5-fold ⩽ 2.0 ns. OUT and $\overline{OUT}$: For singles ⩽ 1.5 ns. For 5-fold ⩽ 1.25 ns.
Maximum Rate	Determined by output specifications.

LIN OUTPUT (Overlap Output)

Number	2 logic
Impedance	High, current source, unused outputs need not be terminated.
Rise and Fall Time	T_{01} ⩽ 1.8 ns, T_{10} ⩽ 2.0 ns.
Width	Equal to input width or overlap at min input "I" level (– 12 mA) + ⩽ 1.0 ns for singles, – ⩽ 1.0 ns for 5-fold
Maximum Rate	⩾ 200 Mc/s
Propagation Delay	6.2 ± 0,75 ns (between min. input and output "I") for singles. For 5-fold it decreases by ⩽ 0,5 ns.
Feedthrough	for n–1, ⩽ ± 15 mV

OUTPUT and $\overline{OUTPUT}$ (Standardized Output)

Number	4 logic 1 complementary
Impedance	High, current source, unused outputs need not be terminated.
Rise and Fall Time	Logic : T_{01} ⩽ 1.5 ns, T_{10} ⩽ 2.2 ns Complementary : T_{10} ⩽ 2.0 ns, T_{01} ⩽ 2.2 ns.
Width	Logic, 9.0 ± 1 ns at min input "I" level (– 12 mA). Complementary, 9.0 ± 1 ns at max input "0" level (– 4 mA).
Maximum Rate	Up to a frequency of ⩾ 70 Mc/s the output consists of pulses, i.e. the level between pulses comes down inside the "0" output band. At a frequency of ⩾ 100 Mc/s the output becomes DC. When this rate is exceeded the output turns into pulses again, but counts will be lost.
Propagation Delay	9.5 ns ± 1.2 ns (between min. input and output "I"), for singles. For 5-fold it decreases by ⩽ 0.5 ns.

POWER CONSUMPTION – 24 V ⩽ 270 mA + 24 V ⩽ 155 mA

N.B. 1) Rise (T_{01}) and fall-times (T_{10}) are measured between maximum output "0" (– 100 mV) and minimum output "I" (–700 mV).

2) All parameters have been determined with input signals having rise and fall times of 0.7 ns.

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INSTRUCTION MANUAL

COINCIDENCE, 5 IN, 7 OUT

Valid for serial No : 500 ...

Approved : Si

CERN Type N 6234

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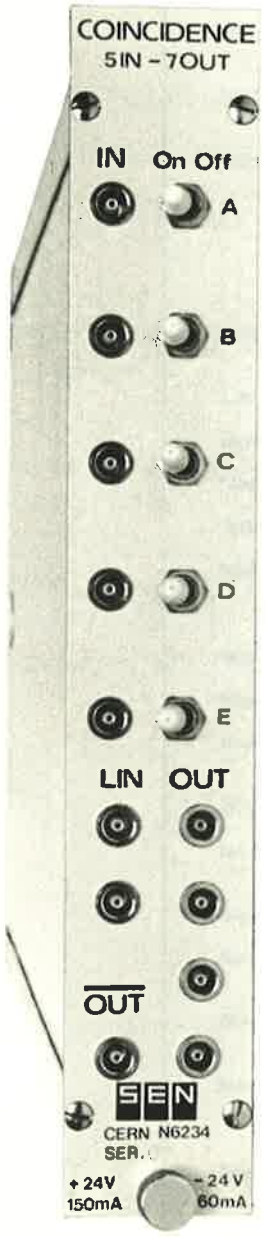


Purpose

Outputs are produced when coinciding signals are applied to the activated inputs.

Logic pulses are required for coincidence operation, complementary logic pulses for anti-coincidence operation.

General Features

The coincidence, which is built in a single-width NIM-module, has five inputs. Each of them can be activated by front-panel switches.

Two linear or overlap outputs and five standardized outputs (4 OUT + 1 $\overline{\text{OUT}}$) are provided.

The amplitude of the output signals conforms to the NIM standard for fast logic levels.

The width of the linear outputs is equal to the input width or overlap.

The width of the standardized outputs is fixed.

Brief Circuit Description

Coincident signals at the activated inputs trigger the tunnel diode D 31. This tunnel diode stays turned on as long as the input signals overlap. The tunnel diode signal is amplified (T 1, T 15, T 16) and provides the linear or overlap output (T 17, T 18).

Standardized outputs: Tunnel diode signal (D31) is amplified by T1 and differentiated by T2, R31, C4. The differentiated signal triggers D32 and D35. These tunnel diodes are reset by the reset transistor T4. The pulse width of the standardized output is the sum of the direct pulse (T6) and the delayed pulse (T7), which compensates the deadtime of the direct pulse to get an output duty cycle of 100%.

SPECIFICATIONS

INPUT	
Number	5
Impedance	50 ohms
Reflections	In "On" State : ⩽ 20%, (capacitive) In "Off" State : ⩽ 15%, (inductive)
Voltage	Logic, – 800 mV for coincidence. Complementary logic for anti-coincidence.
Width	Minimum width or overlap (at minimum input "I" level = – 12 mA) to produce outputs. LIN : For singles ⩽ 2.0 ns. For 5-fold ⩽ 2.0 ns. OUT and $\overline{\text{OUT}}$: For singles ⩽ 1.5 ns. For 5-fold ⩽ 1.25 ns.
Maximum Rate	Determined by output specifications.
LIN OUTPUT	(Overlap Output)
Number	2 logic
Impedance	High, current source, unused outputs need not be terminated.
Rise and Fall Time	T_{01} ⩽ 1.8 ns, T_{10} ⩽ 2.0 ns.
Width	Equal to input width or overlap at min input "I" level (– 12 mA) + ⩽ 1.0 ns for singles, – ⩽ 1.0 ns for 5-fold
Maximum Rate	⩾ 200 Mc/s
Propagation Delay	6.2 ± 0,75 ns (between min. input and output "I") for singles. For 5-fold it decreases by ⩽ 0,5 ns.
Feedthrough	for n–1, ⩽ ± 15 mV
OUTPUT and $\overline{\text{OUTPUT}}$	(Standardized Output)
Number	4 logic 1 complementary
Impedance	High, current source, unused outputs need not be terminated.
Rise and Fall Time	Logic : T_{01} ⩽ 1.5 ns, T_{10} ⩽ 2.2 ns Complementary : T_{10} ⩽ 2.0 ns, T_{01} ⩽ 2.2 ns.
Width	Logic, 9.0 ± 1 ns at min input "I" level (– 12 mA). Complementary, 9.0 ± 1 ns at max input "0" level (– 4 mA).
Maximum Rate	Up to a frequency of ⩾ 70 Mc/s the output consists of pulses, i.e. the level between pulses comes down inside the "0" output band. At a frequency of ⩾ 100 Mc/s the output becomes DC. When this rate is exceeded the output turns into pulses again, but counts will be lost.
Propagation Delay	9.5 ns ± 1.2 ns (between min. input and output "I"), for singles. For 5-fold it decreases by ⩽ 0.5 ns.
POWER CONSUMPTION	– 24 V ⩽ 270 mA + 24 V ⩽ 155 mA

N.B. 1) Rise (T_{01}) and fall-times (T_{10}) are measured between maximum output "0" (– 100 mV) and minimum output "I" (–700 mV).

2) All parameters have been determined with input signals having rise and fall times of 0.7 ns.

ADJUSTMENT AND TEST PROCEDURE

A) INSTRUMENTS REQUIRED

1) Power Supply + 24 V (min 160 mA) – 24 V (min 280 mA).
2) Sampling oscilloscope Tektronix Type 561 or equivalent.
3) EH pulse generator Model 122 or equivalent.
4) 6 way split (resistive).
5) Coincidence Test Unit (Fig. 1)
6) Shaper, type N 2618 CERN NP or equivalent.
7) Delay 2.5 – 66 nsec, Type N 9053 CERN NP or equivalent.
8) Vacuum voltmeter – HP 412 A or equivalent.

B) ADJUSTMENT PROCEDURE

1) Switch on one channel and turn P1, P2, P3, P4 fully anticlockwise.
2) Outputs must be matched, nothing must be connected to input.
3) Connect the supply voltages, switch on power supply. The consumption must be 145 ± 15 mA from + 24 V and 255 ± 20 mA from – 24 V. Check zener voltages: ± 6.0 ± 0.2 V; ± 12.0 ± 0.4 V – 9.1 ± 0.6V and zener D38 – 6.0 ± 0.2 V.
4) D.C. Adjustment
   a) D.C. conditions at inputs. Leave one channel "ON", measure voltage on t.d. D31 to be – 10 to – 25 mV. Measure now for each channel in "ON" state, while all others are "OFF" the D.C. at its input, which should be +10 to – 45 mV.
   b) Linear out (LIN). Vacuum voltmeter: 1 volt range and one terminal at – 6V. Measure the voltage across D60, D61, points Y and Z on circuit diagram, choose between transistors T 17 and T 18 that one connected to the diode with the highest voltage drop just measured above. Bias its base (TP1) 500 mV forward by turning P1, if a D.C. > 1 mV is measured across its matched output, this bias has to be reduced to 450 mV. The amount by which the base emitter voltage of the other transistor is less, must not exceed 170 mV.
   c) Standard output (OUT). Connect the voltmeter between TP 4 (collector T6) and – 9.1V, range + 1 V. Must measure about 400 mV. Turn P4 clockwise which initially should not affect the meter reading, till this meter reading has increased by 15 mV. Turn P3 clockwise, while keeping voltmeter reading about constant by turning P4, till the indication jumps at about 1 V. Leave P 3 exactly at the point where the meter jumped. Connect now the voltmeter between ground and TP3, range 30 V, or, if possible 10 V, turn P3 to reduce reading by 3.0 V. Connect again the voltmeter to – 9.1 V and TP4, range of 1 V, and turn P4 anticlockwise till reading becomes constant, then from here turn P4 clockwise till reading has increased by 15 mV.
5) Pulse Adjustment – Input: 800 mV, 15 ns at 600 mV, repetition rate about 10 Kc/s.
   a) Connect a 6 way split to the output of the pulse generator (which has been carefully adjusted to have zero off-set voltage) via 1 ns cable.
   b) Connect 5 outputs of the 6 way split to the module via 1 ns cables and the 6th to scope (channel B). Connect the sampling scope (5 ns/div, 200 mV/div) to LIN (linear out)

and switch on all inputs; a 15 ns – 800 mV signal must be present. Repeat this test on the other LIN. Disconnect sequentially each input, one at a time: the LIN signal must disappear each time.

c) Connect now scope to an OUT (standard output) and the voltmeter to TP2 and ground. Turn P2 clockwise until an output signal appears, note the voltmeter reading (1), turn further P2 until double pulses appear (vary the length of input pulse 5 – 15 ns in order to find the most sensitive point for this double pulsing), note also this reading (2), then reduce meter reading by 1.0 V by turning P2 (3). Determine voltage difference between positions (1) and (3) to be ≥1.0 V.

d) Check if all outputs have an acceptable shape and are affected or not by the presence of the matching pieces in the following way:

LIN : Connect a LIN to scope, connect and remove the matching piece of the other LIN; the shape of signal must stay nearly constant and the length must not vary more than 0.2 ns.

Repeat this check for the other LIN.

The overshoot must be less than 12%, if the signal seems too slow (see C/9b) put a ferrite core (Philips type 3122.104.91061) into L2.

OUT and $\overline{\text{OUT}}$: Connect the scope to one OUT, connect and remove matching pieces of the $\overline{\text{OUT}}$ and of the other three OUT's: the shape of the signal must stay nearly constant and the length must not vary more than 0.2 ns.

Repeat this check for one of the other three OUT's.

6) D.C. Voltage Finalities – Repeat measurement 4/b. Disconnect all input connections, leave "ON" all inputs and check all the voltages indicated in the check list with reference to the circuit diagram. Make the calculations. Check if all values recorded are within the indicated ranges.

Check List

V_l	V_m	V_r	V_q	
+240 ± 20	-200 ± 20	20 to -20	300 to 600	(mV)

DC – Voltages referred to -6V in point p

V_n	V_o	$V_o - V_n$	
nom. val. -300	nom. val. -600	-150 to -450	(mV)

DC – Voltages referred to 9.1V

V_s nom. val. -300	V_t nom. val. -600	V_u nom. val. -600	V_v nom. val. -600	V_w nom. val. -600	(mV)
	$V_t - V_s$ -150 to -450	$V_u - V_s$ -150 to -450	$V_v - V_s$ -150 to -450	$V_w - V_s$ -150 to -450	(mV)

C) PULSE TESTS

1) Make arrangement as shown on fig. 1.

2) All inputs in "OFF" state:
Adjust the E.H. generator for 800 mV, 5 ns at 600 mV pulses measured on channel A of the scope. The shape of this signal must be correct, otherwise something is wrong at the inputs of the coincidence.

3) Single input:
Disconnect 4 of the 5 input cables and match these. Feed a signal of 800 mV sequentially to every single input set at "ON" state. Both signals on sampling scope must be correct. Repeat this operation with a signal of 550 mV and verify that: LIN remain ≥ 700 mV and OUT are present.

4) Double, triple, four fold coincidence: Scope (channel B) still connected to one OUT. Make double, triple, four fold coincidence with 800 mV signals. Then check the coincidence action (double, triple, four fold) by adding and subtracting 6 ns in one input by using the delay box; the OUT signal must disappear due to this delay addition or subtraction.

5) 5 fold coincidence: Do the same delay test as described above. Reduce the input signal to 600 mV, check if LIN signal stays ≥ 700 mV for the 600 mV input.

6) Anticoincidence: Modify the test set-up as shown by dotted lines on drawing. Feed in 4 signals of 800 mV, 3,5 ns at 600 mV. With scope connected to one OUT, check the presence of an output signal. When channel E is switched "ON", signal should disappear and reappear when 6,5 ns of delay cable is added and subtracted on delay box. Now connect sequentially the shaper to channels A, B, C, D and repeat the above indicated checks.

7) Breakthrough of 4 coincident input signals when 5 inputs are "ON". All 5 inputs "ON", channel B of scope at LIN; first feed 5 inputs into the module and check if output signal is properly there. Then sequentially disconnect one input and match its cable and measure the signal at the scope. This feed-through should be ≤ 15 mV.

8) Minimum input width to produce minimum "1" (– 14 mA) at LIN. Leave channel B of scope at LIN, using arrangement as noted under C/3. Feed sequentially 800 mV, T = 2.5 ns at – 600 mV pulses to all inputs. Check if LIN signal reaches always "1" band (≥ 700 mV) and if OUT signals are present.

9) Amplitude and shape of output signals: *
Feed in single 800 mV, 10ns pulses. Outputs should be as follows:
a) OUT: Width 9.0 ± 1.0 ns at 600 mV (check all).
Amplitude: 750 – 900 mV (→15 – 18 mA)
T01 ≤ 1.5 ns, T10 ≤ 2.2 ns.

$\overline{\text{OUT}}$: Width 9.0 ± 1.0 ns at 4 mA.
Risetime: T10 ≤ 2.0 ns, fall time:
T01 ≤ 2.2 ns.

If these values cannot be obtained, put a fer-

rite core (Philips type 3122.104.91061) into L 1.

b) LIN: T01 ≤ 1.8 ns, T10 ≤ 2.0 ns
Width at 700 mV level equal to input width (→ at 12 mA level) + ≤ 1.0 ns.

10) Rate Test: Connect "single" input 800 mV, T = 5 ns at 600 mV, repetition 100 Mc/s. Check if all LIN reach the nominal output "1" band (800 mV) and level between pulses stays at O volt. OUT should reach the nominal output "1" (800 mV) as a D.C. level and the $\overline{OUT}$ should stay at 0 volt D.C.

* Rise times (T01) and fall times (T10) are measured between maximum output "0" (-100 mV) and minimum output "1" (-700 mV).

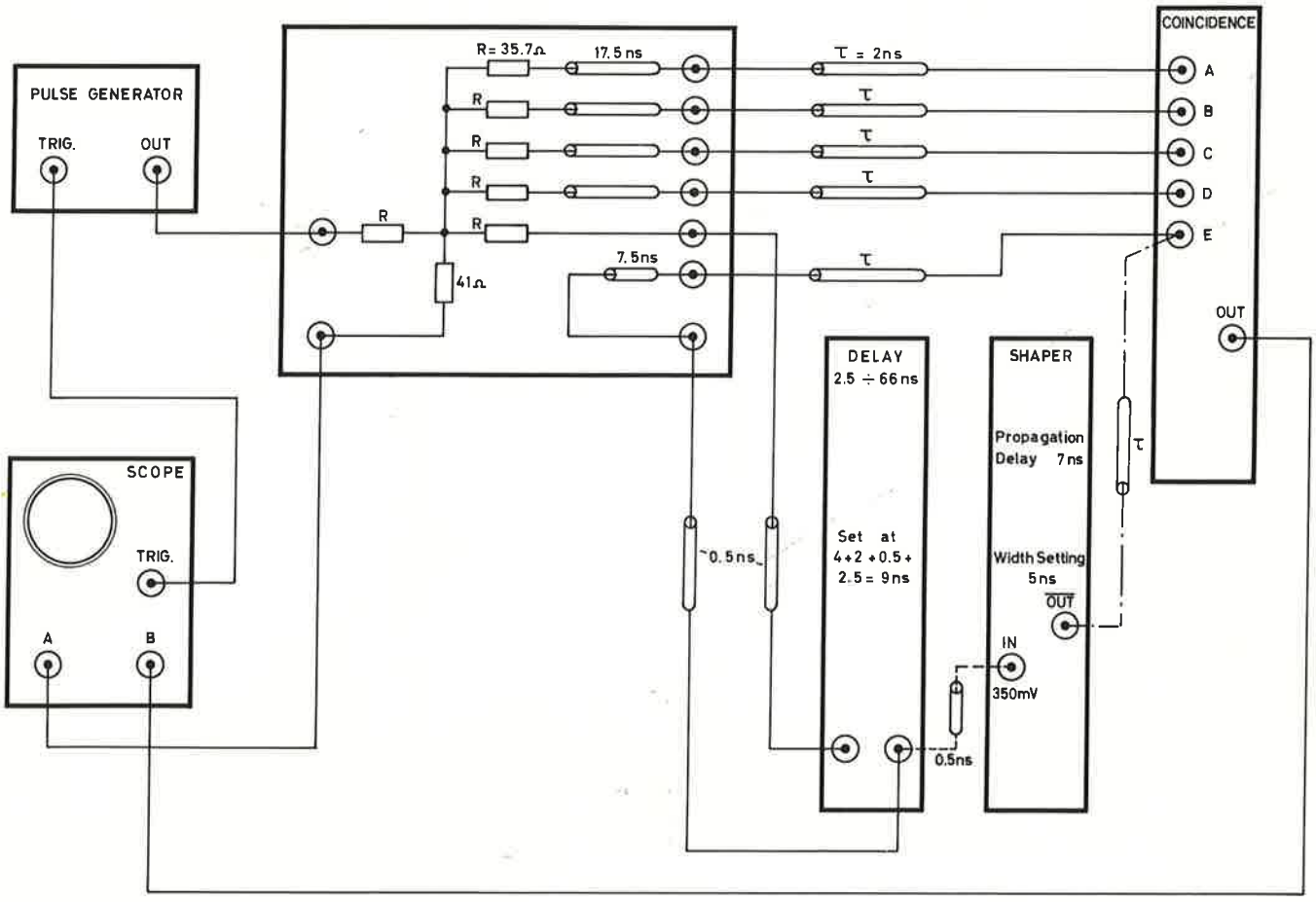


Figure 1

PART LIST

Coincidence, 5Inputs, 7Outputs

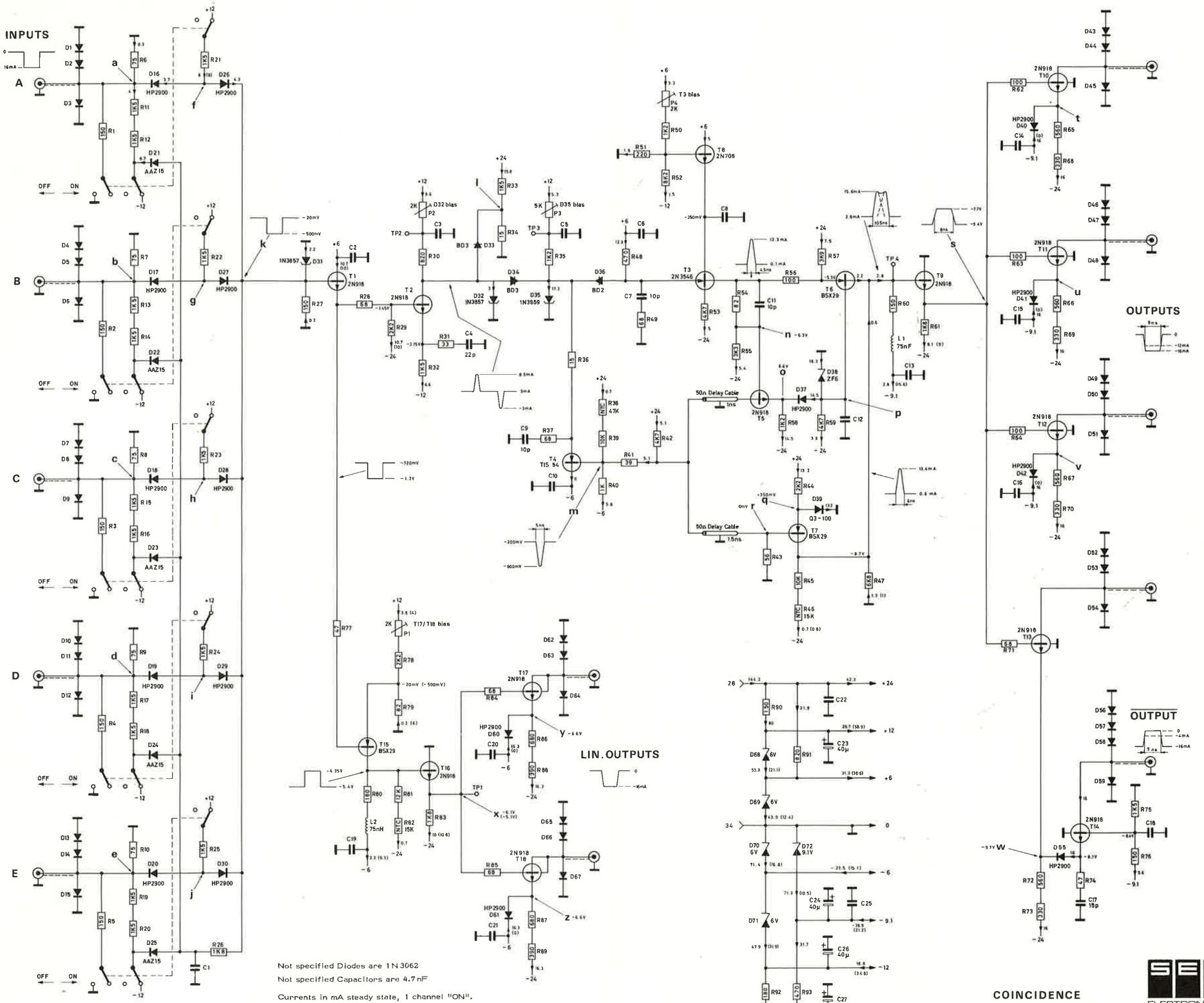
	Component		Value	Manuf.
R 1 - 5	2%	1/4 W	150	Metallux
R 6 - 10	2%	1/8 W	75	"
R11 - 20	2%	1/4 W	1K5	"
R21 - 25	"	"	1K5	"
R26	"	"	1K8	"
R27	5%	"	150	AB
R28	"	"	68	"
R29	"	"	2K2	"
R30	"	"	820	"
R31	"	"	33	"
R32	"	"	1K5	"
R33	"	1/2 W	1K5	"
R34	"	1/4 W	15	"
R35	"	"	1K2	"
R36	"	"	15	"
R37	"	"	68	"
R38	20% 0,6 W	NTC	47K	Phil.
R39	5%	1/4 W	10K	AB
R40	"	"	1K	"
R41	"	"	39	"
R42	"	"	4K7	"
R43	"	"	56	"
R44	"	"	2K2	"
R45	"	"	10K	"
R46	20% 0,6 W	NTC	15K	Phil.
R47	5%	1/4 W	6K8	AB
R48	"	"	470	"
R49	"	"	68	"
R50	"	"	1K2	"
R51	"	"	220	"
R52	"	"	8K2	"
R53	"	"	4K7	"
R54	"	"	82	"
R55	"	"	3K3	"
R56	"	"	100	"
R57	"	"	3K9	"
R58	"	"	1K2	"
R59	"	"	4K7	"
R60	"	"	150	"
R61	"	"	1K8	"
R62 - 64	"	"	100	"
R65 - 67	"	"	560	"
R68 - 70	"	"	330	"
R71	"	"	68	"
R72	"	"	560	"
R73	"	"	330	"
R74	"	"	47	"
R75	"	"	1K5	"
R76	"	"	150	"
R77	"	"	47	"
R78	"	"	2K2	"
R79	"	"	82	"
R80	"	"	180	"
R81	"	"	12K	"
R82	20% 0,6 W	NTC	15K	Phil.
R83	5%	1/4 W	1K8	AB
R84 - 85	"	"	68	"
R86 - 87	"	"	680	"
R88 - 89	"	"	390	"
R90	"	1,5 W	150	Painton
R91	"	1/2 W	820	AB
R92	"	1,5 W	180	Painton
R93	"	1 W	470	AB
P1	20% 3/4 W	Helitrim	2K	Beckman
P2	" "	"	2K	"
P3	" "	"	5K	"
P4	" "	"	2K	"
C1	Ceram.		4,7n	LCC
C2	"		4,7n	"
C3	"		4,7n	"
C4	"	mini.	22p	Phil.

	Component		Value	Manuf.
C5	Ceram.		4,7n	LCC
C6	"		4,7n	"
C7	"	mini.	10p	Phil.
C8	"		4,7n	LCC
C9	"	mini.	10p	Phil.
C10	"		4,7n	LCC
C11	"	mini.	10p	Phil.
C12	"		4,7n	LCC
C13	"		4,7n	"
C14 - 16	"		4,7n	"
C17	"	mini.	15p	Phil.
C18	"		4,7n	LCC
C19	"		4,7n	"
C20 - 21	"		4,7n	"
C22	"		4,7n	"
C23	Electrolyt		40μ - 16V	Phil.
C24	"		40μ - 16V	"
C25	Ceram.		4,7n	LCC
C26	Electrolyt		40μ - 16V	Phil.
C27	Ceram.		4,7n	LCC
L 1 - 2	2 turns of 0.6 mm wire on a M 6 x 6 Plexiglas Former			
D 1 - 15	Si Diode		1N3062	Cosem
D16 - 20*	Si Hot car.		HP2900	HP
D21 - 25	Si Diode		AAZ15	Phil.
D26 - 30*	Si Hot car.		HP2900	HP
D31	Tunnel		1N3857	RCA
D32	Tunnel		1N3857	"
D33	Ge Backward		BD3	GE
D34	Ge Backward		BD3	"
D35	Tunnel		1N3859	RCA
D36	Ge Backward		BD2	GE
D37 **	Si Hot car.		HP2900	HP
D38	Zener		ZF6	ITT
D39	Ge Diode		Q3 - 100	Int. D. C.
D40 - 42**	Si Hot car.		HP2900	HP
D43 - 54	Si Diode		1N3062	Cosem
D55 **	Si Hot car.		HP2900	HP
D56 - 59	Si Diode		1N3062	Cosem
D60 - 61**	Si Hot car.		HP2900	HP
D62 - 67	Si Diode		1N3062	Cosem
D68 - 71	Zener		ZM6 ±3%	ITT
D72	Zener		ZD9, 1±5%	ITT
T 1	NPN Si		2N918	Cosem
T 2	NPN Si		2N918	"
T 3 ***	PNP Si		2N3546	Mot.
T 4	PNP Si		TIS 54	TI
T 5	NPN Si		2N918	Cosem
T 6	PNP Si		BSx29	SGS
T 7	PNP Si		BSx29	"
T 8	NPN Si		2N708	"
T 9	NPN Si		2N918	Cosem
T 10-13	NPN Si		2N918	Phil.
T 14	NPN Si		2N918	"
T15	PNP Si		BSX29	SGS
T16	NPN Si		2N918	Cosem
T17 - 18	NPN Si		2N918	Phil.

* D16 coupled to D26, voltage drop difference at 4mA ≤ 20mV. The same is true for D17/D27, D18/D28, D19/D29, D20/D30.

** Selected, voltage drop at 16mA 525 - 675mV.

*** Or BSX29, SGS, with $f_T \geq 600$MHz at V_{CE} = 5V, I_E = 6mA.



Not specified Diodes are 1N3062

Not specified Capacitors are 4.7nF

Currents in mA steady state, 1 channel "ON". Values in brackets when 5 ch. "ON" with signal present on all inputs.