SEN
ELECTRONIQUE

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INSTRUCTION MANUAL

FE 270 OR, 6 INPUTS

Valid for serial No : 500...

Approved : Si

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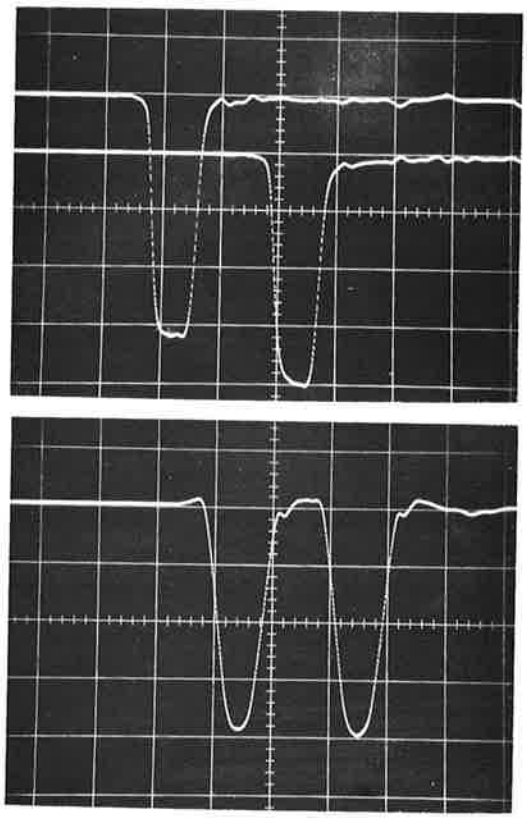
Input and Output Pulse Shapes

(5 ns/div., 200 mV/div.)



— Input A

— Input B (Base line of scope displaced)

— Output

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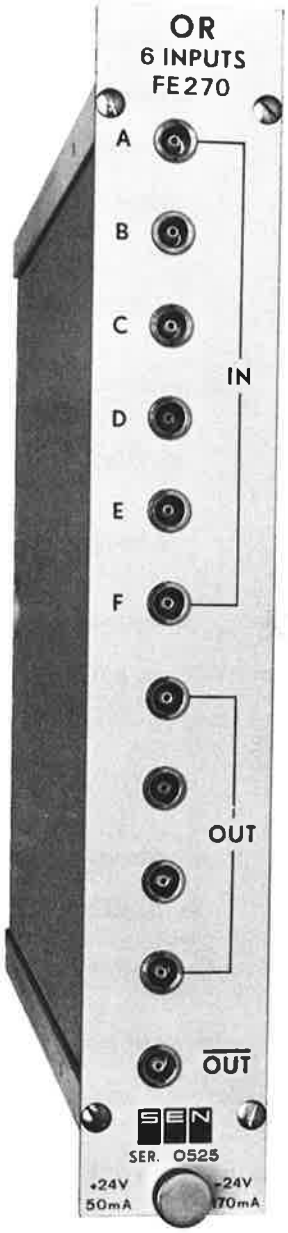


Purpose

Outputs are produced if any number out of the six inputs is present.

Other applications are:
AND Gate (Coincidence with complementary logic signals)

Pulse Generator (by connecting the complementary output via a coaxial cable to an Input)

Set-Reset Bistable (by combining two OR-modules)

General Features

The Or, which is built in a single-width NIM-module, is entirely DC-coupled.

Each of the four logic outputs and the complementary output has its own output transistor. This gives good decoupling between the outputs, and the unused outputs need not be terminated.
The circuit contains no trigger elements, has no hysteresis and no deadtime.

Brief Circuit Description

The Or-function is performed by the diodes D19 - D24. The shape of the signal at the emitter of transistor T7 is therefore the same for one or more input signals. Transistors T7 - T10 amplify this signal. The output stages (T11 - T15) normalize the amplitude of the output signals.

Reference

"A Six - Input Or - Gate", F. Nanni and H. Verveij, CERN Report NP 68 - 39.

Specifications

INPUT

Number	6
Resistance	50 ohms ± 2%
Reflections	⩽ 12.5% for a step with tr = 1.0 ns. Capacitive.
Voltage	Typically − 800 mV, (logical "I"), tr = tf ⩽ 2,5 ns Threshold ⩾ |−200| mV, for which output ⩽ |−100| mV (output "0") Minimum to produce minimum logical "I" (= − 14 mA at output) : − 550 mV DC
Width	Shortest pulse to produce full output 2.5 ns at 600 mV level of a − 800 mV pulse Maximum = DC
Maximum Rate	Typically 150 Mc/s

OUTPUT

Number	4 logic 1 complementary (NOR)	
Impedance	High, current source. Unused outputs need not be terminated.	
Rise and Fall Time	Logic	tr ⩽ 2,0 ns tf ⩽ 2,2 ns
	Complementary	tr ⩽ 2,2 ns tf ⩽ 2,2 ns
Overshoot	⩽ 15% for logic	
Undershoot	⩽ 18% for complementary	
Width	Equal to width (F.W.H.M.) of input signal + 1,3 ns − 0,7 ns Temperature coefficient ⩽ + 30 ps/°C, for input with tr = tf ⩽ 2,0 ns	
Maximum Rate	Equal to maximum input rate	
Propagation Delay	6,5 ns ± 0,75 ns (measured at min "I" level)	

POWER CONSUMPTION +24V ⩽ 50 mA −24V ⩽ 170 mA

N.B. Rise times (tr) and fall times (tf) are measured between maximum output "O" band (−100 mV) and minimum output "I" band (−700 mV).

Specifications subject to minor changes without notice.

Other Applications

OR - Gates are very useful since they do not only offer the OR-function but also several other application modes. Therefore, the OR-mdoule may also be used as a Coincidence, a Generator or as a Set-Reset Bistable.

A. Coincidence: By applying complementary logic pulses instead of logic pulses to the input, the normally logic output (OUT) will deliver complementary logic pulses whereas the normally complementary logic output ($\overline{OUT}$) will give logic pulses. In Boolean terms:

IN	OUT	$\overline{OUT}$	OR-Operation, Logic Inputs
⊓⊔	⊓⊔		OUT=OR = A+B+C+D+E+F
		⊔⊓	$\overline{OUT}$=NOR= $\overline{A+B+C+D+E+F}$
			Coincidence (AND-)Operation, complementary logic Inputs
⊔⊓	⊔⊓		OUT=AND = $\bar{A}\,\bar{B}\,\bar{C}\,\bar{D}\,\bar{E}\,\bar{F}$
		⊓⊔	$\overline{OUT}$=NAND= $\overline{\bar{A}\,\bar{B}\,\bar{C}\,\bar{D}\,\bar{E}\,\bar{F}}$

This mode of operation is very attractive because the channel becomes active only when the input cable is connected. Therefore, no input switches are required for disabling or enabling inputs.
The anti-coincidence function can be obtained via one or more channels by feeding logic signals to these channels. Minimum input overlap (at - 200 mV level) to produce a minimum "1" (- 700 mV) at the output is 2.5 ns.

B. Pulse Generator: The unit can be transformed into a pulse generator by connecting the complementary output ($\overline{OUT}$) via a coaxial cable to an input. Then the logic outputs (OUT) deliver recurrent pulses with 50 % duty cycle. The pulse frequency is equal to

$$f = \frac{1}{2} \cdot \frac{1}{\text{Propagation delay + External cable delay}}$$

$$= \frac{1}{(13 \pm 1.5)\ \text{ns} + 2\ \text{External cable delay}}$$

and the pulse width

$$T = (6 \pm 0.75)\text{ns} + \text{External cable delay}$$

The maximum obtainable frequency is ~70 Mc/s and the minimum pulse width ~7 ns.

The pulse generator can be gated off by connecting a logic signal to one of the remaining inputs.

C. Set-Reset Bistable: Two units can form a Set-Reset Bistable. This is accomplished by connecting the complementary output ($\overline{OUT}$) of each unit to the input of the other. A logic pulse to the input of either unit will cause a change of state.

Or

Adjustment Procedure

Instruments Required

1) Power Supply ± 24 V, min. 200 mA
2) 6 way split
3) E.H. pulse generator, model 122
4) Sampling oscilloscope, Tektronix 661 or equivalent
5) Voltmeter, HP 412 A or equivalent

Adjustment Procedure

1) Put potentiometer P1 at maximum (clockwise).
2) Outputs must be matched, nothing must be connected to input.
3) Connect the supply voltages. Switch on power supply. The consumption must be 170 ± 10 mA from -24 V and 42 ± 5 mA from +24 V. Check zener voltages: -6 ± 0.2 V; -12 ± 0.4 V.
4) D.C. Adjustment. Voltmeter in -1 V range, leaving meter at -6 V, put ground terminal at -6 V. Measure the voltage of T 14 at emitter (TPb). Adjust base (TPa) emitter bias of T 14 to 300 mV forward by turning potentiometer P1 and measure if the VBE of T11, T12, T13 are 200 ÷ 450 mV, by measuring the voltages in TP c, d, e. See now, if any DC is present at the matched logic outputs; a value up to 0,5 mV is acceptable.
5) Measure voltage across R25 between TPn and -12 V. It should be 1.1 ÷ 1.3 V.
6) Check voltages across D19, D20, D21, D22, D23, D24 by measuring the emitter voltage of T7, TPf and emitters T1, T2, T3, T4, T5, T6, TP g, h, j, k, l, m. The forward voltage across these diodes must be -80 mV ÷ + 20 mV. Nominal value -30 mV.

Pulse Tests

1) Inputs: Connect sampling scope to an output and feed a 800 mV, T = 20 ns pulse from generator to every input sequentially. A 800 mV output should occur which is virtually independent of the chosen input.

2) Outputs: Leave one input connected and check if all outputs are present with an acceptable shape.

3) Output amplitude, overshoot and undershoot: Input conditions as above. Measure if all outputs are 15 ÷ 17 mA.
   Overshoot $\leqslant$ 15% for logic,
   undershoot $\leqslant$ 18% for complementary.

4) Minimum input: Reduce single input signal to 550 mV. All logic outputs must reach the output "1" band ($\geqslant$ 700 mV), and the complementary output the output "0" band ($\leqslant$ 100 mV), (figure 1). Try all inputs sequentially leaving scope connected to smallest output.

5) Threshold: Apply pulse of 200 mV, T = 20 ns simultaneously to all inputs, all outputs must remain $\leqslant$ |20| mV (spikes). See if any signal due to instability is present at outputs, if so, take off C7 and check again.

6) Output rise and fall time: Input single 800 mV, T = 20 ns; tr must be $\leqslant$ 2,0 ns, tf $\leqslant$ 2,2 ns for all outputs.

7) Output width: Input as above but T = 10 ns. Output width must be equal to input width (F.W.H.M) 10,3 + 1 ns for all outputs.

8) Minimum input width, to produce minimum "1" (- 14 mA) at output: Feed in a single 800 mV, T = 2,5 ns at - 12 mA, check if all logic outputs reach the output "1" band ($\geqslant$ 700 mV) and the complementary output the output "0" band ($\leqslant$ 100 mV).

9) Rate test: Connect "single" input pulses from E.H. pulser, 800 mV, T = 2,5 ns at - 12 mA, 150 Mc/s. Check if all logic output pulses reach the output "1" band ($\geqslant$ 700 mV) and level between pulses stays within the output "0" band ($\leqslant$ 100 mV). Complementary pulses should reach the output "0" band and level between pulses stays within the output "1" band ($\geqslant$ 700 mV).

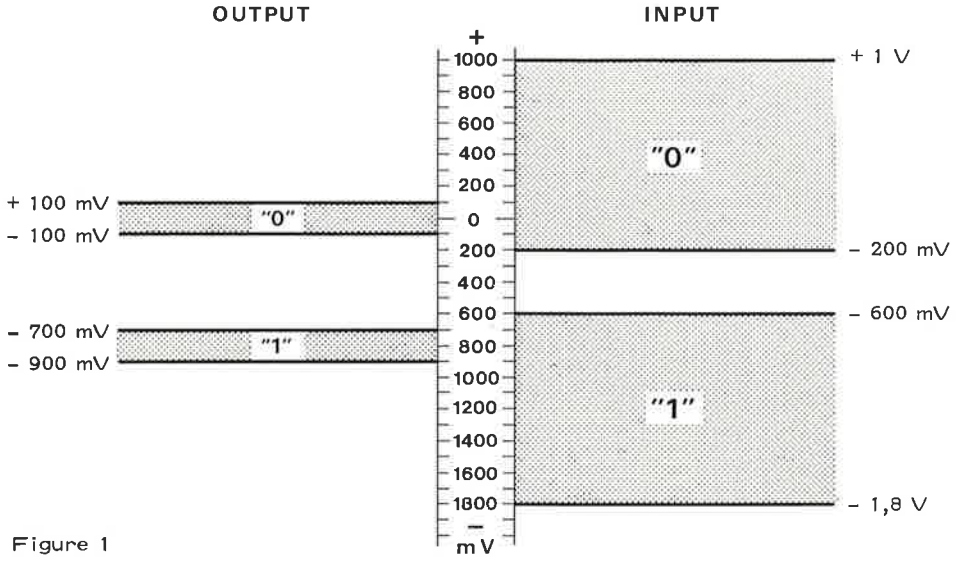


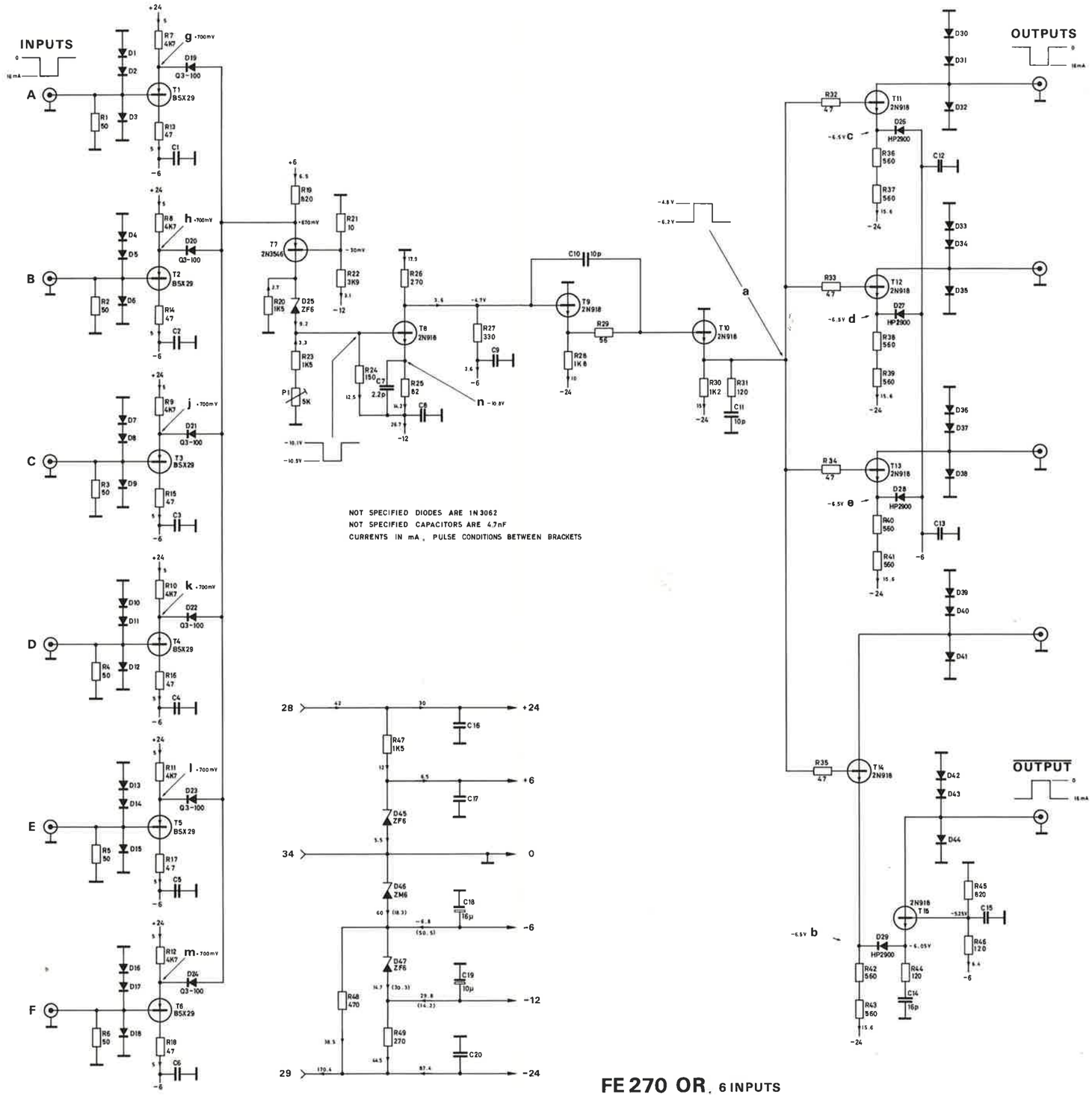
Figure 1

Or

Part List

	Component		Value	Manuf.
R 1- 6	2%	1/4 W	50	Metallux
R 7-12	5%	"	4K7	AB
R13-18	"	"	47	"
R19	"	"	820	"
R20	"	"	1K5	"
R21	"	"	10	"
R22	"	"	3K9	"
R23	"	"	1K5	"
R24	"	"	150	"
R25	"	"	82	"
R26	"	"	270	"
R27	"	"	330	"
R28	"	"	1K8	"
R29	"	"	56	"
R30	"	1/2 W	1K2	"
R31	"	1/4 W	120	"
R32-35	"	"	47	"
R36-43	"	"	560	"
R44	"	"	120	"
R45	"	"	820	"
R46	"	"	120	"
R47	"	1/2 W	1K5	"
R48	"	1, 5 W	470	Painton
R49	"	"	270	"
P 1	20%	3/4 W Helitrim	5K	Beckman
C 1- 6	Ceram.		4, 7n	LCC
C 7	"	mini	2, 2p	Phil.
C 8	"		4, 7n	LCC
C 9	"		4, 7n	"
C10	"	mini.	10p	Phil.
C11	"	"	10p	"
C12-13	"		4, 7n	LCC
C14	"	mini.	15p	Phil.
C15	"		4, 7n	LCC
C16-17	"		4, 7n	"
C18	Electrol.		16µ-10V	Phil.
C19	"		10µ-16V	"
C20	Ceram.		4, 7n	LCC
D 1-18	Si Diode		1N 3062	Cosem
D19-24	Ge Diode		Q3-100	Int. DC
D25	Zener 6V ± 3%		ZF 6	Int. Rect.
D26-29*	Si Diode sel. ±50 mV at 14 mA		HP 2900	HP
D30-44	Si Diode		1N 3062	Cosem
D45	Zener 6V ± 3%		ZF 6	Int. Rect.
D46	Zener 6V ± 3%		ZM 6	Int. Rect.
D47	Zener 6V ± 3%		ZF 6	Int. Rect.
T 1- 6	PNP Si		BSX 29	SGS
T 7	PNP Si		2N 3546	Mot.
T 8	NPN Si		2N 918	TI
T 9	NPN Si		2N 918	"
T10	NPN Si		2N 918	"
T11-14	NPN Si		2N 918	"
T15	NPN Si		2N 918	"

*) selected ± 50 mV at 14 mA



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DRAWING NO FE55
DEC 23-68 RAPARAUS