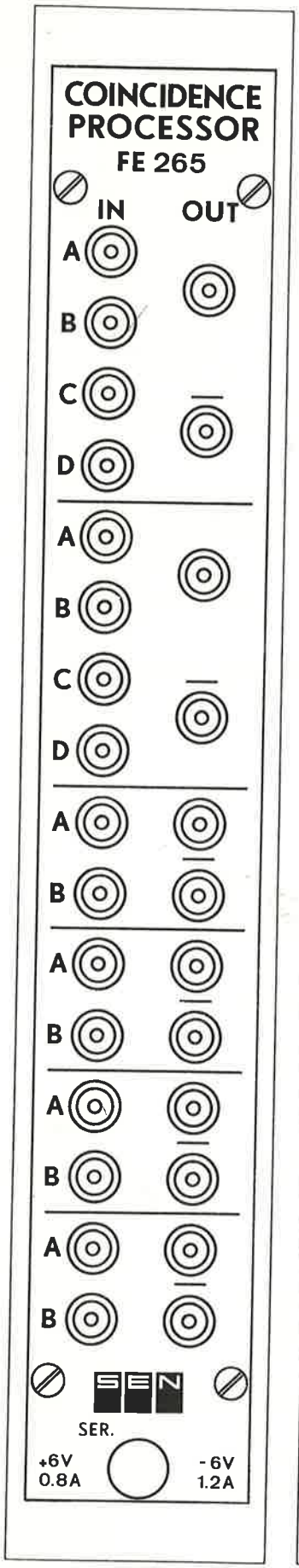
Fast Electronics

FE 265 COINCIDENCE PROCESSOR

SEN
ELECTRONIQUE



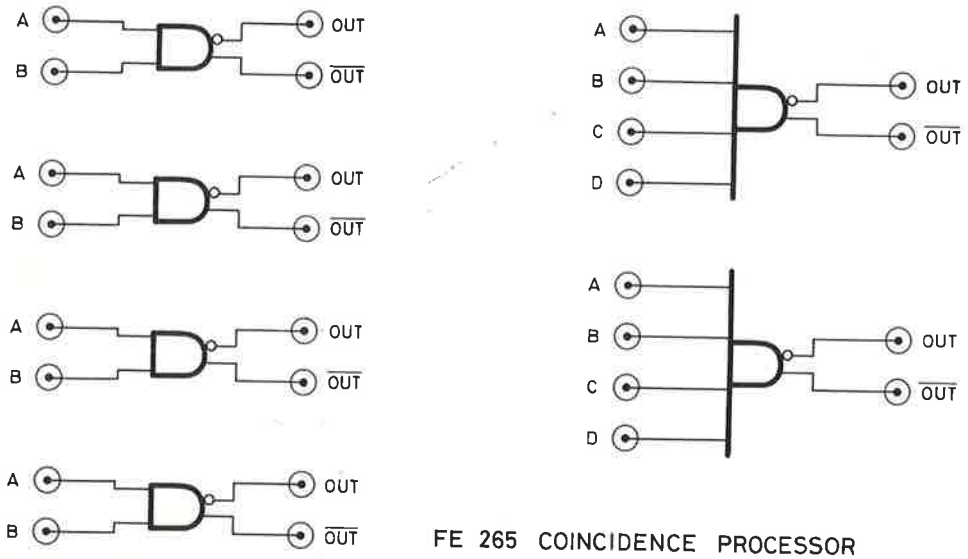
FE 265 Coincidence Processor

CERN N 6239

The unit will function as an OR-gate when logic (NIM: "0" = 0V, -800mV = "1") pulses are fed to the inputs, and as AND-gate in case of complementary logic pulses. In the latter mode, logic pulses can be applied for veto (or anticoincidence) purposes.

In the AND-mode an input is automatically activated when it is connected to a source of complementary logic signals. This also determines the coincidence conditions if the number of simultaneous input signals required to produce output signals equals the number of connected inputs.

One module contains two independent 4-input gates and four independent 2-input gates (each gate provides one inverted and one non-inverted output).



FE 265 COINCIDENCE PROCESSOR

SEN ELECTRONIQUE

PRELIMINARY FEBRUARY 1973

1211 GENEVE 13 - SUISSE - Case postale 57 - 31, Av. Ernest-Pictet - Tél. (022) 44 29 40 - Télex 23359 - Câbles SENELECTRON

SPECIFICATIONS

INPUT

AND-GATE MODE

Number:	2 four-input gates 4 two-input gates
Impedance:	50 ohms
Reflections:	≤12%
Voltage:	Complementary logic for coincidence. Logic for anticoincidence.
Width:	Shortest pulse to produce full output: ≤3.0ns (2.6ns). Shortest overlap≤3.2ns. Both measured at -200mV.
Crosstalk:	≤7% between inputs.
Maximum Rate:	≥150MHz, determined by output specifications.

OR-GATE MODE

Voltage:	logic
Width:	shortest pulse to produce full output ≤ 2.2ns (1.9ns) at -600mV.

For all other parameters refer to AND mode.

POWER REQUIREMENT

- 6V = 1.2A ± 25%

+ 6V = 800mA ± 30%

N.B. 1) Rise- and fall-times are measured between maximum output "0" (-100mV) and minimum output "1" (-700mV).

2) All parameters have been determined with input signals having rise- and fall-times of 0.7ns.

3) The values shown in brackets apply when the other output is matched.

OUTPUT

AND-GATE MODE

Number:	Each gate has one complementary logic output OUT (non-inverted), and one logic output $\overline{OUT}$ (inverted).
Impedance:	When output is at 0mV ≤4 ohms, it increases to ≤8 ohms at -800mV while loaded with 50 ohms.

Rise- and fall-times:

complementary	t_{01}	≤2.1ns (1.8ns)
	t_{10}	≤2.4ns (1.8ns)
logic	t_{10}	≤2.4ns (1.8ns)
	t_{01}	≤2.2ns (1.8ns)

Overshoot:	≤12%
Width:	Equal to input width, tolerance 0 to -1.6ns. Input width defined at -600mV for logic inputs and at -200mV for complementary logic inputs. Outputs widths defined in the same manner.
Crosstalk:	≤12% from input of one channel to the output of another.

Propagation delay:
4.4 ±0.8ns (4.0 ±0.8ns) between -200mV at input and -100mV at output.

OR-GATE MODE

Number:	Each gate provides one logic output OUT (non-inverted), and one complementary logic output $\overline{OUT}$ (inverted).

Rise- and fall-times:

logic	t_{01}	≤2.0ns (≤1.8ns)
	t_{10}	≤2.4ns (≤1.8ns)
complementary	t_{10}	≤2.4ns (1.9ns)
	t_{01}	≤1.9ns (≤1.6ns)

Overshoot:	≤12%
Width:	Equal to input width, +0.4 to -0.8ns. Input width defined at -600mV for logic inputs and -200mV for complementary logic inputs. Output width defined in the same manner.

Propagation delay:
4.0 ±0.6ns (3.7 ±0.6ns) between minimum input and output 1 state.

For all other parameters refer to AND mode.

SEN ELECTRONIQUE

FE 265 Coincidence Processor

1.5 Output Levels.
Mach all inputs. Check with the DVM that all non-inverting outputs are 0 ±80 mV and that the inverting outputs are -800 ±80 mV. While measuring the levels, the outputs must be loaded with 50 ohms. If one or more "0" levels are not correct, readjust R74 to bring them inside tolerance. If one or more "1" levels are not correct, readjust R79. Correct sequentially to each input -800 mV (from 50 ohm source impedance) and verify again the output logic levels as above.

1.6 Power Requirements, without Load.
Check the following: +6V ≤850mA
-6V ≤1100mA

2. Pulse Tests

2.1 Coincidence Test

Apply 10ns complementary logic pulses, rate of 10MHz, sequentially to each input, verifying that the related outputs appear correctly.

Apply the same pulses to the inputs of each section simultaneously, and verify that the outputs are again correct.

2.2 Rise and Fall Times:

a) Apply logic pulses in sequence to a single input.
Pulse width: 10ns. Rate: 10MHz.

Outputs should be as follows:

Logic	t_{01}	≤ 2.0ns
	t_{10}	≤ 2.4ns
Complementary	t_{10}	≤ 2.4ns
	t_{01}	≤ 1.9ns

b) Apply complementary logic pulses in sequence to a single input.
Pulse width: 10ns. Rate: 10MHz.
Outputs should be as follows:

Complementary	t_{01}	≤ 2.1ns
	t_{10}	≤ 2.4ns
Logic	t_{10}	≤ 2.4ns
	t_{01}	≤ 2.2ns

ADJUSTMENT AND TEST PROCEDURE

A. INSTRUMENTS REQUIRED

1. Power Supply +6V (1A min.) -6V (1,4A min)
2. Sampling Oscilloscope Tektronix, type 561A or equivalent.
3. Pulse Generator, type EH 122 or equivalent.
4. Digital Voltmeter, type ED 2043 ROCHAR or equivalent.
5. Electronic Multimeter Philips, type PM 2401 or equivalent.
6. Delay Box 2.5 - 66ns, type FE 290 (CERN N9053).
7. Three-Way Resistive Split.
8. Four-Way Resistive Split.
9. LEMO Cables:
   3 x 5ns (split to coincidence processor from coincidence processor to scope)
   1 x 0.5ns (EH to split)
   1 x 8ns (EH to scope trigger)
   1 x 3ns
   1 x 2ns
10. 4 Adaptors LEMO/GEN. RADIO
    1 Adaptor LEMO/BNC
11. 3 matching pieces LEMO 50 ohms.
12. Check-Out Table.

B. ADJUSTMENT PROCEDURE

1. DC Adjustment

1.1 Turn all potentiometers anti-clockwise.

1.2 Connect supply voltages.

1.3 +0.92V Adjustment:
Connect digital voltmeter between C41 (33µF) and ground.
Adjust, turning R74 (100 ohms) clockwise to give reading of +0.92V.

1.4 -4.60V Adjustment:
Connect the digital voltmeter between C46 (33µF) and ground.
Adjust, turning R79 (50 ohms) clockwise to give reading of -4.60V.

2.3 Minimum Input Width:

Connect 2.2ns wide logic pulses at 10MHz rate to the inputs.
Verify that all outputs attain the output "0" band (-100mV), and the output "1" band (-700mV).

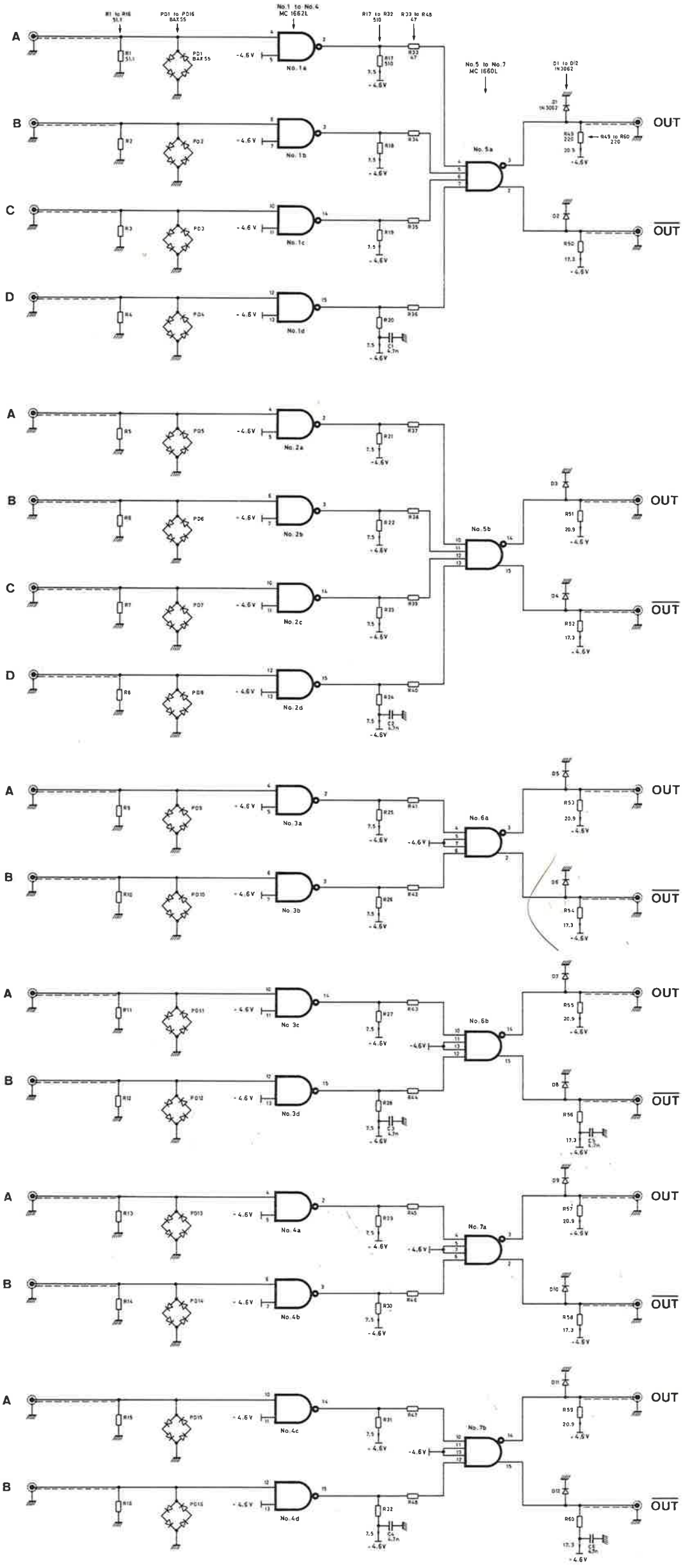
2.4 Output Width:

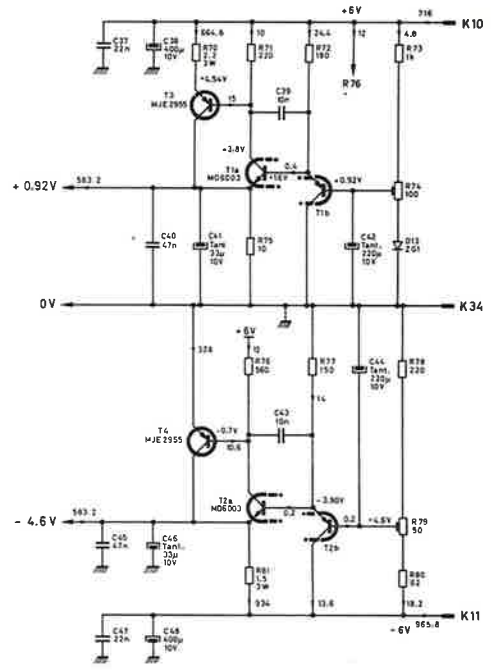
a) Apply 10ns wide logic pulses at 10MHz rate to the inputs.
Outputs should be equal to input width +0.4 to -0.8ns.
Repeat measurement for each input, checking the two corresponding outputs.

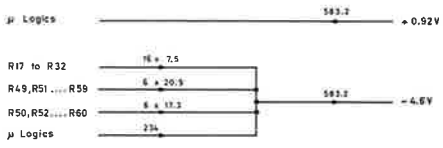
b) Apply complementary logic pulses, 10ns wide at 10MHz rate.
Outputs should now be equal to input width +0 to -1.6ns.
Repeat measurement for each input, checking the two corresponding outputs.

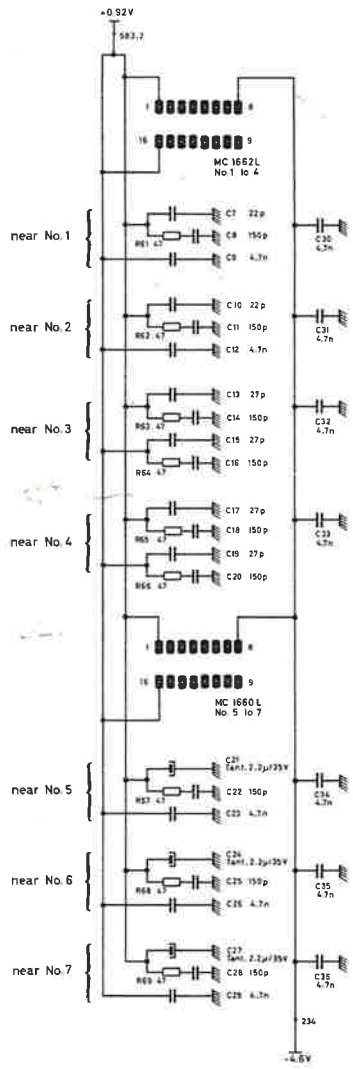
2.5 Rate Test:

Connect 3.5ns wide logic pulses, at 150MHz rate, sequentially to each input, and verify that the related outputs attain "0" and "1" bands.









NOTE : T1, T2 + Heatsinks Thermalloy 2211
T3, T4 + Heatsinks see drawing 8016-1A4

FE 265

SEN ELECTRONIQUE

CERN N6239

COINCIDENCE PROCESSOR