SEN
ELECTRONIQUE

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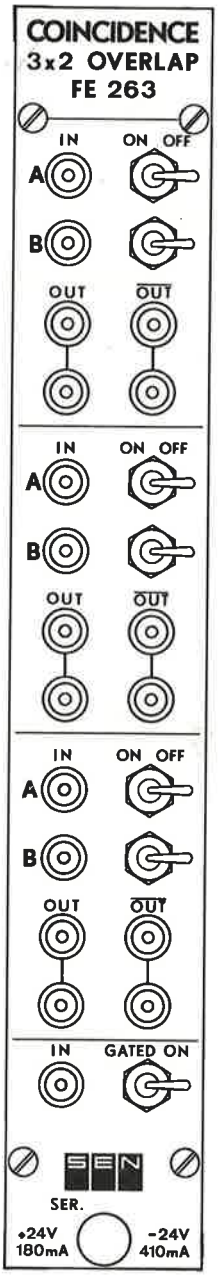

FE 263 COINCIDENCE

Triple, Two-Fold, Overlap

(CERN Type N6237)

Purpose

Three individual twofold coincidences are provided.

Logic pulses are required for coincidence operation, complementary logic pulses for anticoincidence operation.

General Features

Each input can be activated by a front panel switch.

The output width is equal to the input width or overlap.

The individual sections can be gated by a common gate signal.

SPECIFICATIONS

INPUT (for each individual section)

Number	2
Impedance	50 ohms
Reflections	In "ON" State : $\leqslant$ 20% (capacitive) In "OFF" State : $\leqslant$ 20% (inductive)
Voltage	Logic, −800 mV for coincidence. Complementary logic for anti-coincidence.
Width	Minimum width or overlap (at minimum input "1" level = −600 mV) to produce outputs $\leqslant$ 2.0 ns Maximum D.C.
Maximum rate	$\geqslant$ 150 Mc/s determined by output specifications.

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OUTPUT (for each individual section)

Number	2 logic 2 complementary
Impedance	High, current source. The unused output of any dual must be terminated, but completely unused duals need not be terminated.
Rise and fall times	Logic : $T_{01} \leqslant 1.7$ ns, $T_{10} \leqslant 2.0$ ns Complementary : $T_{10} \leqslant 1.5$ ns, $T_{01} \leqslant 2.0$ ns
Width	Equal to input width or overlap at minimum input "I" level (−600 mV), with the following tolerances, Logic : −0.5 to +1.0 ns at minimum input "I" (−600 mV) Complementary : +0 to +1.3 ns at maximum input "0" (−200 mV)
Maximum rate	$\geqslant$ 150 Mc/s.
Propagation delay	7.5 ±1.2 ns (between min. input and output "I")
Feedthrough	for n-I $\leqslant \lvert\pm 5\rvert$ mV

GATE

Front panel switch controlled. In position "ON" outputs are produced on the application of input signals, without the necessity of a gate signal. In position "GATED" inputs will produce outputs only if the logic level (min. −600 mV) – D.C. or pulse – is present at the gate input.

Impedance	50 ohms
Reflections	$\leqslant$ 20%
Voltage	Logic, −800 mV for "ON" gating. Complementary logic for "OFF" gating.
Width	Shortest pulse to open or close gate $\leqslant$ 2.5 ns at minimum input "I" level (−600 mV) Minimum overlap with input pulses to produce output of min. output "I" $\leqslant$ 2.5 ns. Maximum D.C.
Maximum Rate	$\geqslant$ 125 Mc/s.
Propagation Delay	Delays of INPUT and GATE are equalized up to input AND-gate.

POWER CONSUMPTION −24 V 410 mA ± 20 mA +24 V 180 mA ± 10 mA

N.B. 1) Rise (T_{01}) and fall-times (T_{10}) are measured between maximum output "0" (−100 mV) and minimum output "I" (−700 mV)

2) All parameters have been determined with input signals having rise and fall times of 0.7 ns.