SEN
ELECTRONIQUE

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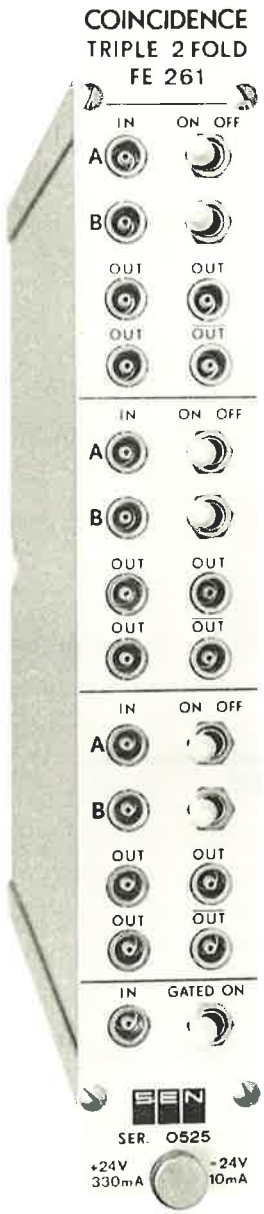


# FE 261 COINCIDENCE

## Triple 2 Fold

### Purpose

Three individual twofold coincidences are provided.

Logic pulses are required for coincidence operation, complementary logic pulses for anticoincidence operation.

The individual sections can be gated by a common gate signal.

### General Features

The Coincidence with LEMO connectors is built in a single-width NIM module. With BNC connectors it is a double-width module.

Each input can be activated by a front panel switch.

The output width is fixed.

**BNC – Connectors:** The same module is available with BNC connectors instead of LEMO connectors. The ordering number is **FE 261/B**



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## SPECIFICATIONS

**INPUT** (for each individual section)

| | |
|---|---|
| **Number** | 2 |
| **Impedance** | 50 ohms |
| **Voltage** | Logic, -800mV for coincidence<br>Complementary logic for anti-coincidence |
| **Width** | Minimum width or overlap (at - 12mA) to produce outputs $\leqslant$ 1.5ns<br>Maximum : DC |

**OUTPUT** (for each individual section)

| | | | |
|---|---|---|---|
| **Number** | 3 logic, 1 complementary logic | | |
| **Impedance** | High, current source. Unused outputs need not be terminated. | | |
| **Rise and Fall Time** | Logic | $T_{01} \leqslant$ 1.5ns | $T_{10} \leqslant$ 2.0ns |
| | Complementary | $T_{10} \leqslant$ 1.5ns | $T_{01} \leqslant$ 2.0ns |
| **Width** | Logic | 8.5 ± 0.75ns (at-12mA = min. "I") | |
| | Complementary | 8.75 ± 0.75ns (at -4mA = max. "O") | |
| **Max. Rate** | $\geqslant$ 50Mc/s | | |
| **Propagation Delay** | 10.0 ± 1.5ns (between min. input and output "I") | | |

**GATE**

Front panel switch controlled. In position ON outputs are produced on the application of input signals, without the necessity of a gate signal. In position GATED inputs will produce outputs only if the logic level (min. -600mV) -- DC or pulse — is present at the gate input.

| | |
|---|---|
| **Impedance** | 50 ohms |
| **Voltage** | Logic, -800mV, for ON gating<br>Complementary logic for OFF gating |
| **Width** | Shortest pulse to open or close gate $\leqslant$ 2.5ns (at -12mA = min. "I").<br><br>Minimum overlap to make with imputs to produce outputs $\leqslant$ 3.5ns (at -12mA = min. "I").<br>Maximum : DC |
| **Max. Rate** | $\geqslant$ 50Mc/s, determined by output specifications. |
| **Propagation Delay** | Delays of INPUT and GATE are equalized up to input AND gate. |

**POWER CONSUMPTION** -24V 510 ± 30mA +24V 330 ± 20mA

N.B. 1) Rise ($T_{01}$ and fall times ($T_{10}$) are measured between output "O" (-100mV and minimum output "I" (-700mV).

2) All parameters have been determined with input signals having rise and fall times of 0.7 ns.

**Specifications subject to minor changes without notice.**