technical information manual

NIM Model 622

Quad 2-Fold Logic Unit

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
West Nyack, New York

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refine and improve the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Spring Valley, NY, telephone 914-425-2000, or from your local distributor in countries other than the U.S.A.

LeCROY RESEARCH SYSTEMS

technical information manual

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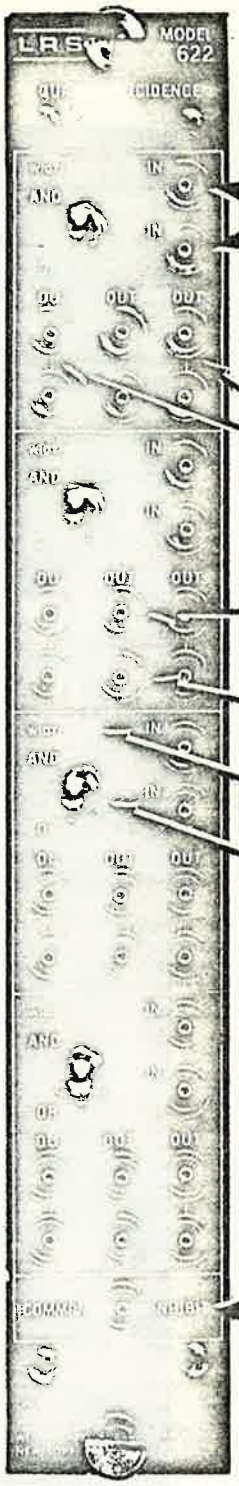
NIM Model 622
Quad 2-Fold Logic Unit



50 Ω inputs; require NIM fast logic level (>-600 mV)

2 pairs of bridged negative outputs; switched current source; 50 Ω; quiescently 0 mA; logical 1, -32 mA per pair.

1 individual normal output; 50 Ω; full differential type current source; quiescently, 0 mA; logical 1, -16 mA.

1 complementary output; 50 Ω; quiescently -16 mA; logical 1, 0 mA.

Width adjust, 5 nsec to 1 μsec; continuous to 600 nsec (1 μsec at end of pot).

Function switch determines "AND" or "OR" operation.

#1 width standard NIM module package; 7.8 watts power consumption; utilizes ±6 V, ±12 V, -24 V.

Common leading edge inhibit (veto); 50 Ω; requires >-600 mV signal.

ENGINEERING DEPARTMENT
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SPECIFICATIONS
NIM Model 622
QUAD 2-FOLD LOGIC UNIT

INPUT CHARACTERISTICS

Number of Channels:	4, all identical.
Logic Inputs:	Two, 50 Ω direct-coupled; reflections < 7% for standard AEC fast logic signals (−600 mV minimum) of 2 ns risetime.
Slow Bin Gate:	Via rear connector, with rear-panel, ON/OFF switch; quiescently +4 volts, clamping to ground inhibits logic unit; direct-coupled; risetimes and falltimes approximately 50 ns.
Veto:	Front-panel connector permits simultaneous inhibiting of all channels; 50 Ω; requires NIM-level signal (> −600 mV); direct-coupled; must overlap leading edge of input signal that would otherwise cause the coincidence condition; must precede input by approximately 5 ns.

OUTPUT CHARACTERISTICS

Bridged Negative Outputs:	2 pairs; NIM, quiescently 0 mA, −32 mA during output; duration, 5 ns to 1 μs, continuously variable up to 600 ns via front-panel screwdriver control (narrower widths possible at slight expense of amplitude); risetimes and falltimes (all outputs terminated in 50 Ω) typically 2.0 ns (max. 2.5 ns), 10% to 90%. Output falltimes slightly longer on wide output durations. Width stability better than ± 0.2%/°C maximum. Updating.
Fast Negative Timing Output:	One, NIM; quiescently 0 mA, −16 mA during output. Other characteristics same as above, except risetimes are typically 1.5 ns (max. 2.0 ns) and minimum width is ≤ 6 ns.
Complementary Output:	One; quiescently, −16 mA, 0 mA during output. Other characteristics same as for Fast Negative Timing Output.

GENERAL

Functions:	Fan-in (2-fold); coincidence; inhibit.
Maximum Rate:	110 MHz typical, input and output.
Coincidence Width:	Determined by input pulse durations; total widths from approximately 1.0 ns up without limit.
Double-Pulse Resolution:	Less than 9 ns at minimum output width setting.
Input-Output Delay:	9.5 ns typical.
Multiple-Pulsing:	None; one and only one output pulse of preset duration is produced for each input pulse, regardless of input pulse amplitude or duration.
Packaging:	In RF-shielded, AEC/NIM #1 module (AEC Report #TID-20893); Lemo-type connectors.
Current Requirements:	−6 V at 450 mA; +6 V at 215 mA; −12 V at 165 mA; +12 V at 20 mA; −24 V at 85 mA.

UPDATING ADDENDA TO GENERAL DESCRIPTION OR SPECIFICATIONS

Current Requirements:	The -24 V current drain is actually 85 mA as opposed to the "160" mA indicated in the specifications.
Coincidence Resolving Time:	The required minimum coincidence overlap time of the 622 in the "And" mode is 1.1 nsec.
Resolving Time Jitter:	The Resolving Time Jitter, as defined in the Operation section of this manual, is $\pm$20 psec.

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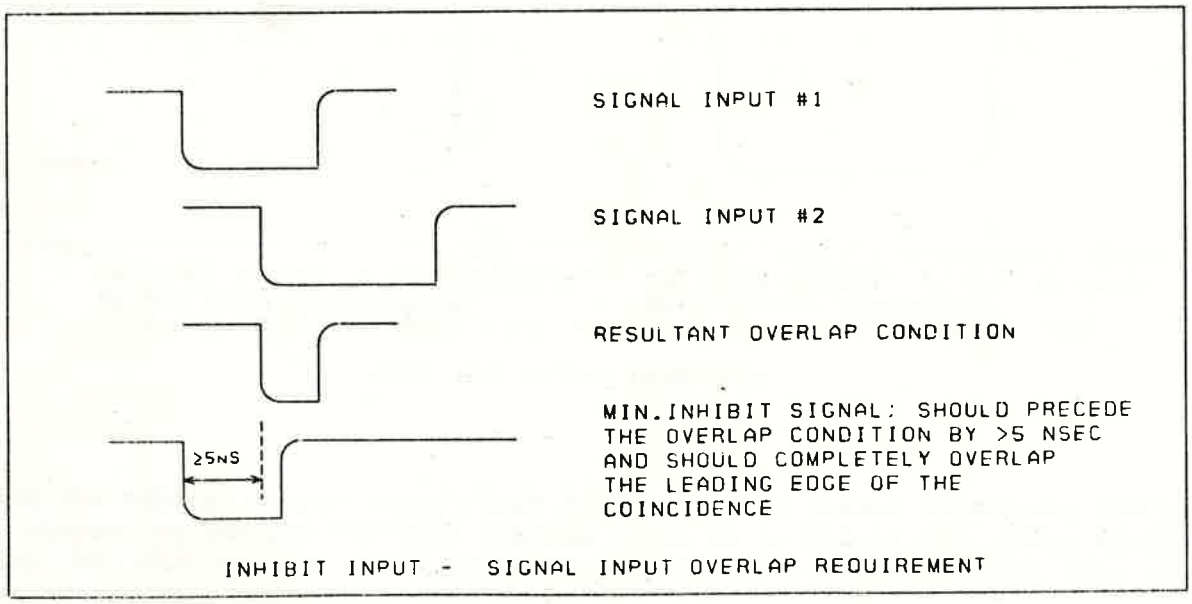
Input Characteristics

Logic Inputs: The Model 622 has direct-coupled, 50 Ω impedance inputs which accept fast NIM logic signals (-0.6 V to -1.8 V). These inputs, typically driven from a discriminator or other logic unit, are protected both for transient and DC signals up to ±5 volts. Since the input reflections are less than 7% for signals of as little as 2 nsec risetime, even the maximum level signal in the NIM-specified range for a logic input (i.e., -1.8 volts) will reflect only approximately 125 mV, eliminating the probability of accepting multiple pulses corresponding to only one original input pulse.

Common Inhibit Input: The common inhibit input of the 622 requires NIM logical one input signals as described above. In order to inhibit (veto) a coincidence, the applied veto pulse must overlap the leading edge of the input signal that would otherwise cause the coincidence condition. Due to internal delays, the leading edge of the veto signal should precede the coincidence by at least 5 nsec. Consider the diagram below.



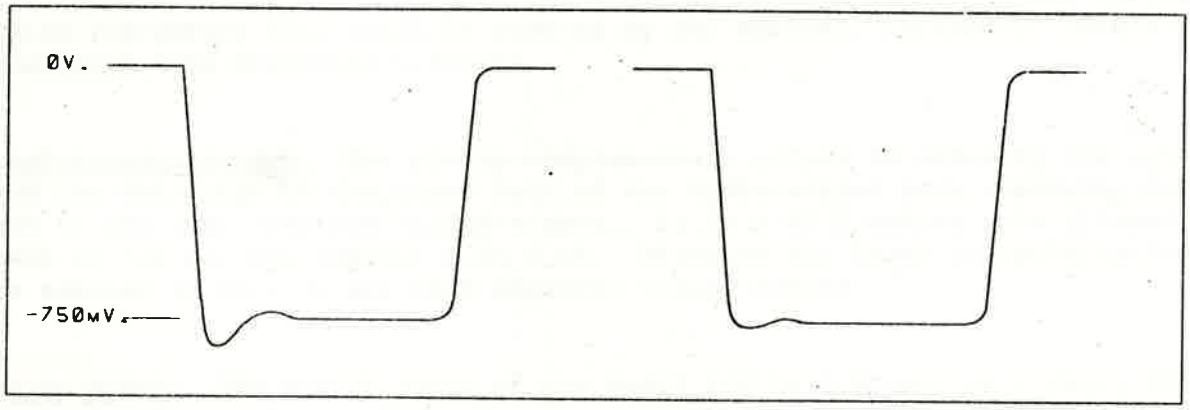
INHIBIT INPUT - SIGNAL INPUT OVERLAP REQUIREMENT

To veto signals when the 622 is set in the "OR" condition, the inhibit signal must merely overlap the leading edge of any pulse it is to inhibit, subject to the ≥5 nsec delay mentioned above.

Output Characteristics

Bridged Negative Outputs: The Model 622 has two pairs of current source 50 Ω outputs, delivering -32 mA of current during the output and 0 mA quiescently. These outputs are of the switched current source type, requiring no quiescent current and permitting extremely low power dissipation in the total circuit. The standard switched current outputs maintain a risetime of 2.5 nsec. and a reasonably clean shape, as long as care is taken to terminate at least one-half of the other bridged output in that channel.

The actual shape of typical outputs from 622 are approximated below.

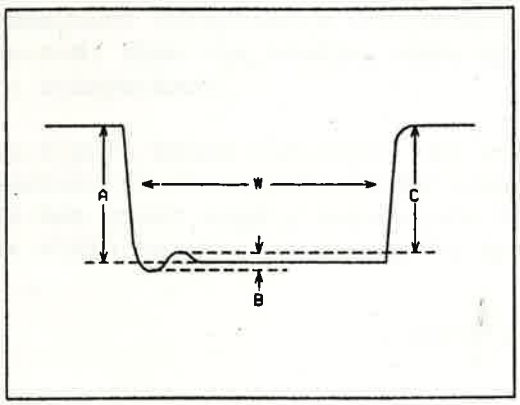


SWITCHED CURRENT OUTPUT, ADJACENT OUTPUT PAIR UNTERMINATED: TR-2.5 NSEC; OVERSHOOT <15%

SWITCHED CURRENT OUTPUT, ADJACENT OUTPUT PAIR TERMINATED: TR-2.0 NSEC; OVERSHOOT <10%

MODEL 622 OUTPUT WAVEFORMS

Using the typical output pulse shape following as a visual reference, LRS output shapes for current switched outputs (such as on Models 622, 621L, 621AL, 621BL, 621 BLP) are set up to adhere to the following restrictions, with adjacent output pair terminated into 50 Ω.



AMPLITUDE: -700mV<A<-850mV.

OVERSHOOT: B<10% OF A; C DOES NOT REACH -600mV

RISETIME: <2.5 NSEC.

FALLTIME: <2.5 NSEC. AT MINIMUM WIDTH.

MINIMUM WIDTH: WMIN (FWHM) <5.0 NSEC.

MAXIMUM WIDTH: WMAX (FWHM) - 1 USEC.

Fast Negative Timing Output: The fast negative timing output on the 622 is a full differential type current source output. Its name originates from the contrast in risetime (1.3 nsec vs. 2.5 nsec) between it and the other 4 negative outputs on the 622. Because the risetime is much faster, there is less timing inaccuracy that would be created by the nominal "threshold" levels of subsequent time measuring circuits.

Complementary Output: The single complementary output is actually the output from the collector of the other half of the differential pair supplying current to the fast negative timing output. It is a 50 Ω output with quiescent level at -16 mA, and logical 1 at 0 mA. Risetime and other characteristics are similar to that of the fast negative timing output.

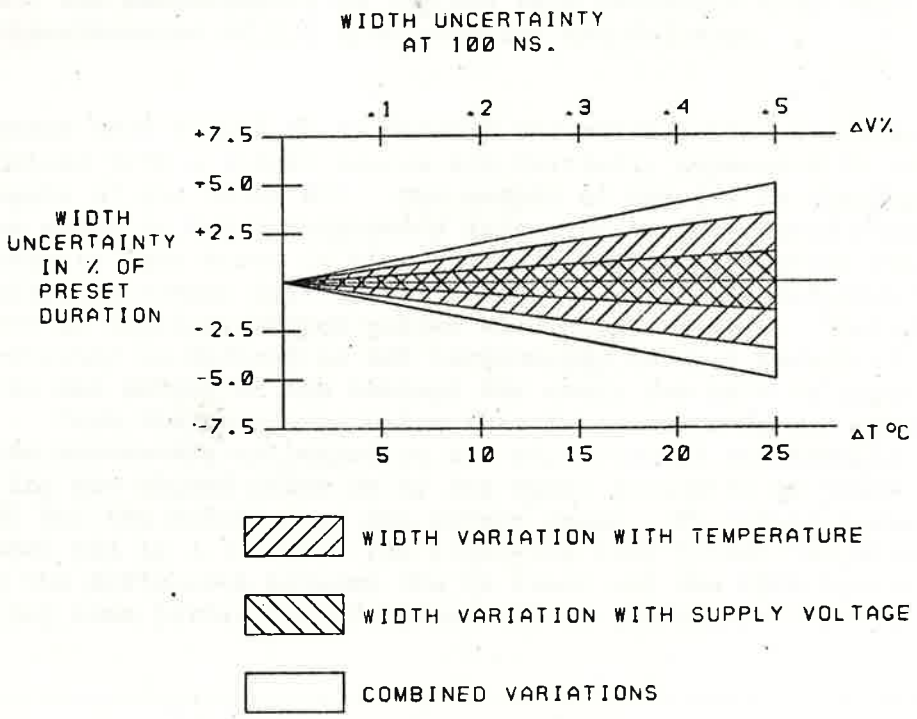
Output Width: The output range of the Model 622 is 5.0 nsec to 1 μsec, continuously adjustable via front-panel potentiometer. Because the potentiometer is very sensitive beyond 600 nsec, it is actually almost impossible to set the width between 600 nsec and 1 μsec. As a result, the specifications indicate continuous adjustment up to 600 nsec, with a ≃1 μsec setting at the far end of the pot.

Output Width Uncertainty

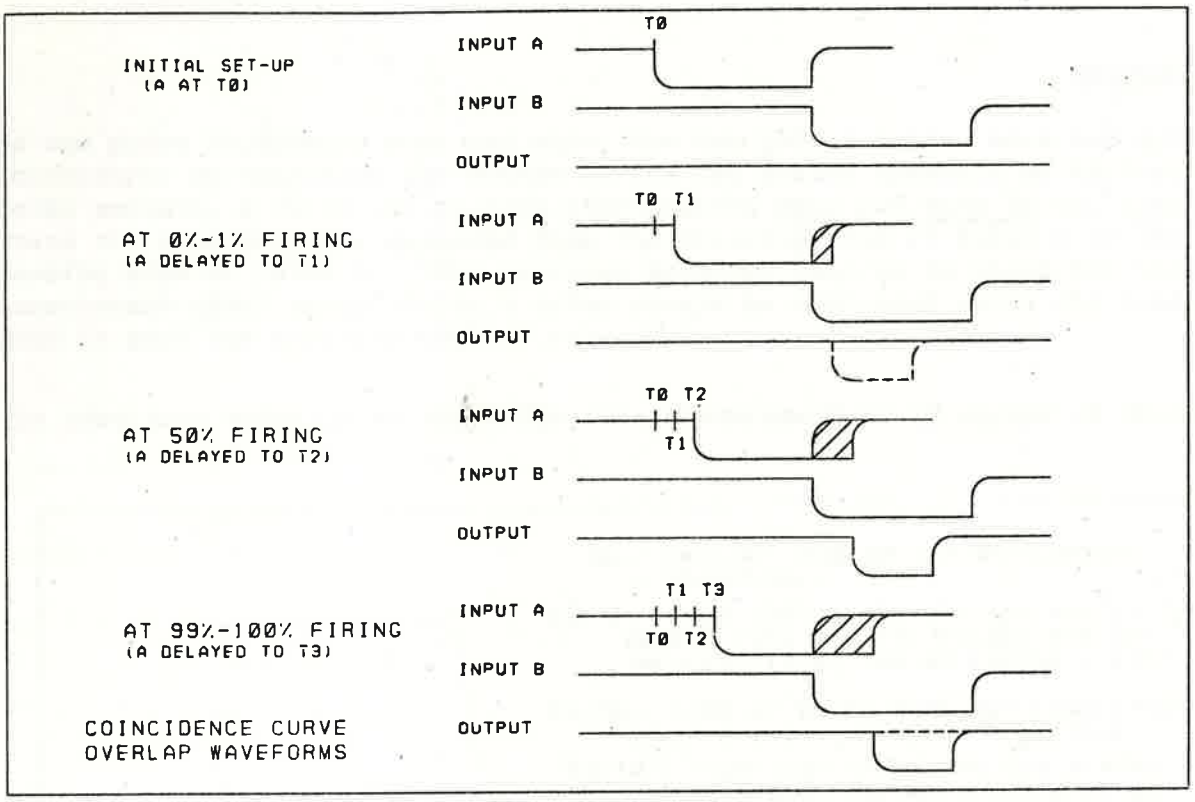
The main contributions to output uncertainty in the Model 622 are a function of external conditions. Variations in both temperature and NIM bin voltage can

cause slight changes in output width with consequences that may be adverse to subsequent coincidence measurements. If the output pulses are to be simply counted, then the leading edge is the important factor and width variations are unimportant.

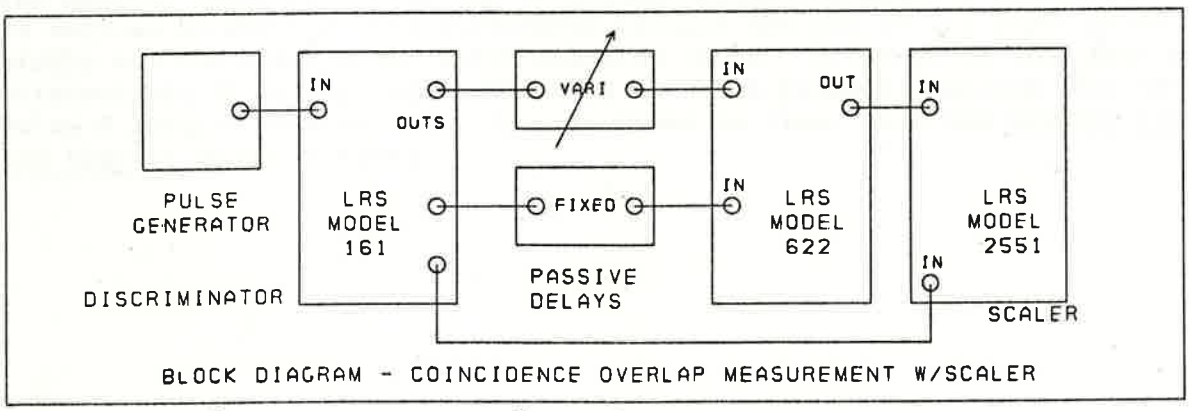
The figure below indicates the uncertainty in output width of the 622 as a function of reasonable variations in temperature and supply voltage. Since the 622 has power supply regulation in it and is very well temperature compensated, the width variations are quite insignificant.



Usage of Bridged Negative Outputs Driving a Single Cable: In applications where it is necessary to drive very long cable lengths from a logic unit output it is common to use only one half of the bridged 32 mA output and to leave the other half unterminated. This effectively sends all 32 mA into the one cable, giving nearly a double amplitude output. It is important to know that the 622 has clamp diodes that limit the output amplitude so as not to saturate the output transistors. This limit is approximately -1.4 volts. It cannot be assumed, therefore, that the 32 mA into one 50-ohm cable will give a 1.6 volt output signal.



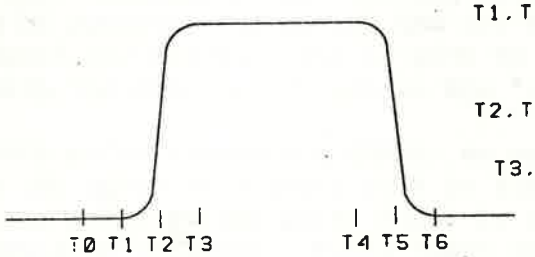
Coincidence Curve Method of Measuring Resolving Time: An alternate method used at LRS to measure the resolving time and time jitter involves making a coincidence curve and then measuring its "risetime" and "falltime". Two pulses from a single source are initially separated in time and fed into the inputs of the 622, at the same time being collectively counted in a scaler (see diagram folowing). The 622 output is also counted into another scaler channel.



BLOCK DIAGRAM - COINCIDENCE OVERLAP MEASUREMENT W/SCALER

As one pulse is delayed more and more, the two pulses become more and more coincident; by comparing the counts in the two scaler channels at different delay amounts, a curve can be made representing Rate Out/Rate In vs. Time Delay where the time delay is measured from the trailing edge of Pulse A to the leading edge of Pulse B. (The previous waveform diagram is valid for this measurement also, except Pulse A delay should be continued until its leading edge is past the trailing edge of Pulse B.)

The resultant coincidence curve for this measurement would appear as follows:



COINCIDENCE OVERLAP
MEASUREMENT WAVEFORM

T0 - INITIAL TIME OF NON-OVERLAPPED CONDITION

T1.T6 - TIME JUST WHERE THE 622 BEGINS TO DETECT THAT THE TWO PULSES ARE CO-INCIDENT. (I.E. THE 0% FIRING LIMIT)

T2.T5.- TIME AT WHICH RATE OUT EQUALS 50% OF RATE IN. (I.E. 50% TRIGGERING)

T3.T4 - TIME JUST WHERE THE 622 ALWAYS DETECTS BOTH PULSES A AND B IN CO-INCIDENCE (I.E. 100% FIRING POINT) THE COINCIDENCE WIDTH W IS DEFINED AS THE DURATION BETWEEN THE 50% FIRING POINTS (I.E. T5-T2) THE RESOLVING TIME JITTER IS THE TIME DURATION BETWEEN T1 AND T3

The minimum coincidence overlap or minimum resolving time of the logic unit is defined as one-half the difference between the sum of the input pulse widths and the coincidence width measured above. Alternately (but with more difficulty), if t_0 represents the time at which pulse A trailing edge and Pulse B leading edge are exactly coincident in time, then the minimum resolving time is equal to t_2-t_0.

If both input pulses A and B are identical in shape, and if the inputs to the coincidence unit are identical, the trailing edge side of the coincidence curve should be symmetrical to the leading edge side. If they differ, the larger one (either 0% to 100% or 100% to 0%) is specified as the resolving time jitter.

It is important to note that the major contribution toward resolving time jitter in typical logic units is the instability of the "threshold" level of the differential amplifier following the input "AND" stage, particularly for inputs with slow inherent risetimes (i.e., $\geq$ 2 nsec). In the 622, a true high sensitivity discriminator is used which has a very stable and jitter-free threshold (the LD601C hybrid used in all LRS multichannel NIM discriminators). For this reason, the resolving time jitter of the 622 is quite small.

Timing Characteristics: Maximum CW rate capability of the 622 is guaranteed at 100 MHz. Typically, the maximum rate is 110 MHz, with some units being capable of operation up to 120 MHz for small bursts of input pulses. The measurement for maximum rate is made by applying pulses to one of the two inputs, with the mode switch set in the "OR" position.

The double pulse resolution (DPR), as opposed to CW rate capability, actually defines the speed of a logic unit in high energy physics applications, since the double pulse or the pulse burst is apt to occur, whereas a CW input pulse train would be unlikely. For a logic unit in the "AND" mode, the coincidence width of the input pulses would limit the double pulse resolution of the unit. Each input itself is capable of operation at a 110 MHz CW rate and a DPR of 9 nsec. This measurement is made by setting the 622 in the "OR" mode, putting in two 4 nsec FWHM pulses spaced approximately 10 nsec apart at the half maximum points (i.e., -375 mV for a -750 mV input signal) and finding how far this 10 nsec time difference can be lowered before the 622 output pulse achieves only a 50% firing rate (i.e., Rate Out/Rate In = 0.5). Alternately, with the 622 set in the "OR" position, two pulses can be fed from different cables into the two inputs. By varying the time from leading edge of one (half max. point) to the leading edge of the other, the DPR can be measured. Care should be taken to use pulses of as narrow a width as possible when measuring minimum double pulse resolution.

Packaging: The 622 Quad Coincidence Unit is packaged in a #1 NIM module with Lemo-type connectors. Due to front panel space limitations, the 622 is not offered with BNC's.

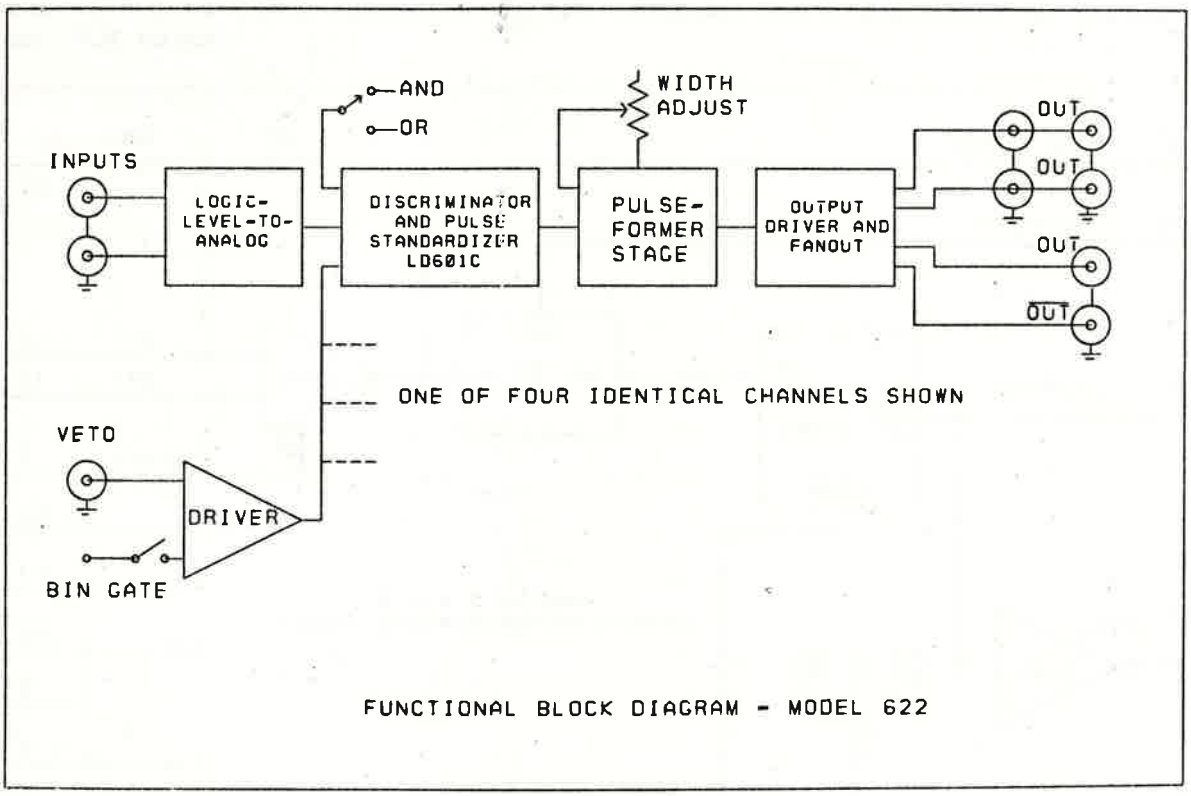
Power Requirements: The current usage of the 622 is low enough to permit the use of the 12 modules per standard 96-watt NIM bin offering 5 A of +6 V, 2 A of ±12 V, and 1 A of ±24 V. Power calculation works out to 7.8 watts, which does not exceed the 8 watts recommended by the NIM standard for the maximum power dissipation for a single NIM slot.

Recommended Use of the NIM Power Bins: It is highly recommended to keep any NIM bin at as constant a temperature as possible, using air conditioning in the trailer or experimental station and definitely using fans to assure an air flow through all modules in every bin. Elimination of large temperature variations removes the worry of temperature drift effects upon modules of any manufacturer, and the forced air flow is good insurance against the potential failure of components in the modules due to excessive heating for extended periods of time. Despite the fact that all components are pre-aged and burned-in before insertion into LRS modules, and the modules themselves are temperature cycled for days under power between initial test and final test, it is recommended to avoid subjecting any modules to adverse operating conditions if it could be avoided.

FUNCTIONAL DESCRIPTION

General

Each of the four channels of the Model 622 is composed of four basic sections: The Input Logic-Level-to-Analog Converter, the Discriminator Stage, the Timing or Pulse-Former Stage, and the output Stage. A block diagram of the Model 622 can be seen below, and a complete schematic can be found at the end of this manual.



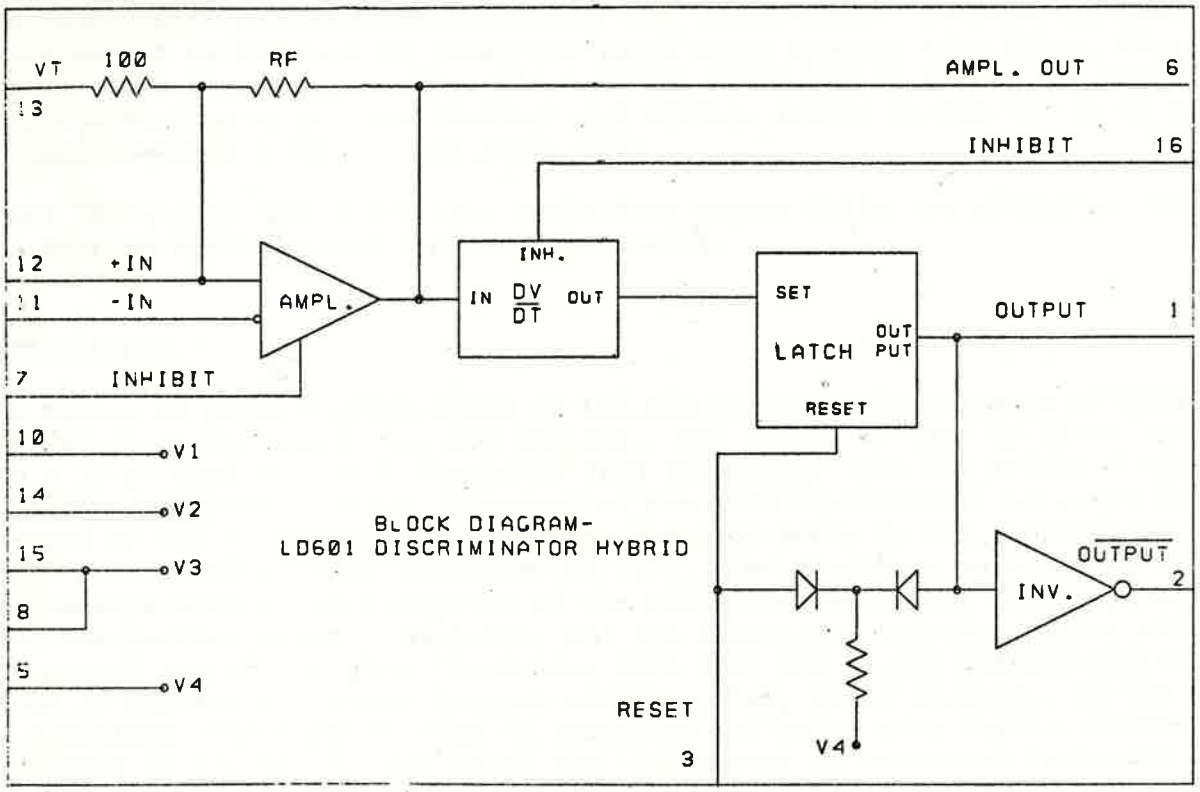
FUNCTIONAL BLOCK DIAGRAM - MODEL 622

Input Logic-Level-to-Analog Converter

The input stage accepts two inputs, and (via a two diode current switch) removes one unit of current per input from the resistor diodes connected to the -IN of the LD601C. The result is that with no inputs, the voltage at -IN is near zero volts, with one NIM-level input the -IN voltage will go to about -250 mV, with two inputs it goes to about -450 mV to detect the existence of two time coincident inputs (AND mode).

Discriminator and Pulse Standardizer Stage

The discriminator and pulse former stage is based on the LRS Model LD601C hybrid. This unit contains all of the circuitry of the discriminator as is functionally presented below. The threshold level is set by changing the voltage bias on a fast differential amplifier which has a small amount of internal positive feedback to provide regeneration at threshold. In actual operation the V_T is grounded, and the threshold level is determined by the 2.5:1 (AND) or 4:1 (OR) voltage divider (composed of the switch selected external 150 Ω or 300 Ω resistor and the internal 100 Ω resistor) operating from -0.8 volts.



BLOCK DIAGRAM-
LD601 DISCRIMINATOR HYBRID

When an input signal applied to -IN is equal to the threshold voltage at +IN the amplifier output will begin to go positive. This will force +IN closer to 0 volts, which increases the differential input voltage in such a direction that the output locks and then the cycle reverses. The amplifier output thus provides a time-over-threshold pulse with fixed amplitude. This pulse can be monitored at the AMPL. OUT point (Pin 6). The quiescent level should be nominally -2.4 volts going to -1.6 volts during the pulse. The leading edge

of this output sets the latch circuit which is used as a pulse width standardizer. Before the amplifier and the latch can be set, the inhibit inputs (used for the bin gate and veto) must be off. The required level at Pins 7 and 16 of the LD601 must be 0 to -1.6 V to enable, and -2.5 to -6.0 to disable. The purpose of the first inhibit is to avoid generating a low level transient at the output associated with the leading edge of an amplified input pulse inhibited at the dV/dt stage only. (The common inhibit driver provides a level shift so that 0 volts at the bin gate or -600 mV at the veto input will inhibit, greater than +3 volts at the bin gate input or 0 volts at the veto input will enable.) Once the latch is set, a latch OUTPUT is available to start the 622 timing stage. The OUTPUT amplitude and leading edge should be similar in appearance to the AMPL OUT above, but the width of the output will be fixed independent of the input width. Internally, the latch output is fed back to reset the latch after a short time delay, thus generating a short output pulse whose actual width can be set by the proper external section of RC time constant and voltage levels at Pin 3. It is set at approximately 3 nsec in the Model 622.

Older 622's used LD601B hybrids, while more recent units use LD601C's. These two hybrids are identical and interchangeable.

Timing Stage

The timing or pulse-forming stage of the 622 utilizes three stages of MC1692 MECL receiver for amplifying and shaping. The timing is done by first charging a 33 pf capacitor with the pulse from the LD601C (via one MC1692 stage) and the differential stage (composed of two A430 transistors) until it is clamped by the FD777 diode to a voltage set indirectly by the front-panel width potentiometer (via two stages of 747). The discharge rate is set by the current source stage composed of the width potentiometer, one stage of 747, the current source transistor, and its associated 604-ohm emitter resistor. The actual current is varied from near zero (for the 1 μsec maximum width) to about 10 mA (for the 5 nsec minimum width). Thus, simultaneously, as the width is increased, the clamp voltage is increased (allowing more initial charge to be stored on the timing capacitor) and the current is decreased (reducing the rate of discharge), thus multiplying the effect of the width control. An internal trim resistor, T, sets the minimum width to 5 nsec. The effect of the 2N5962 and the diodes associated with it are to provide fast recovery of the timing capacitor. The 1692 ECL amplifiers are interconnected in a manner to provide stable leading edge timing and fast risetimes and falltimes of the output pulse. The first amplifier (output pin 3) provides final shaping and standardization of the pulse from the LD601C to the timing stage, as well as

driving the output stage directly via a second 1692 amplifier (output pin 14). This provides a prompt output pulse for the duration of the 601C output, independent of the delay encountered in initializing the timing stage. Before the 601C output is over, the timing capacitor is charged, causing the third 1692 amplifier (output pin 15) to now maintain the pulse level to the output stage (using emmitter ORing until the timing capacitor is subsequently discharged to a sufficiently low level (approximately -2.0 volts)). At this point (because of regeneration) the third amplifier promptly switches back to its quiescent off condition, terminating the output pulse.

Output Stage

The output stages of the 622 utilize two different types of circuits. The single normal and complementary outputs use a conventional differential stage. This stage requires a continuous 16 mA of current which is quiescently available at the complementary output connector. During an output pulse, the MC 1692 receiver will switch from the quiescent level of -2.4 volts to a higher level of -1.6 volts, causing the differential stage to switch the 16 mA current from the complementary to the normal output connector for the duration of the pulse. The other two pairs of outputs each supply 32 mA of current during the pulse, because at this time the bases of the two A430 transistors are at -1.6 volts. The emitters are therefore at about -2.4 volts. This places about 600 mV across each 16-ohm emitter resistor, and the resulting 32 mA will be available at each output connector pair for the duration of the pulse. Quiescently, the bases of these transistors are at -2.4 volts; therefore, there is only a -600 mV drop available for V_{BE} so the transistors are off, resulting in a substantial power saving.

All outputs are diode clamped so they will provide proper operation even without output loads. Without the diode path for the current during the pulse, even on a single output stage, the current would have to be supplied via the transistor base, which would severely load the driver and not allow proper drive to the remaining stages.

The amplitudes of the Model 622's can be trimmed, if necessary, with resistors (labeled T) in parallel with the 10-ohm emitter resistors.

Internal Power Supplies

Four internal power supplies are used to generate the -0.8, -2.35, -3.0, and -11.5 V which are special bias voltages used by the four channels. These stages provide voltage regulation and tracking and provide proper temperature compensation for the other sections, particularly the width and threshold circuits. They depend to some degree on uniform heating of the entire circuit board. Heating local areas of the board may cause drifting, but during use in a normal bin environment, these supplies compensate to stabilize operation. In all cases, the power supply uses a LM301 operational amplifier to maintain the output voltage of a series-pass transistor equal to an input reference voltage. The reference voltages are adjusted via individual potentiometers or trimmed resistors.

If the -6 voltage is sequenced on before the +6 voltage, the LD601C may be forced into a DC latched condition. To prevent this, a relay contact does not supply the -6 VDC until the relay coil, operating from the +6 VDC, is energized. This insures that the +6 is up before the -6 in any power-on sequence.

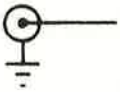
STANDARD DRAFTING SYMBOLS, ELECTRONIC

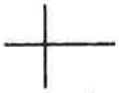

Connection to any given voltage.

Line ending at the edge of the sheet indicates continuance on another sheet.


Male pin or card edge contact.


Female pin, socket or card edge connector.

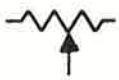

Coaxial connector.


No connection.


Connection.


Resistor, 1/4 W, ±5%, value in ohms (unless specified otherwise).

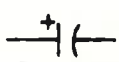

Resistor, 1/4W, ±1%, value in ohms (unless specified otherwise).

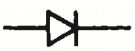

Resistor, variable, any type.

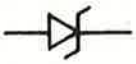

Resistor, variable, any type.

Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).


Capacitor, variable. Values in Picofarads (unless specified otherwise).


Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).

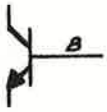

Diode, signal or rectifier.


Diode, zener.

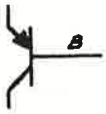

Diode, tunnel.


Diode, snap.

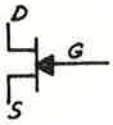

Light emitting diode (LED).



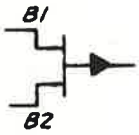
NPN Transistor.



PNP Transistor.



Field effect transistor, P Channel.



Field effect transistor, N.


Air choke.


Ferrite bead.


Ferrite core choke, Z 500 ohms when f > 60 MHz (unless otherwise indicated).


Ferrite core choke, 40 uH, (unless otherwise indicated).

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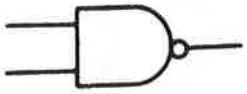
LeCroy Research Systems Corp.
Spring Valley, New York

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL).

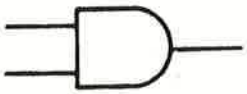
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

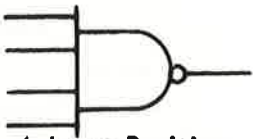
Supply voltages of IC's are shown in a table on each schematic.



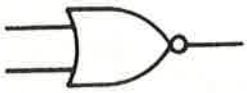
2-Input Positive NAND Gate



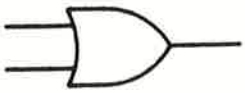
2-Input Positive AND Gate



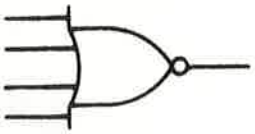
4-Input Positive NAND Gate



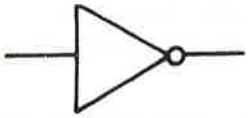
2- Input Positive NOR Gate



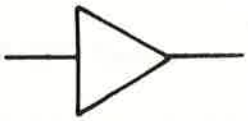
2 -Input Positive OR Gate



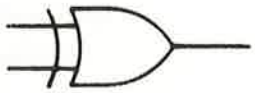
4-Input Positive NOR Gate



Inverter or Inverting Buffer



Non-Inverting Buffer

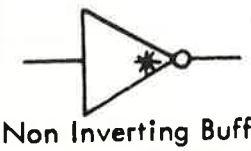


Exclusive OR Gate

Open collector outputs are identified by an asterisk (*) on the output connection.

2-Input Positive NAND Gate W/Open Collector

2-Input Positive OR Gate W/Open Collector



Non Inverting Buffer W/Open Collector

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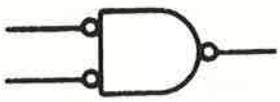
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS
EMITTER - COUPLED LOGIC (ECL)

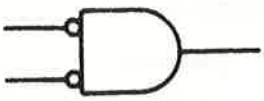
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

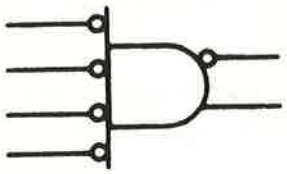
Supply voltages of IC's are shown in a table on each schematic.



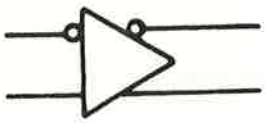
2 - Input Gate.
Negative AND (Positive OR) Gate.



2 - Input Gate.
Negative NAND (Positive NOR) Gate.

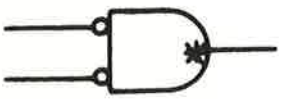


4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.

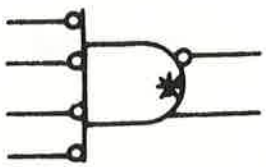


Differential
Amplifier.

Open emitter outputs are identified by an asterisk (*) on the output connection.



2 - Input Negative NAND Gate.
With Open Emitter.



A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.

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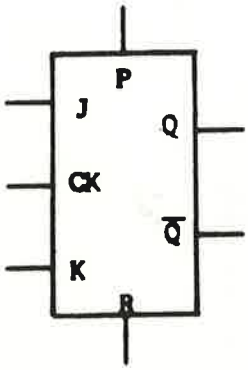
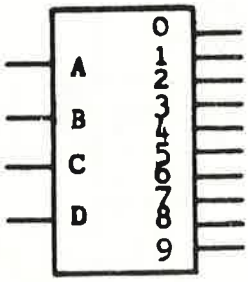
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS.
TRANSISTOR - TRANSISTOR LOGIC (TTL) OR
EMITTER COUPLED LOGIC (ECL).

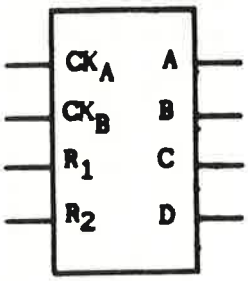
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave
Flip-Flop

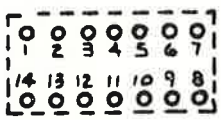


BCD-To-Decimal
Decoder-Driver

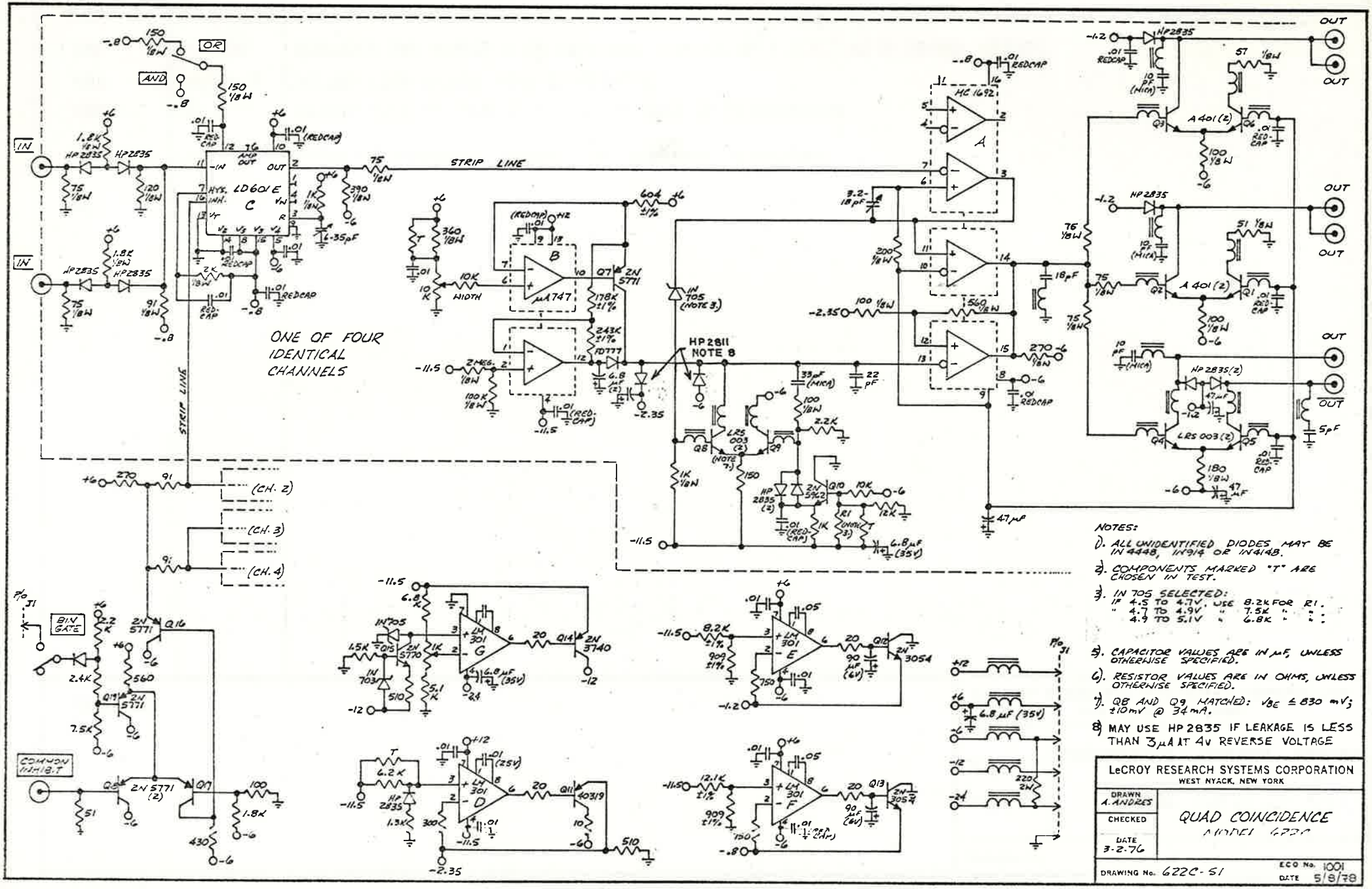


Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.



Bottom View


ONE OF FOUR IDENTICAL CHANNELS
STRIP LINE
HP2811 NOTE 8
(CH. 2)
(CH. 3)
(CH. 4)
COMMON INHIBIT
BIN GATE
NOTES:
1). ALL UNIDENTIFIED DIODES MAY BE IN4448, IN914 OR IN414B.
2). COMPONENTS MARKED "T" ARE CHOSEN IN TEST.
3). IN 705 SELECTED:
IF 4.5 TO 4.7V, USE 8.2K FOR R1.
" 4.7 TO 4.9V " 7.5K " " "
" 4.9 TO 5.1V " 6.8K " " "
5). CAPACITOR VALUES ARE IN μF, UNLESS OTHERWISE SPECIFIED.
6). RESISTOR VALUES ARE IN OHMS, UNLESS OTHERWISE SPECIFIED.
7). Q8 AND Q9 MATCHED: VBE ≤ 830 mV; ±10mV @ 34mA.
8) MAY USE HP 2835 IF LEAKAGE IS LESS THAN 3μA AT 4V REVERSE VOLTAGE
LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK
DRAWN A. ANDRES
CHECKED
DATE 3-2-76
QUAD COINCIDENCE
MODEL 622C
DRAWING No. 622C-S1
ECO No. 1001
DATE 5/8/78

ECO NO.	DATE	DESCRIPTION
197	6-29-76	REVISIONS TOSCHEMATIC, PARTS LIST AND ASSEMBLY DRAWING TO COMPLY WITH CHANGES TO PROTOTYPE. INCLUDES REINSTATING 3.2 - 18 pF CAPACITOR AT MC1692. PARTS LIST ONLY: HARDWARE CORRECTED, WIRES INCLUDED.
223	8-30-76	2 K RESISTOR ADDED TO REPLACE "T" RESISTOR AT LD601E, PINS 7 TO 15 (-.8V).
386	5-3-77	REPLACED TWO HP2835's ON RAMP BUS (PIN 13 OF I.C.A.) WITH HP2811 DIODES.
494	10-12-77	SILVER LEMO SIGNAL RING ELIMINATED
540	12-1-77	LAYOUT CHANGED FROM /B TO /C FOR EASE OF FABRICATION.
1001	5-8-78	CORRECTED SCHEMATIC (SHEET 1 OF SCHEMATIC AFFECTED).

REMARKS

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN	ENGINEERING CHANGE ORDERS
CHECKED	MODEL 622C
DATE	
DRAWING No.	