technical information manual

NIM Model 621L

Quad Discriminator

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the model type and serial number with all requests for parts or service.

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West Nyack, New York

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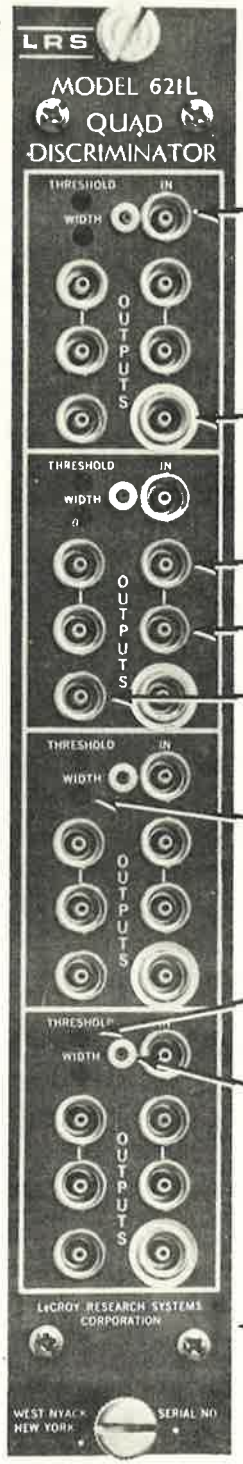
manual



NIM Model 621L

Quad Discriminator

50 Ω input, < 2% reflections.

1 complementary 50 Ω output
(quiescently, -16 mA; logical 1, 0 mA).

2 pairs bridged 50 Ω outputs
(quiescently, 0 mA; logical 1, -32 mA per pair).

1 normal 50 Ω output
(quiescently, 0 mA; logical 1, -16 mA).

Continuous width adjust, 5 ns to 1 us.

Threshold adjust, -30 mV to -1 volt;
stability, < 0.2%/°C.

Threshold monitor point; reads 10X
actual threshold.

Standard AEC/NIM packaging, in conformance
with AEC Report TID-20893, No. 1 width module.

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General Description

LRS Model 621L retains the format and operating features of particle physics' most widely used discriminator, the LRS Model 321BL. A new hybrid input stage provides substantial improvement in input characteristics: an almost perfect impedance match to eliminate reflections and consequent multiple-pulsing; a drift-free -30 mV threshold; overload protection to withstand outputs from even the most serious phototube malfunctions; virtually no input dc offset; and a new standard of compactness and reliability. A threshold monitor test point is provided on each channel to permit accurate and reproducible threshold settings using an external DC voltmeter.

Output durations are continuously adjustable from 5 ns to 1 us and are highly stable and independent of input amplitude, duration, and rate. Their long-term stability is excellent, permitting their direct use in critical coincidence applications without any need for external clipping cables. Each channel provides five standard amplitude negative NIM current source outputs and one complementary output. The resulting flexibility from this doubling of the output fan-out capability over previous circuits permits simpler and more efficient logic design. This greatly increased fan-out is achieved by means of a new output circuit design that utilizes very little quiescent power.

The -30 mV threshold offered by the Model 621L is almost a factor of two lower than that of the most sensitive previous circuits. It will permit experimenters to routinely reverse-terminate photomultiplier anodes. This procedure, coupled with the greatly improved input termination characteristics of the 621L, greatly reduces the possibility of multiple-pulsing due to reflections in the input system.

The pulse-forming circuit in the Model 621L is deadtimeless (updating), and the unit may be retriggered during the time an output from a previous input signal is being produced.

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Specifications

INPUT CHARACTERISTICS

Signal Input:	Threshold, - 30 mV to - 1 volt (continuously variable up to - 600 mV); front-panel screwdriver adjustment; screwdriver included; 50 Ω protected to ± 5 A for 0.5 us clamping at ± 7 V; direct-coupled; reflections < 2% for input pulses of 2 ns risetime; stability < 0.2%/°C over 20°C to 60°C operating range; offset 0 ± 1 mV; threshold monitor 10:1 ratio of monitor voltage to actual voltage.
Gate:	Slow gate via rear connector and rear panel ON-OFF switch; rise and fall times, approximately 50 ns; clamp to ground from + 5 inhibits; direct-coupled.

OUTPUT CHARACTERISTICS

Outputs:	Six, NIM; one positive (quiescently - 16 mA, 0 mA during output), two bridged negative (0 mA quiescently, - 32 mA during output); one negative (0 mA quiescently, - 16 mA during output).
Duration:	Continuously adjustable via front-panel screwdriver control from 5 ns to 1 us. Narrower minimum width possible at slight expense of amplitude. Stability better than ± .1%/°C.
Rise and Fall Times:	Less than 2.5 ns or 2 ns typical all outputs, 10% to 90%. Output falltimes slightly longer on wide output durations.

GENERAL

Maximum Rate:	120 MHz typical, input and output.
Double Pulse Resolution:	Less than 8 ns.

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Time Slewing:	1 ns for input amplitudes 110% of threshold and above.
Input-Output Delay:	9.5 ns typical.
Multiple Pulsing:	None; one and only one output pulse of preset duration is produced for each input pulse, regardless of input pulse amplitude or duration.
Packaging:	In RF-shielded AEC/NIM No. 1 module; Lemo-type connector
Power Requirements:	-6 V at 460 mA; +6 V at 120 mA; -12 V at 170 mA; +12 V at 20 mA. OPTIONAL, at slight additional cost, internal power supply operating from 120 VAC to eliminate ±6 V requirement; +12 V at 140 mA; -12 V at 170 mA; and 120 VAC at approximately 50 mA.

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Circuit Description

Each of the four channels of the Model 621 is composed of three basic sections: the input and discriminator stage, the timing or pulse-former stage, and the output stage. A block diagram of the Model 621 can be seen in Figure 2, and a complete schematic can be found at the end of this manual.

The input and discriminator stage is based on the LRS Model LD601 hybrid. This unit contains all of the circuitry of the discriminator with the exception of the input termination and high voltage protection. The latter two functions are self-explanatory in the schematic, and the LD601 is functionally presented in Figure 1. The threshold level is set by changing the voltage bias on a fast differential amplifier which has a small

FUNCTIONAL BLOCK DIAGRAM
LD601 DISCRIMINATOR HYBRID

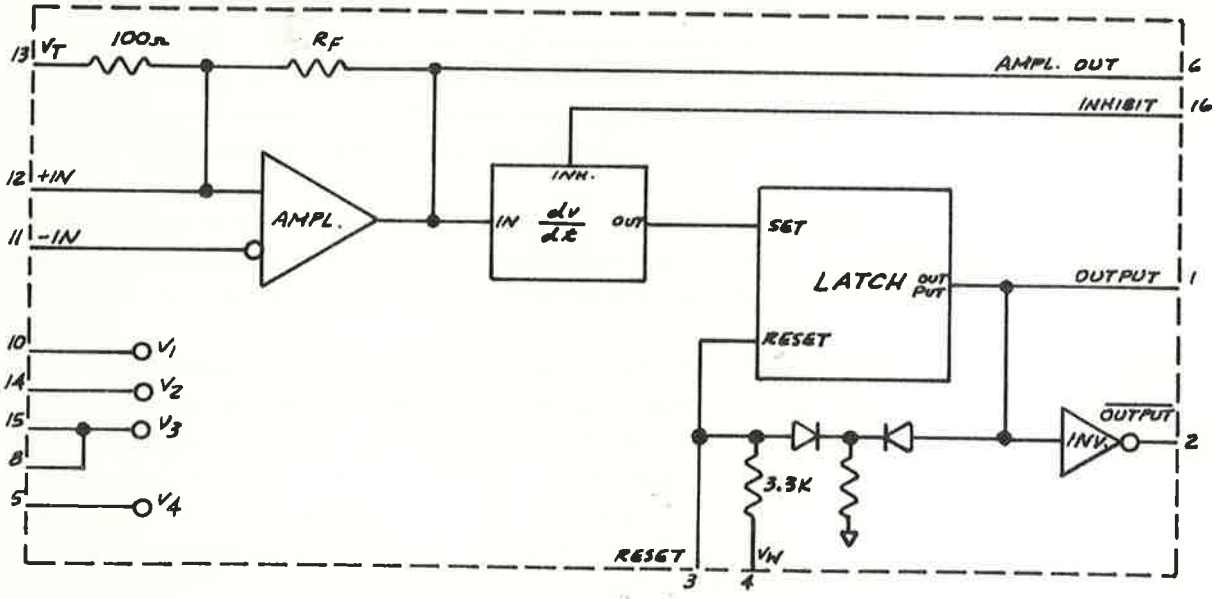

FIG. 1

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amount of positive feedback to provide regeneration at threshold. In actual operation, the V_T input is grounded, and the threshold level is determined by the 10:1 voltage divider (composed of the external 909 Ω and internal 100 Ω resistors) operating from a voltage which is set by a front-panel potentiometer and monitored at the front-panel test point. The measured voltage will be 10 times the actual threshold voltage. When an input signal applied to the -IN is equal to the threshold voltage at the +IN, the amplifier output will begin to go positive. This will force the +IN closer to 0 volts, which increases the differential input voltage in such a direction that the output locks up. It will stay in this mode until the input signal falls below the level on the +IN, and then the cycle reverses. The actual amplifier output provides a time-over-threshold pulse with fixed amplitude. This pulse can be monitored at the AMPL. OUT (pin 6) point. Its quiescent level should be nominally -2.4 volts going to -1.6 volts during the pulse. The leading edge of this output will set a latch circuit which is used as a pulse width standardizer. Before the latch can be set, the inhibit input (used for the bin gate) must be off. At pin 16 of the LD601 the required levels are 0 to -1.6 volts enables; -2.5 to -6 volts inhibits. (The common bin gate driver shifts this so that 0 volts at the Bin Gate input will inhibit, greater than +3 volts will enable.) Once the latch is set, a latch OUTPUT is available to start the 621 timing stage. The OUTPUT amplitude should be similar to the AMPL. OUT above, but the width will be fixed independent of the input width. Internally, the latch output is fed back to reset the latch after a short time delay, thus generating a short output pulse whose actual width can be set by the proper external selection of RC time constant and voltage levels at pins 3 and/or 4. It is set at approximately 3 ns in the Model 621.

There are two trim resistors associated with this stage. T1 sets the minimum width as measured at the test point, and T2 calibrates the LD601 to its respective channel. If the LD601 is changed, T2 will probably require retrimming.

The timing or pulse-forming stage of the Model 621 utilizes three stages of MC1692 for amplifying and shaping. The actual timing is done by first charging a 33 pfd capacitor with the pulse from the LD601 (via one MC1692 stage and the differential stage composed of Q3 and Q4) until it is clamped by the HP2800 diode to a voltage set indirectly by the front-panel width potentiometer (via two stages of 747)). The discharge rate is set by the current source stage composed of the width potentiometer, one stage of 747, Q2 and the 604 Ω emitter resistor on Q2, where the actual current is varied from near zero (for the maximum 1 us width) to about 10 mA (for the minimum 5 ns width). Thus, simultaneously, as the width is increased, the clamp voltage is increased (allowing more initial charge to

be stored on the timing capacitor) and the current is decreased (reducing the rate of discharge), thus multiplying the effect of the width control. The effect of Q5 and the diodes associated with it are to provide fast recovery of the timing capacitor. The 1692 ECL amplifiers are interconnected in a manner to provide stable leading edge timing and fast rise and fall times of the output pulse. The first amplifier (output pin 3) provides final shaping and standardization of the pulse from the LD601 to the timing stage, as well as driving the output stage directly via a second 1692 amplifier (output pin 14). This provides a prompt output pulse for the duration of the 601 output, independent of the delay encountered in initializing the timing stage. Before the 601 output is over, the timing capacitor is charged, causing the third 1692 amplifier (output pin 15) to now maintain the pulse level to the output stage (using emitter ORing) until the timing capacitor subsequently discharges to a sufficiently low level (approximately -2.0 volts). At this point (because of regeneration) the third amplifier promptly switches back to its quiescent off condition, terminating the output pulse.

The output stages utilize two different types of circuits. The single normal and complementary outputs use a conventional differential stage. This stage requires a continuous 16 mA of current which is quiescently available at the complementary output connector via Q9. During an output pulse, the 1692 will switch from the quiescent level of -2.4 volts to a higher level of -1.6 volts, causing Q8 to conduct, switching the 16 mA current from the complementary to the normal output connector for the duration of the pulse. The other two pairs of outputs each supply 32 mA of current during the pulse, because at this time the bases of Q6 and Q7 are at -1.6 volts; therefore, the emitters are at about -2.4 volts. This places about 600 mV across each 18 Ω emitter resistor, and the resulting 32 mA will be available at each output connector pair for the duration of the pulse. Quiescently, Q6 and Q7 bases are at -2.4 volts; therefore, there is only -600 mV drop available for V_{BE} so the transistors are off, resulting in a substantial power saving. All outputs are diode clamped so they will provide proper operation even without output loads. Without a path for the current during the pulse, even on a single output stage, the current would have to be supplied via the transistor base, which would severely load the driver and not allow proper drive to the remaining stages.

Three internal power supplies are used to generate the -0.8, -2.2, and -3.0 special bias voltages used by the four channels. Operation of these supplies is simple. A 741 operational amplifier is used to maintain the output voltage of a series-pass transistor equal to a reference voltage. The -3 volt supply includes two diodes to temperature-compensate for the 1692 output and the Q6-Q7 output transistor V_{BE}.

If the -6 voltage is sequenced on before the +6 voltage, the LD601 may be forced into a DC latched condition. To prevent this, a relay contact does not supply the -6 VDC until the relay coil, operating from the +6 VDC is energized. This insures that the +6 is up before the -6 in any power-on sequence.

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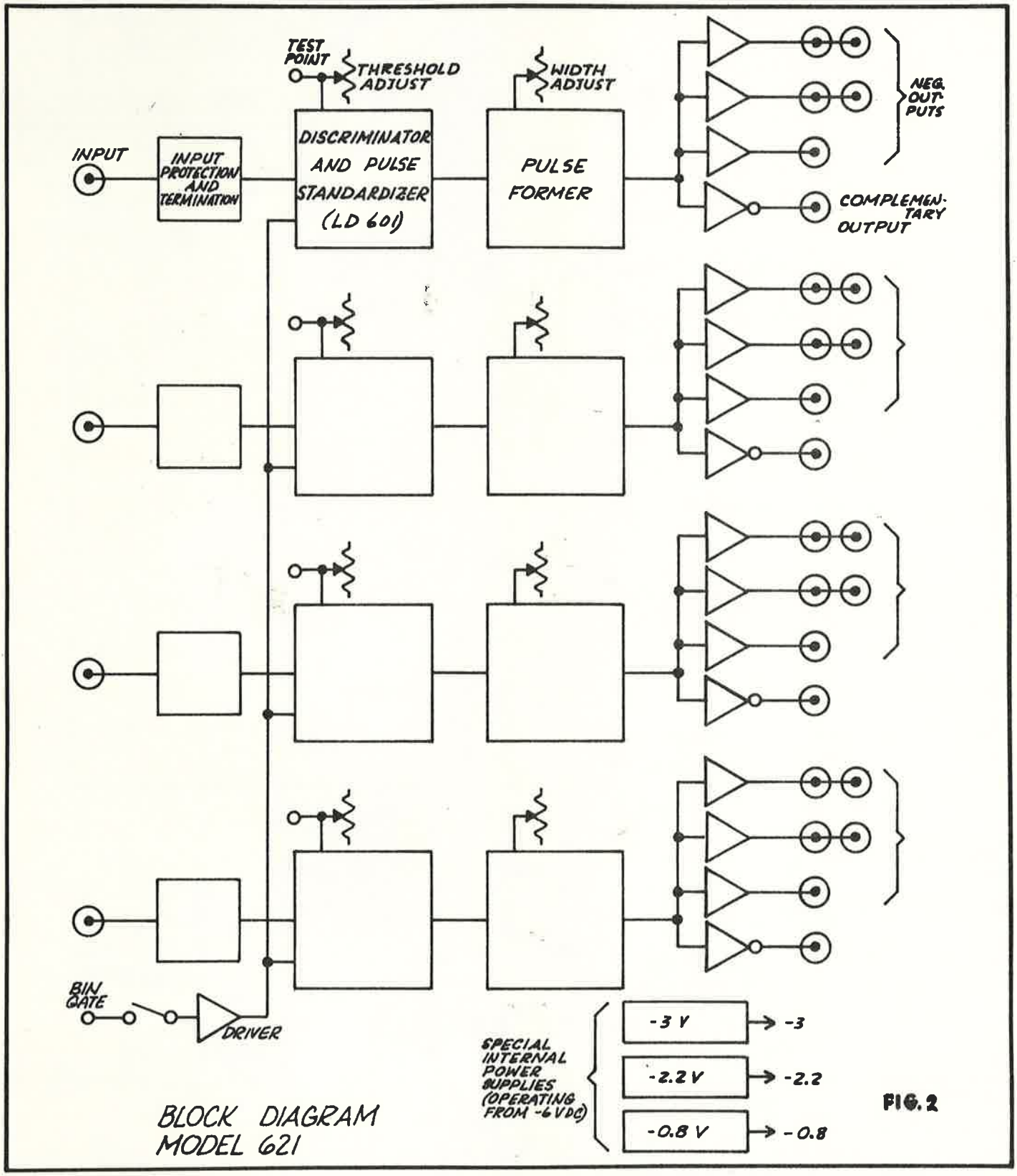

BLOCK DIAGRAM
MODEL 621

FIG. 2

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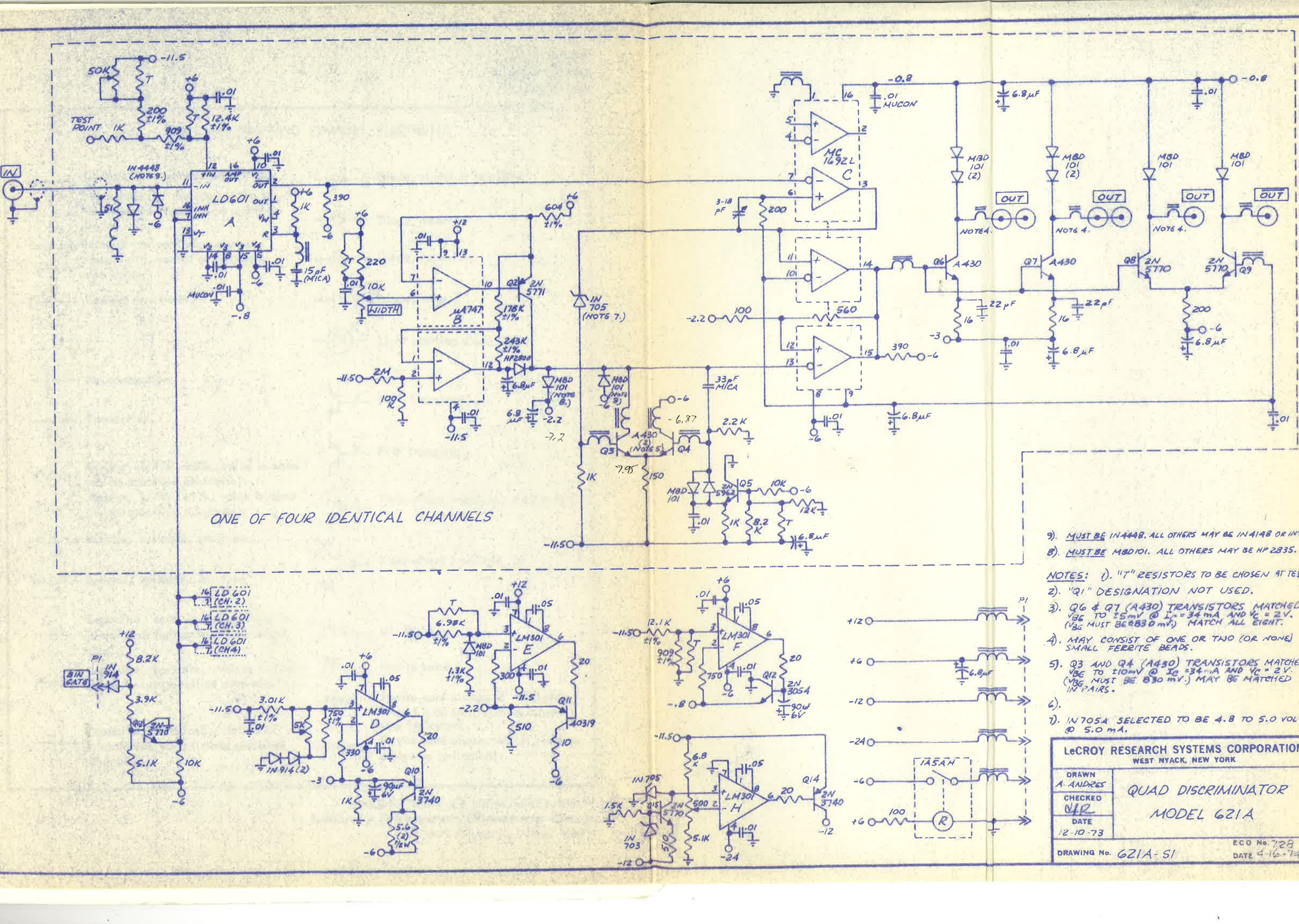


9). MUST BE IN4448. ALL OTHERS MAY BE IN4148 OR IN914.

8). MUST BE MBD101. ALL OTHERS MAY BE HP 2835.

NOTES: 1). "T" RESISTORS TO BE CHOSEN AT TEST.

2). "Q1" DESIGNATION NOT USED.

3). Q6 & Q7 (A430) TRANSISTORS MATCHED: V_{BE} TO 15mV @ I_C = 34 mA AND V_C = 2V. (V_{BE} MUST BE ≤830 mV.) MATCH ALL EIGHT.

4). MAY CONSIST OF ONE OR TWO (OR NONE) SMALL FERRITE BEADS.

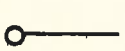
5). Q3 AND Q4 (A430) TRANSISTORS MATCHED: V_{BE} TO 10mV @ I_C = 34 mA AND V_C = 2V. (V_{BE} MUST BE 830 mV.) MAY BE MATCHED IN PAIRS.

6).

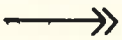
7). IN 705A SELECTED TO BE 4.8 TO 5.0 VOLTS @ 5.0 mA.

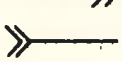
LeCROY RESEARCH SYSTEMS CORPORATION WEST NYACK, NEW YORK	
DRAWN A. ANDRES	QUAD DISCRIMINATOR
CHECKED NJR	MODEL 621A
DATE 12-10-73	
DRAWING No. 621A-51	ECO No. 728 DATE 4-16-74

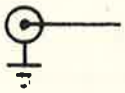
STANDARD DRAFTING SYMBOLS, ELECTRONIC

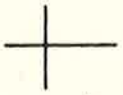

Connection to any given voltage.

Line ending at the edge of the sheet indicates continuance on another sheet.


Male pin or card edge contact.


Female pin, socket or card edge connector.

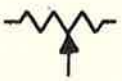

Coaxial connector.

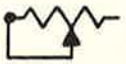

No connection.


Connection.

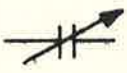

Resistor, 1/4 W, ±5%, value in ohms (unless specified otherwise).

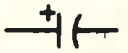
Resistor, 1/4W, ±1%, value in ohms (unless specified otherwise).

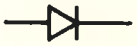

Resistor, variable, any type.

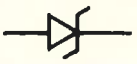

Resistor, variable, any type.

Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).


Capacitor, variable. Values in Picofarads (unless specified otherwise).

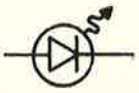

Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).


Diode, signal or rectifier.


Diode, zener.

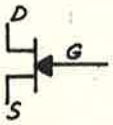

Diode, tunnel.


Diode, snap.

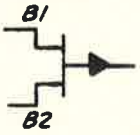

Light emitting diode (LED).

NPN Transistor.

PNP Transistor.



Field effect transistor, P Channel.



Field effect transistor, N.


Air choke.


Ferrite bead.


Ferrite core choke, Z 500 ohms when f ≥ 60 MHz (unless otherwise indicated).


Ferrite core choke, 40 uH, (unless otherwise indicated).

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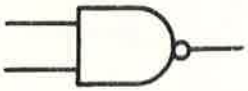
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL).

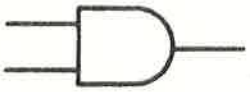
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

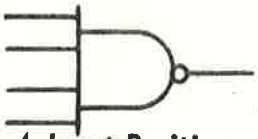
Supply voltages of IC's are shown in a table on each schematic.



2-Input Positive NAND Gate



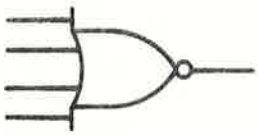
2-Input Positive AND Gate



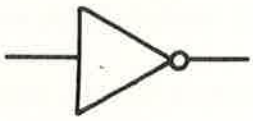
4-Input Positive NAND Gate

2- Input Positive NOR Gate

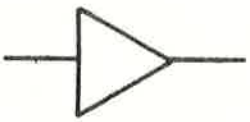
2 -Input Positive OR Gate



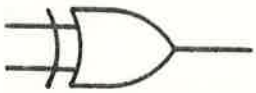
4-Input Positive NOR Gate



Inverter or Inverting Buffer

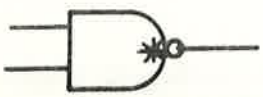


Non-Inverting Buffer



Exclusive OR Gate

Open collector outputs are identified by an asterisk (*) on the output connection.



2-Input Positive NAND Gate W/Open Collector

2-Input Positive OR Gate W/Open Collector

Non Inverting Buffer W/Open Collector

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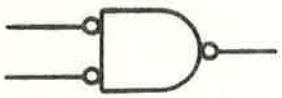
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS EMITTER - COUPLED LOGIC (ECL)

The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

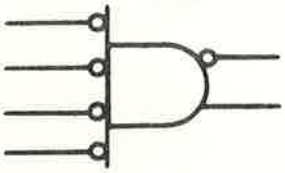
Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

Supply voltages of IC's are shown in a table on each schematic.

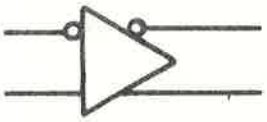


2 - Input Gate.
Negative AND (Positive OR) Gate.

2 - Input Gate.
Negative NAND (Positive NOR) Gate.

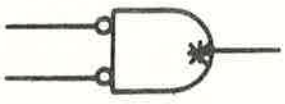


4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.

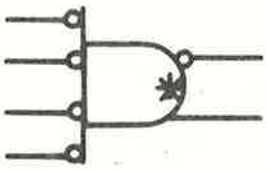


Differential
Amplifier.

Open emitter outputs are identified by an asterisk (*) on the output connection.



2 - Input Negative NAND Gate.
With Open Emitter.



A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.

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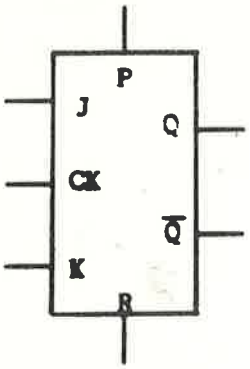
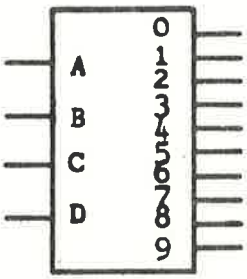
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL) OR EMITTER COUPLED LOGIC (ECL).

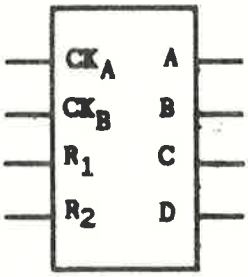
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave Flip-Flop



BCD-To-Decimal Decoder-Driver



Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.

Bottom View

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