technical information manual

NIM 620 Series

8-Channel Discriminator
620BL, 620BLP, 620CL

Project Engineer: B. Yamrone
Operations: A. Michalowski
August, 1977

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

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LeCroy Research Systems Corp.
Spring Valley, New York

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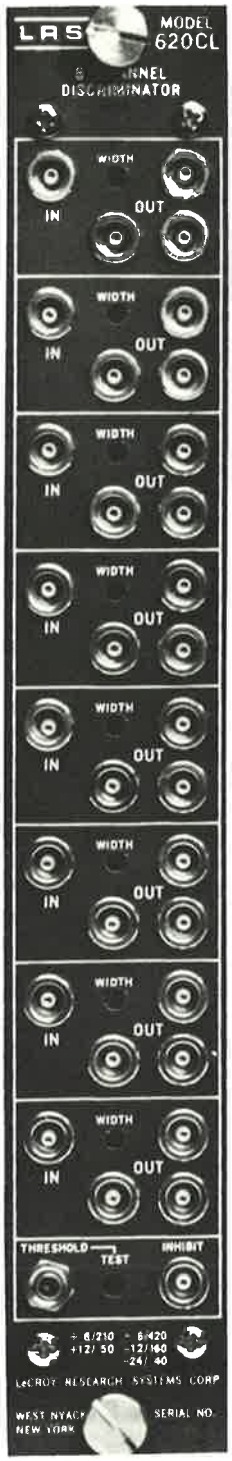
TECHNICAL DATA

LeCroy



NIM Model 620CL

8-Channel Discriminator

With Veto

The LRS Model 620CL, a new, non-updating, 100 MHz octal discriminator, ideal for hodoscope and other applications, is similar in design and performance to the widely-used Model 620AL. Utilizing the same hybrid circuit front end as most other LRS discriminators (the LD601 Series), the 620CL offers input reflection characteristics (<4%) still unmatched by other commercially available discriminators and an excellent reliability record based upon active field use of a significant number of the same front-end hybrid during the past few years.

The 620CL offers eight independent channels of discriminator, the thresholds of which are commonly variable from −30 mV to −1 volt via a front-panel, screwdriver-adjustable potentiometer (screwdriver included). A front-panel threshold monitor point permits accurate determination of threshold setting with a DC voltmeter. The stability of the threshold is < 0.2%/°C to assure accurate results in varied operating environments.

The outputs of the 620CL are low-impedance voltage outputs providing output levels greater than −800 mV into a 50 Ω load. The output durations are independently presettable via front-panel screwdriver adjustment from 5 ns to greater than 20 ns. Output risetimes and falltimes are less than 2.5 ns.

In slight difference to the original 620AL, the Model 620CL has a built-in front-panel fast veto input which permits all channels in common to be inhibited for the duration of the veto signal. Veto must overlap the leading edge of the signal to be inhibited and must precede it by approximately 5 ns.

The 620CL is packaged in an RF-shielded NIM #1 width module utilizing Lemo-type connectors. Power dissipation is approximately 6.6 watts and current usage is within the limits supplied by a standard NIM crate, permitting the use of 12 modules (96 channels) per bin.

November, 1975

Innovators In Instrumentation

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3. ADDENDA TO SPECIFICATIONS

None.

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4. OPERATIONAL DESCRIPTION

4a. Input Characteristics

Threshold Range: The threshold range of the Model 620 series Quad Discriminators is -30 mV to -1 volt. Because the front panel screwdriver adjustable potentiometer gets more and more sensitive as the threshold is increased, it eventually reaches a point (approximately -600 mV) beyond which it becomes difficult to set. Thus, beyond the -600 mV level it should be assumed that the discriminator will attain its maximum threshold setting of -1 volt with almost negligible additional turning of the pot.

The low minimum threshold of the Model 620 series units makes it possible to use lower gain photomulitpliers, lower high voltage in the phototubes, and to drive PM signals over longer cable lengths than would be possible with higher thresholds. Compared with a -50 mV discriminator, for instance, utilizing RG-58 cable, the -30 mV discriminator would permit cable runs 66.7 feet longer than those permitted by a -50 mV discriminator for equal amplitude pulses. In addition, the low minimum threshold helps make it possible for one to back-terminate at the photomultiplier to absorb reflections and high amplitude noise. (In this case, the PM drives 25 Ω, the tube current is shared, and the amplitude is half that of the unterminated system.)

Threshold Uncertainty: While most people consider the threshold of a discriminator to be that value which is written on a spec sheet or determined by a front panel pot, in reality the actual value not only varies from channel to channel, but can be a strong function of other environmental conditions. The external factors with the strongest effect upon the threshold value are the temperature coefficient of threshold and the power supply coefficient of threshold. Combining these, the actual threshold value V_T is given by:

V_T= Threshold according to front panel control setting ± dc offset ± temperature coefficient X temperature change from calibration temperature ± supply coefficient X voltage change from calibration voltage.

Threshold Memory: In order for an experimenter to be assured of a well defined threshold value, it must be independent of the

The figure below indicates the total threshold uncertainty of the 620 Series Discriminators.

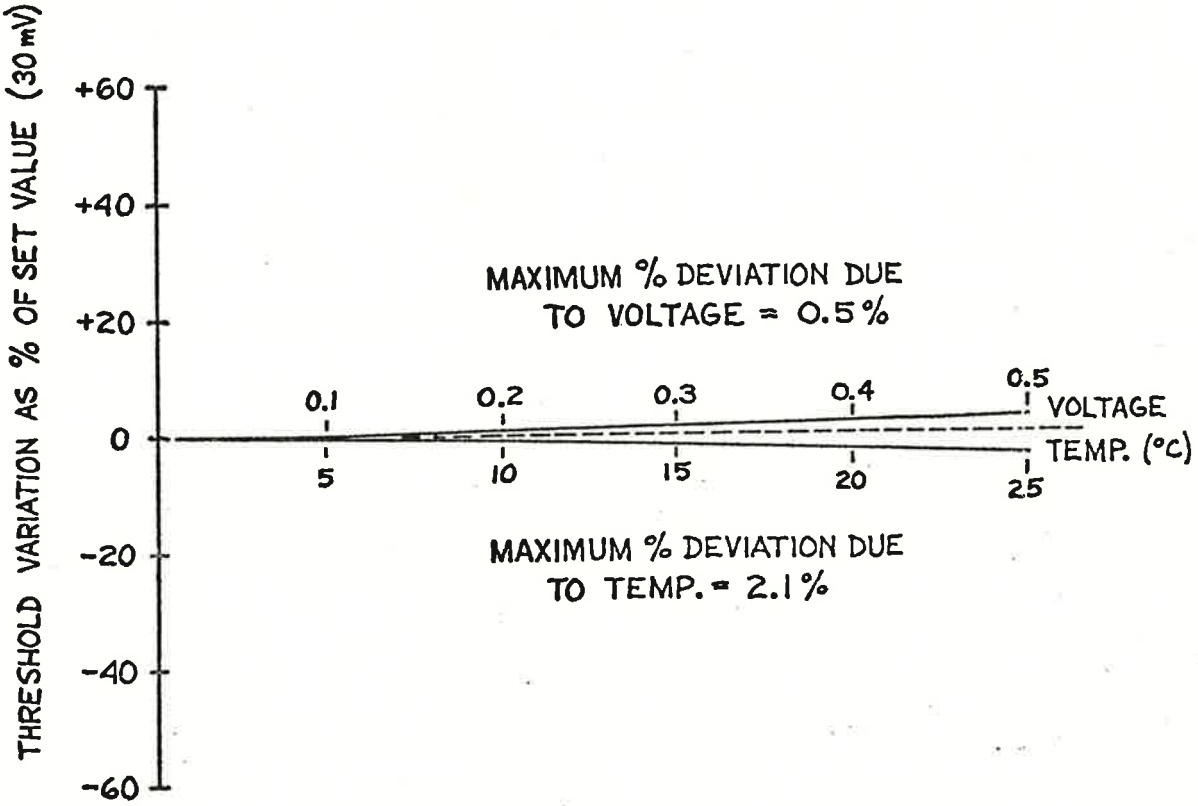

FIGURE 1

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typical conditions encountered in its use. While one does not expect large changes in basic pulse shape, etc., a discriminator does experience all varieties of pulse pair separation. If a discriminator's threshold is affected by previous events, it is said to have threshold memory. To the experimental physicist, this is additional threshold uncertainty, since the discriminator's threshold for any given event depends upon the elapsed time from the preceding threshold crossing. In most discriminators, threshold memory (or second pulse sensitivity) becomes much larger as the pulse separations are reduced. The effect can be further aggravated by the amplitude of the preceding signal, so much so with some circuits, that an overload or noise pulse can effectively paralyze the discriminator for threshold level signals for 10's of nanoseconds following the overload.

Note that in figure two the threshold for the second pulse is 6% for all spacing wider than 9 nsec. The second graph (i.e., the one more favorable to the descriminator) shows exceptionally clear response with virtually no effect in evidence above 10.5 nsec.

Threshold Calibration: Determination of the input threshold set by the front panel control has typically required the experimenter to calibrate each change in setting with an external pulse source and oscilloscope. Newer discriminators offer a front panel test point whose dc level is proportional to the actual discriminator threshold. Not only does this allow rapid and simple determination of threshold, but it also allows the experimenter to easily return the threshold level to a previously recorded setting. The convenience, and therefore the usefulness, of this feature is strongly dependent upon the characteristics of this monitor voltage, particularly its linear proportionality with the threshold setting. Figure 3 indicates the characteristic curve for the LeCroy Model 620 series discriminators.

4b. 620 Series Threshold Hysteresis

In standard Model 620 series discriminators, hysteresis is built into the front end, such that every threshold crossing will not trigger the discriminator unless the previous signal has returned to below approximately -15 mV. This avoids multiple pulsing due to, for example, fine structure riding on a flat-topped pulse that may bring the pulse above and below threshold. See figure 4.

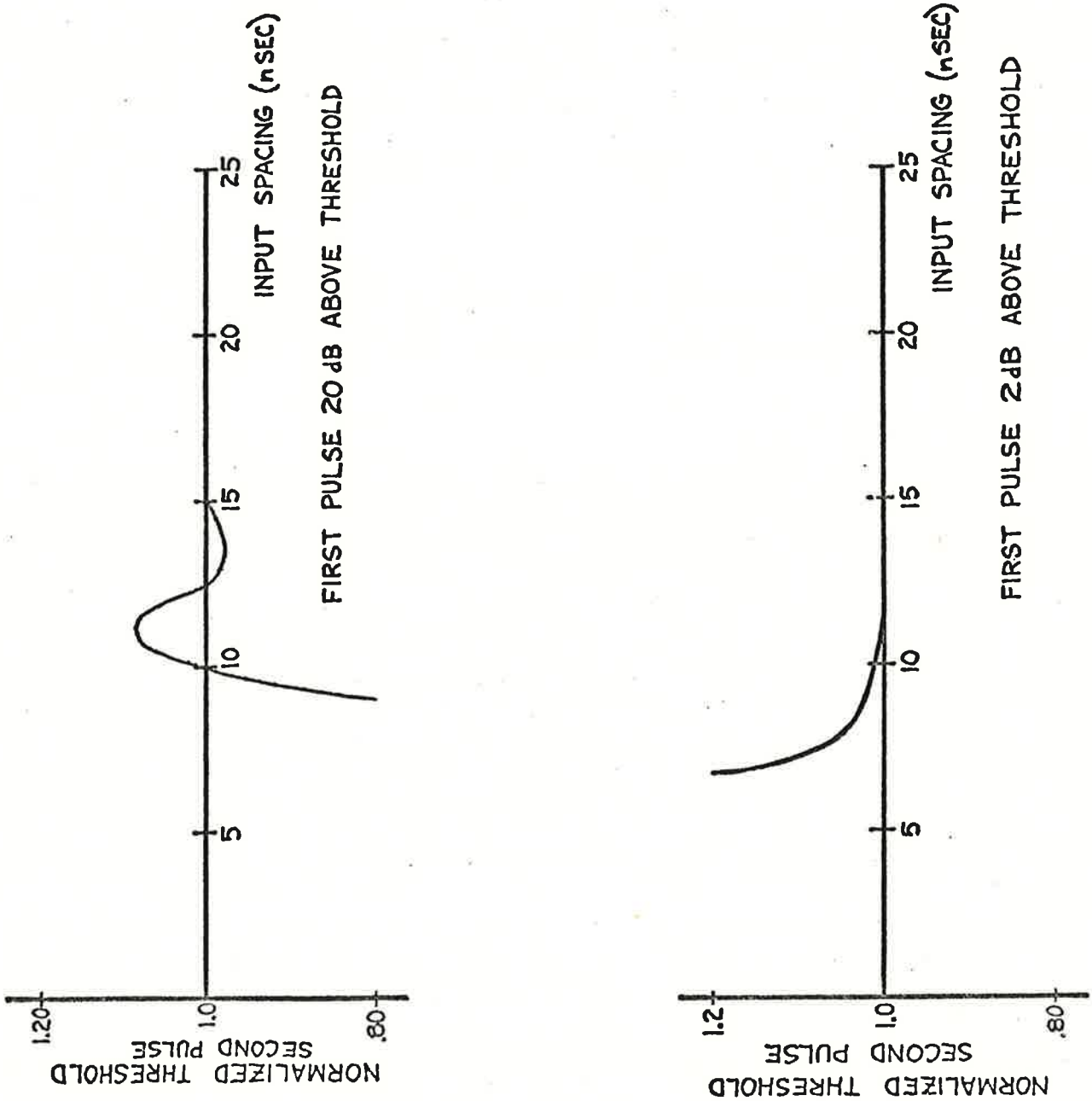

FIGURE 2

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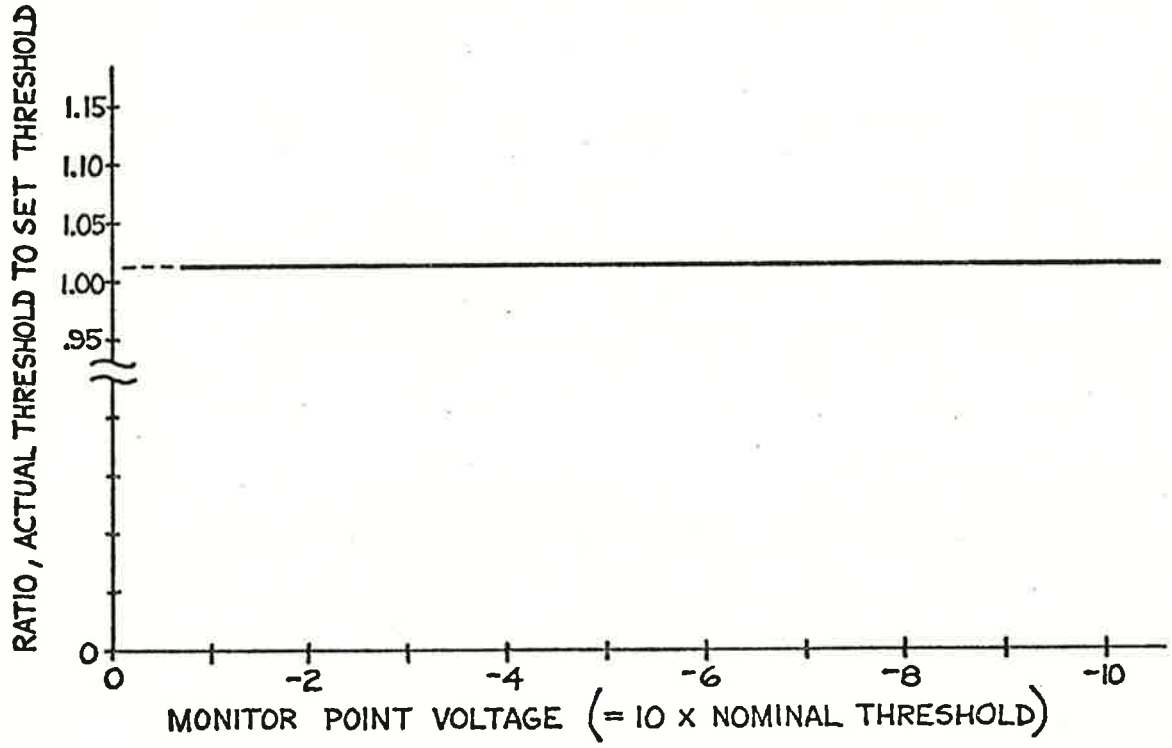

FIGURE 3

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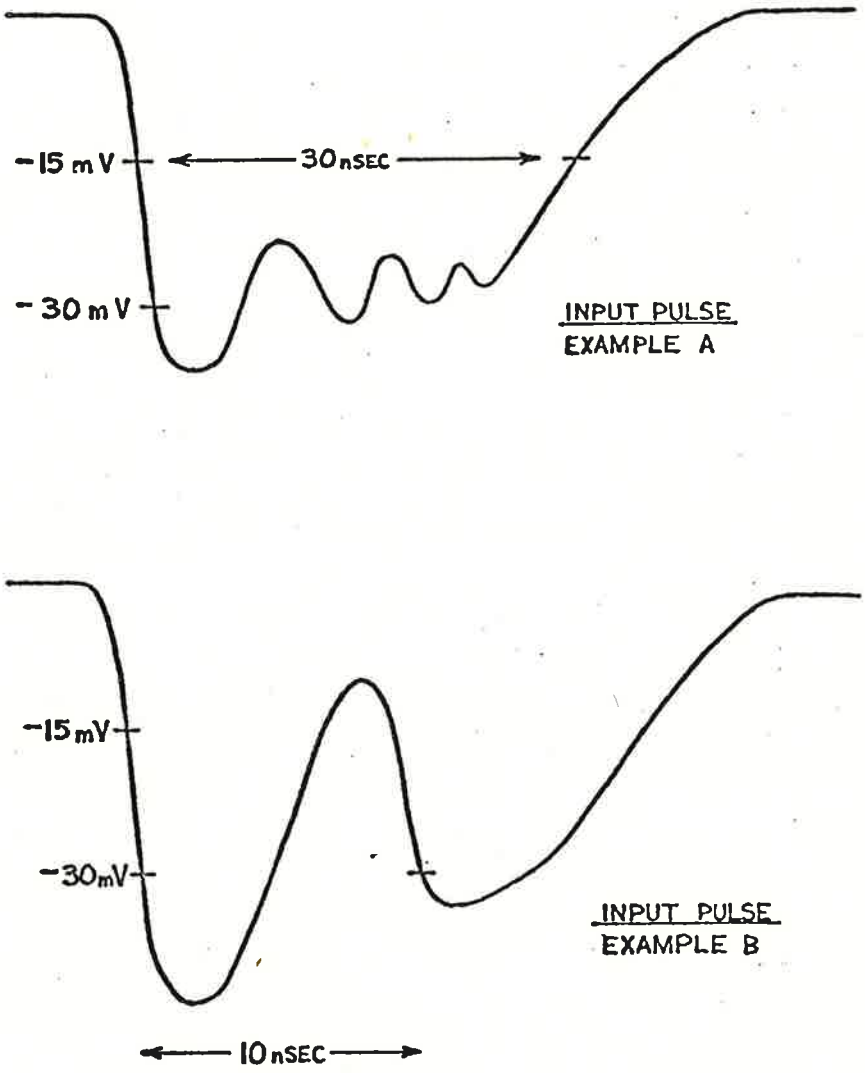

FIGURE 4

In Example A, the pulse shape variations of the input pulse will not re-trigger the discriminator even though they cross the threshold level at a time exceeding the DPR of the unit. In Example B, since the input signal does go back through -15 mV and then once again rises to exceed the -30 mV threshold level, two discriminator outputs would result. Since LeCroy discriminators are most often used with photomultipliers and plastic scintillators, and since the characteristic pulses out of this type detector are typically smooth for each individual event, multiple outputs should only occur when they represent multiple events.

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4c. Input Reflections

Input reflections probably account for the majority of multiple-pulsing problems encountered in an experiment. As discriminator thresholds have become lower, the amount of reflected signal required to retrigger the unit has decreased accordingly. Unless the percentage of input reflections is reduced along with the minimum threshold value, the experimenter finds himself in the situation where multiple-pulsing negates the usefulness of lower threshold. The input reflections of a discriminator effectively determine the allowable dynamic range of event or noise input signals.

On the experimental floor, a limited dynamic range may mean that minimum threshold values will have to be set higher to prevent multiple-plusing on noise or large (shower) event signals. In addition, high input reflections also limit the ability of a discriminator to be used to restandardize logic signals which have been degraded by long cables.

Figure 5 shows the maximum input voltage and allowable dynamic range as a function of discriminator input reflections.

As is evident the 620 series discriminators offer a dramatic improvement in input reflection suppression over previously available discriminators. Because of the extremely low reflection coefficient of the 620's (i.e., <2% for inputs of risetime ±2 nsec), maximum input signal is more than a volt larger than it would be for a unit exhibiting the typical 10% reflections, offering five times increase in the discriminators' dynamic range.

4d. Input Protection

The inputs of the Model 620 series discriminators are protected to 5 A for 0.5 μsec, clamping at +1 and -7 volts.

The DC protection is limited by the 0.25 watt dissipation limit of the input resistor, which can be assumed to offer protection against DC signals between -5 volts and +5 volts.

4e. Bridged High Impedance Input Option

The Model 620 series modules are offered with bridged high impedance input options. Although other models have been supplied occasionally

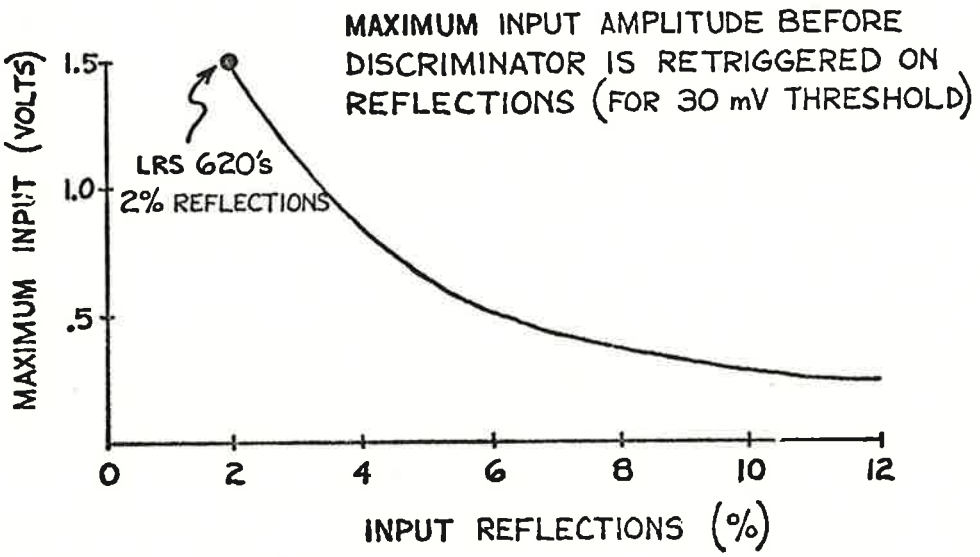

FIGURE 5

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with this option in the past by special request. The bridged high impedance inputs permit a user to drive one cable only from the photomultiplier to the discriminator to permit subsequent fast logic decision and pattern recognition to be performed. A popular method in the absence of this discriminator input option is to run two cables, one of which is from the dynode, which then must be inverted before the ADC or discriminator could accept it.

For this bridged input option, the left bottom output connector is generally sacrificed. The wire normally feeding this cable is tied to 50 Ω to provide the correct impedance to the driver. A silver colored ring is placed around this connector (as well as around the original input connector) when the unit is modified for this option to signify the fact that there are now two input connectors. In standard usage, the silver colored ring usually specifies complementary output.

4f. Inhibit Input (620 CL Only)

The Model 620CL provides an inhibit function to inhibit all eight channels. The input impedance is 50 Ω and requires an input pulse with a negative amplitude equal to or greater than 600 mV (standard NIM level pulse). To ensure proper operation when inhibiting, the inhibit input pulse must overlap the leading edge of the input signal (to be inhibited) and must precede it by 5 nsec. When in its time state, the inhibit driver will inhibit the dv/dt section of the LD601 (see the Functional Block Diagram), it will not inhibit the input amplifier on the hybrid.

4g. Output Characteristics

Low Impedance Voltage Output: The Model 620 series discriminator both require only one output driver (for 3 outputs)per channel. This driver requires no quiescent current, thereby permitting extremely small average power dissipation while still providing fast output response time. The output amplitude,although somewhat dependent on the number of output loads, will always be more negative than -800 mV in the logic "1" state.

The low impedance voltage output stage response times will be optimum when driving at least two 50 Ω loads.

Summing Output (620 BL Only): The summing output (unlike the low

impedance voltage output) provides a relatively high impedance output. It provides a -2 mA amplitude pulse for each channel that is in the logic "1" condition. Since the summing output is obtained by a diode or gate, it is not a true current source output, and therefore should not be wire-OR'ed with other summing outputs.

The output shape and response times can be optimized by loading at least two of the three outputs on each channel that will provide current to the summing outputs.

4h. Non-Updating Operation

The LeCroy Model 620 series discriminators are non-updating. In a non-updating discriminator the output will not be extended if a second pulse comes in before the first output returns to zero. The second pulse will not be run by the discriminator.

4i. Timing Characteristics

Maximum Rate: Maximum CW rate capability of the 620 series discriminators is guaranteed at 100 MHz. Typically, the maximum rate is 110 MHz, with some units being capable of operation up to 120 MHz for small bursts of input pulses.

Double Pulse Resolution: The speed of a discriminator is practically defined by its double pulse resolution or the line between the leading edges of the most closely spaced pulse pair to which the discriminator produces two distinct output pulses. Although simple in concept, this specification can be misleading unless the input conditions are precisely defined and ambiguities in performance are disclosed. Characteristic curves which more adequately describe double pulse resolution are indicated and discussed below and in figure 6.

Double Pulse Resolution VS. Input Amplitude: The double pulse resolution of some discriminators is a strong function of the amount of overdrive. Typical anomalies include substantial increases in amplitude to achieve minimum pulse pair resolution (which is an effective threshold increase as a function of rate) and/or limited input dynamic range over which the discriminator adheres to specifications. A third effect is equivalent to tracking error. Does

a discriminator have 8 nsec DPR if it never produces output pulses spaced more closely than 10 nsec apart? In some cases this effective timing error can be much larger than time shift due to intrinsic slewing or risetime dependent slewing. Figure 6 shows the minimum double pulse resolution of the LeCroy Model 620 series discriminators as a function of input amplitude from threshold to 10X threshold.

It is worth noting that the 620's maintain a DPR of under 9 nsec for all inputs over the 10:1 dynamic range. Although not featured as part of the general specifications, the double pulse resolution is much better than specified over most of the measured dynamic range. Also significant is the absence of tracking error at the limit of the discriminator's input performance. Throughout the measured range, the time shift of the output averages 2.54% or approximately 200 psec.

Double Pulse Resolution VS. Input Width: The DPR of a discriminator is a strong function of the duration of the first pulse in an input pair, since this width affects the recovery time allowed the discriminator input stage between the two pulses. If the double pulse resolution is not linear with input width, it may mean that the discriminator may not respond to the second pulse following an overload photomultiplier signal. The double pulse resolution VS. input width of the Model 620 series discriminators is shown in figure 7.

4j. Tracking Error

The ability of a discriminator to be used for precise timing (coincidence or TOF) in an environment which encounters narrow pulse pair separations is demonstrated by considering the time shift (or tracking error) introduced as the time interval between successive inputs is reduced. In an experiment, tracking error is equivalent to time dispersion as a function of input rate. For many experiments, this can be critical, since it is often in high rate situations that the best timing resolution is required.

Tracking error of the Model 620 series discriminators as a function of input pulse spacing is indicated in figure 8. Note that the tracking error assumes the shape of a damped oscillation which decays to zero at several times the unit's minimum double pulse resolution.

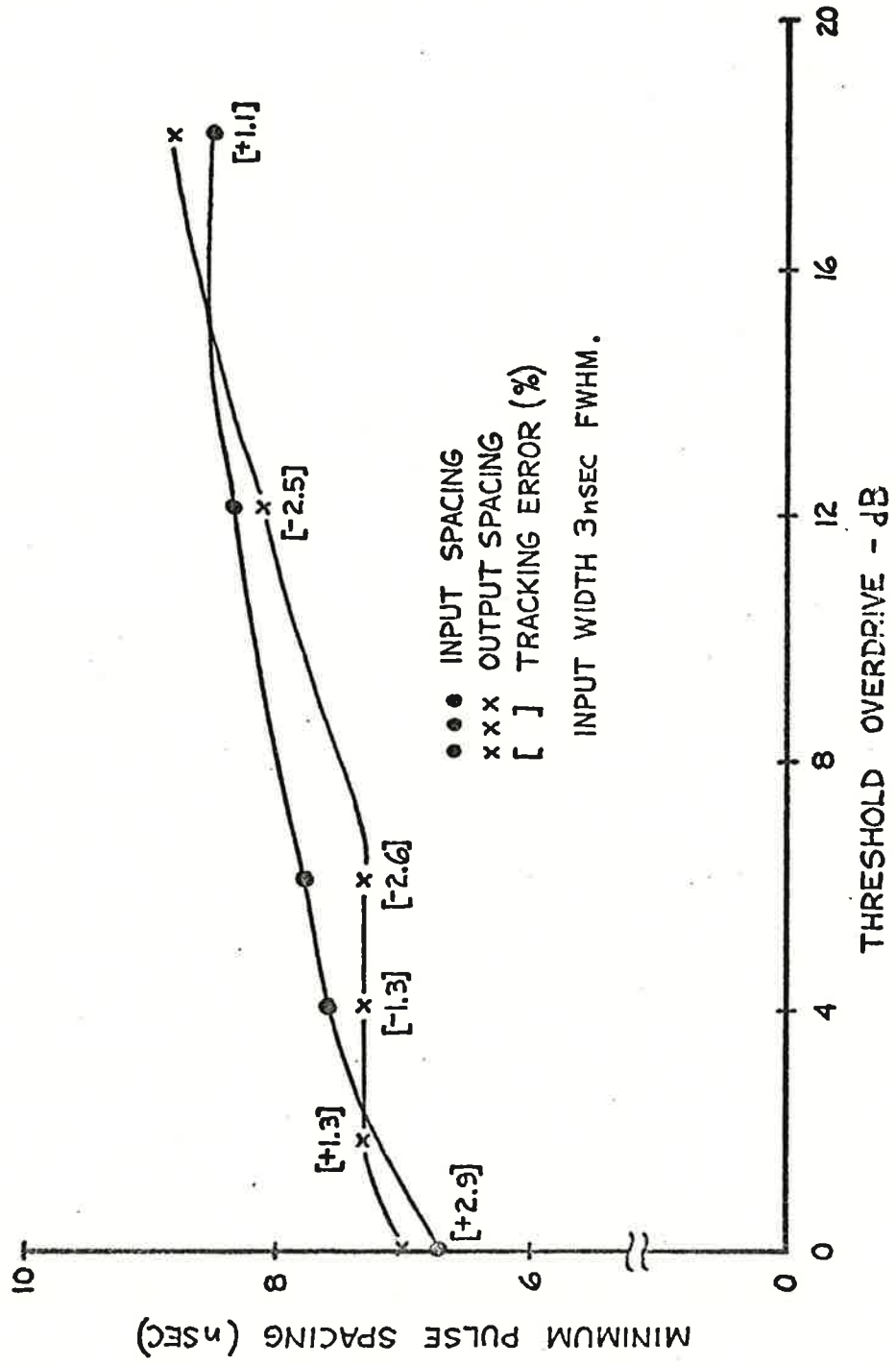

FIGURE 6

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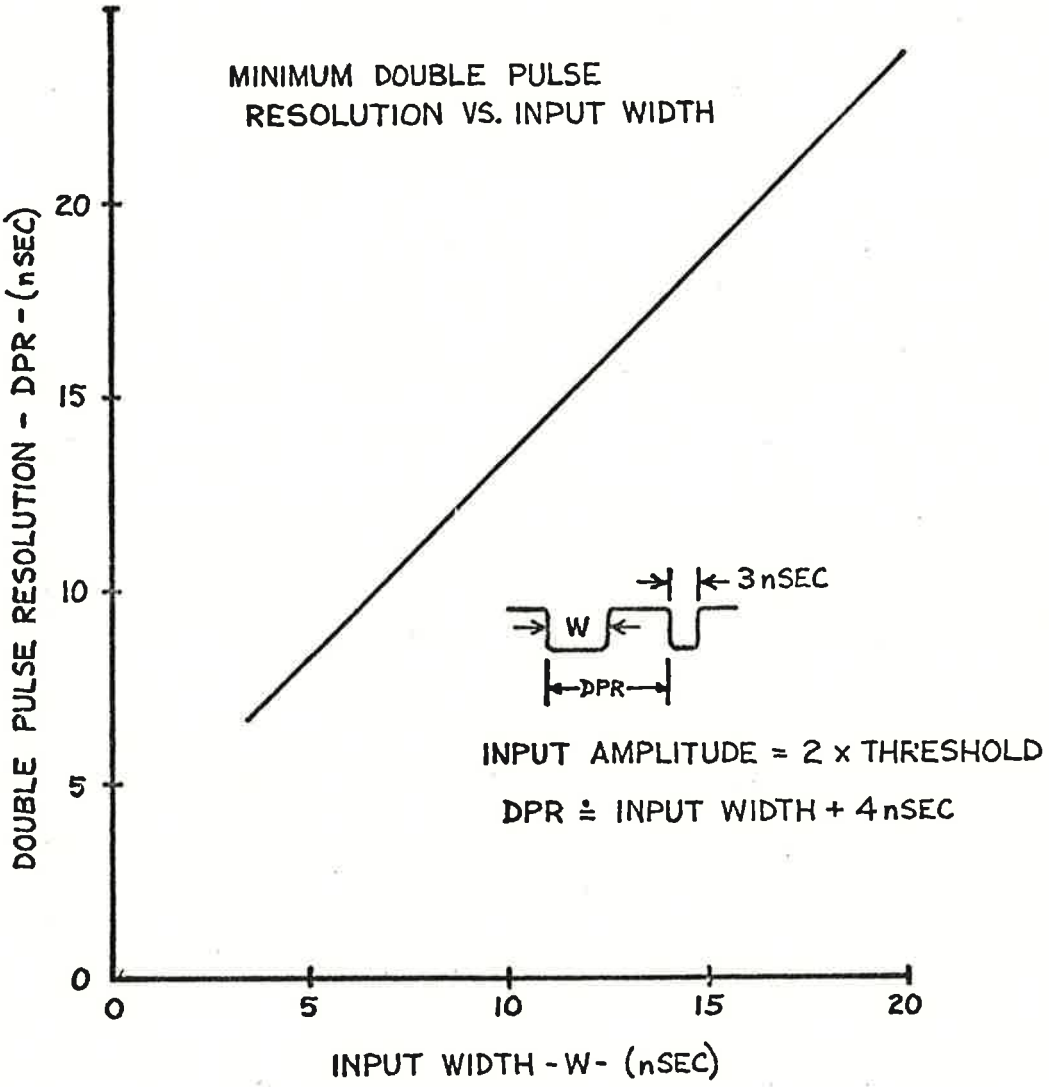

FIGURE 7

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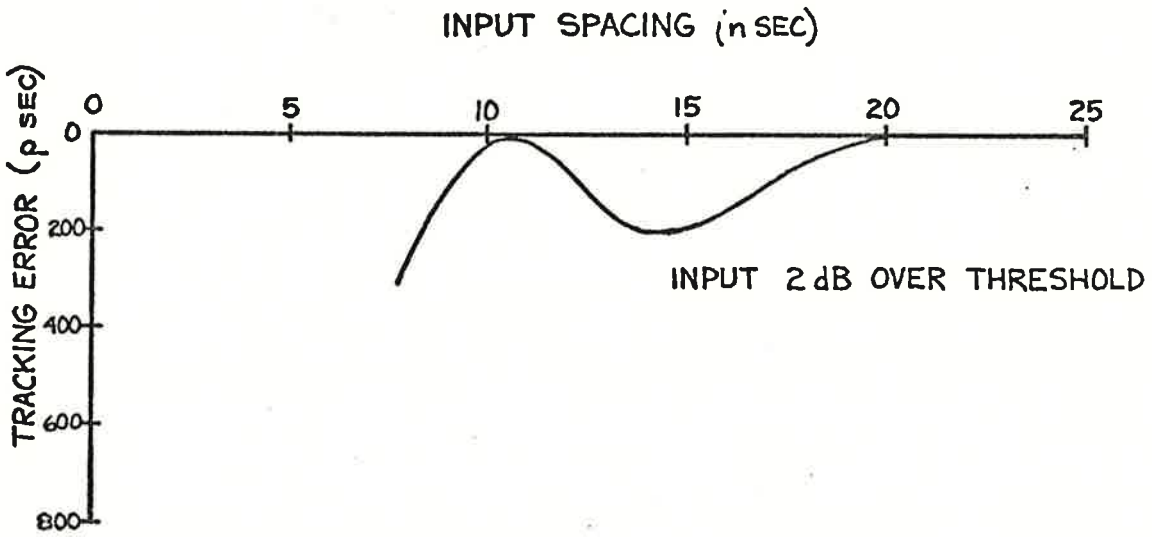

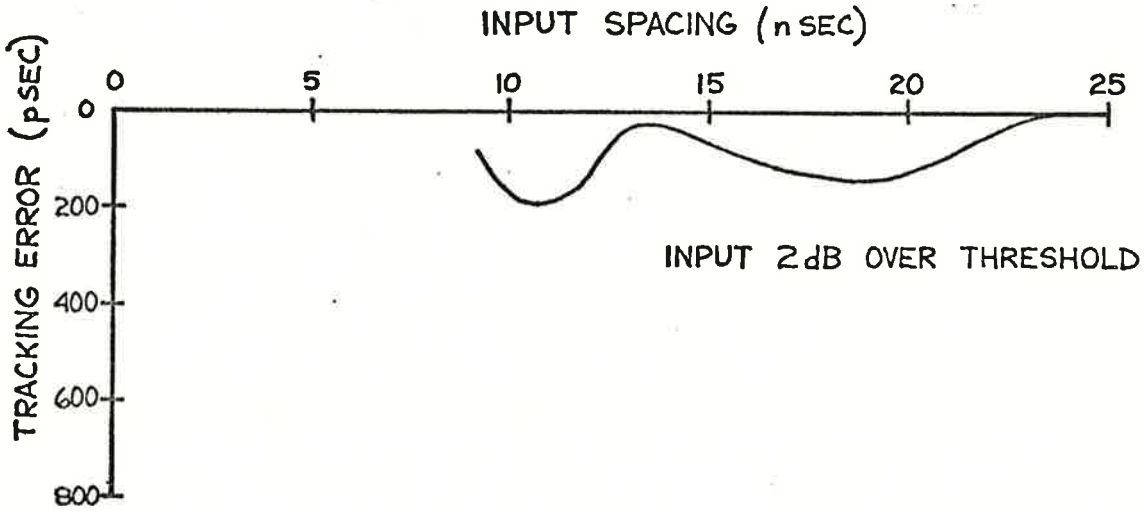

FIGURE 8

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4k. Slewing

At less than maximum input rates which do not tax the double pulse resolution of the discriminator, a class of characteristics comes into play which defines the fidelity of the discriminator output to the time information in the input signal. The most important of these, and the most difficult to strictly define and to measure, is time slewing or walk. This is variation in the input-to-output time delay of a discriminator with input amplitude. The net measured slewing yielded by a discriminator has two components, one contributed by the discriminator itself (intrinsic slewing) and the other dependent upon the input risetime.

Intrinsic slewing might be defined as the slewing measured with a delta function input. Risetime-dependent slewing arises from the fact that the discriminator fires earlier on the leading edge of a large pulse of finite risetime than on one of smaller amplitude. For an extreme range of pulse heights, the maximum contribution is equal to the 0 to 100% risetime of the pulse.

With most discriminators, by far the largest portion of the slewing occurs in the amplitude region just above threshold, threshold being defined as the input amplitude that produces 50% triggering. Slewing specifications are frequently given over an input amplitude range from threshold to a specified overload factor (such as 10X threshold).

No commonly accepted standard exists for measuring the slewing characteristics of discriminators. One technique which LeCroy considers relevant to describing a discriminator's timing characteristics is to obtain a time spectrum of shift in input-output delay when a uniform spectrum of pulse heights from below threshold to many times threshold is used to drive the discriminator. Such an input spectrum constitutes a relatively severe test of the discriminator's timing performance for it contains a relatively higher proportion of near threshold pulses than does a usual beam-derived photomultiplier spectrum. It takes into account all aspects of discriminator slewing performance and presents their combined effect in terms of a time dispersion curve such as indicated in Figures 9 & 10.

41. Packaging

The 620 series discriminators are all packages in a #1 NIM module

with LEMO-type connectors. Due to front panel space limitations, the 620's are not offered with BNC's.

4m. Current Requirements

The current usage of the 620 series is low enough to permit the use of 12 modules per standard 96-watt NIM bin offering a 5 A of ±6 V, 2 A of ±12 V, and 1 A of ±24 V. Power calculation works out to 6.51 watts, which does not exceed the 8 watts recommended by the NIM standard for maximum power dissipation for a single NIM slot.

4n. Recommended Use of the NIM Power Bins

It is highly recommended to keep any NIM bin at as constant a temperature as possible, using air conditioning in the trailer or experimental station and definitely using fans to assure an air flow through all modules in every bin. Elimination of large temperature variations removes the worry of temperature drift effects upon modules of any manufacturer, and the forced air flow is good insurance against the potential failure of components in the modules due to excessive heating for extended periods of time. Despite the fact that all components are pre-aged and burned-in before insertion into LeCroy modules, and the modules themselves are temperature cycled for days under power between initial test and final test, it is recommended to avoid subjecting any modules to adverse operating conditions if it could be avoided.

5. FUNCTIONAL DESCRIPTION

5a. General

Each of the eight channels of the Model 620 series is composed of two basic sections: the input and discriminator stage, and the output stage. A block diagram of the Model 620 series can be seen in figure 11, and a complete schematic of the specific model can be found at the end of this manual.

5b. Input and Discriminator

The input and discriminator stage is based on the LeCroy Model LD601 hybrid. This unit contains all of the circuitry of the discriminator with the exception of the input termination and high voltage protection. The latter two functions are self-explanatory in the schematic enclosed, and the LD601 is functionally presented in figure 12. The threshold level is set by changing the voltage bias on a fast differential amplifier which has a small amount of positive feedback to provide regeneration at threshold. In actual operation the V_T input is obtained by a voltage follower (IC PB). The voltage on the wiper of the front panel threshold potentiometer appears on the test point for monitoring the threshold.

The measured voltage will be 10 times the actual threshold voltage. When an input signal applied to -IN is equal to the threshold voltage at +IN, the amplifier output will begin to go positive. This will force +IN closer to 0 volts, which increases the differential input voltage in such a direction that the output locks and then the cycle reverses. The amplifier output thus provides a time-over-threshold pulse with fixed amplitude. This pulse can be monitored at the AMPL. OUT point (pin 6). The quiescent level should be nominally -2.4 volts going to -1.6 volts during the pulse. The leading edge of this output sets the latch circuit which is used as a pulse width standardizer. Before the latch can be set, the inhibit inputs (used for the bin gates and front panel inhibit on the 620CL) must be off. The required level at pin 16 of the LD601 must be 0 to -1.6 V to enable, and -2.5 to -6.0 to disable. (The common bin gate driver shifts this so that 0 volts at the Bin Gate input will inhibit, greater than +3 volts will enable.) Once the latch is set, a latch OUTPUT is available to drive the output stage. The OUTPUT amplitude and leading edge

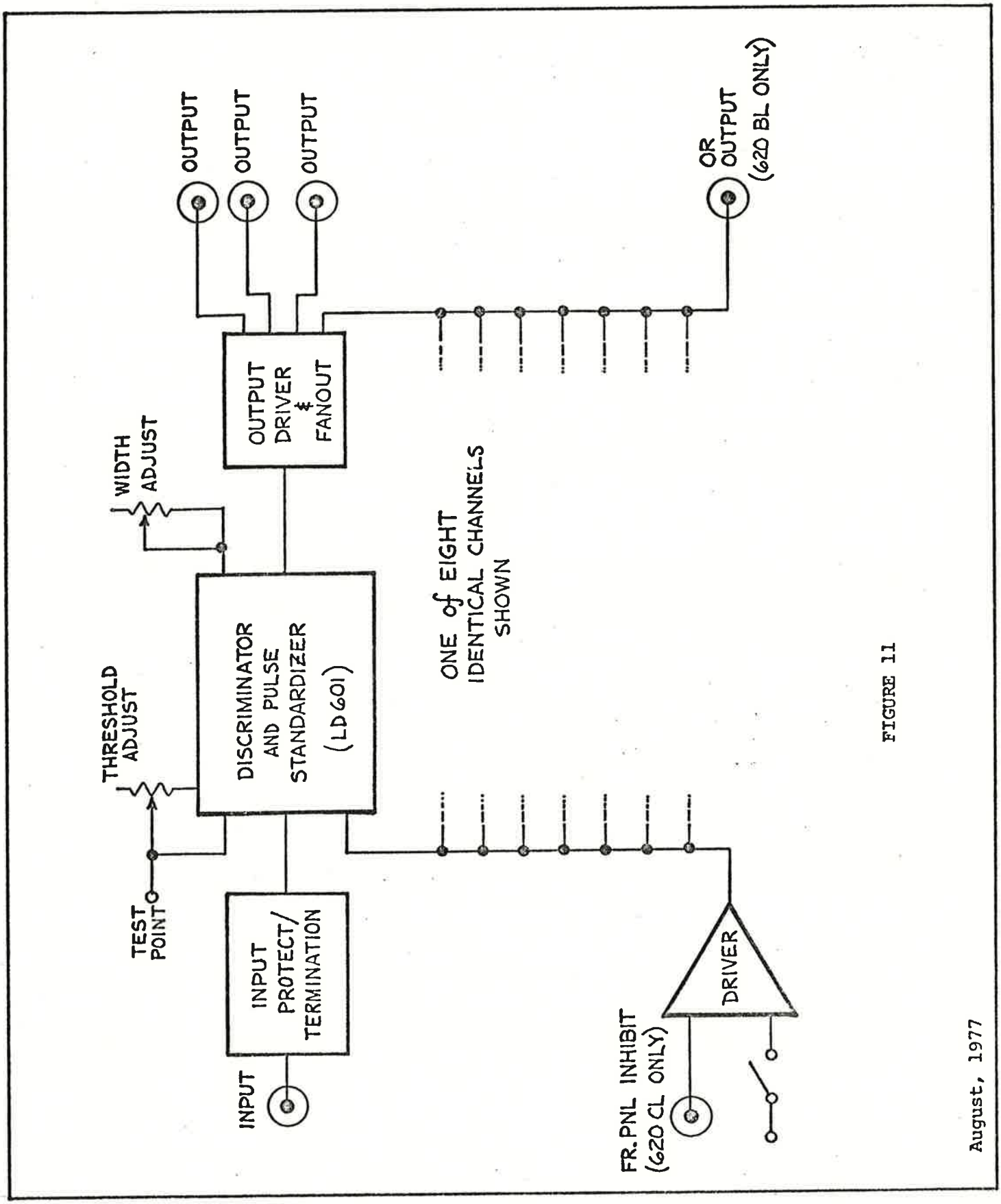

FIGURE 11

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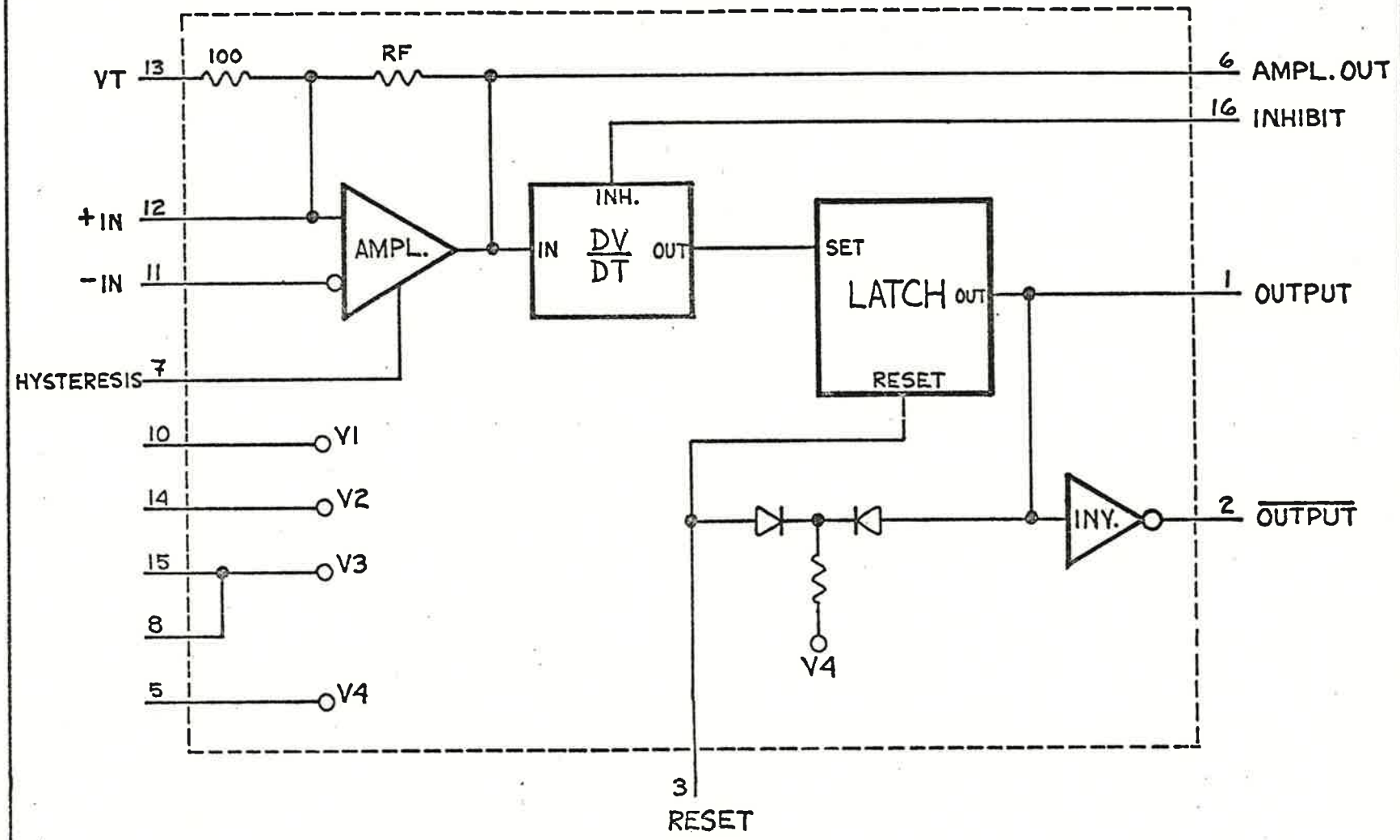

BLOCK DIAGRAM - LD 601E DISCRIMINATOR HYBRID

FIGURE 12

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should be similar in appearance to the AMPL OUT(Fig. 12), but the width of the output will be independent of the input width. Internally, the latch output is fed back to reset the latch after a short time delay, thus generating an output pulse whose actual width can be set by the front panel width adjustment pot.

5c. Output Stage

The output stage is a simple NPN inverter stage with the emitter returned to the negative 3.8 volt supply. The stage is normally based in the cut off region. During an output pulse sufficient base current is supplied from the LD601 to turn the output driver on. In the on condition, the collector voltage is approximately -2.7 volts. The 110 Ω series resistor and the 50 impedance of the load form a divider to provide a -840 mV output to the output connector. In order to reduce the turn off delay time of the output stage, the output driver is prevented from entering the saturation region by an anti-saturation technique, consisting of a conventional diode and a hot carrier diode.

The Model 620B also includes a diode switching network driven by the output stage to provide a signal for the summing (OR) output.

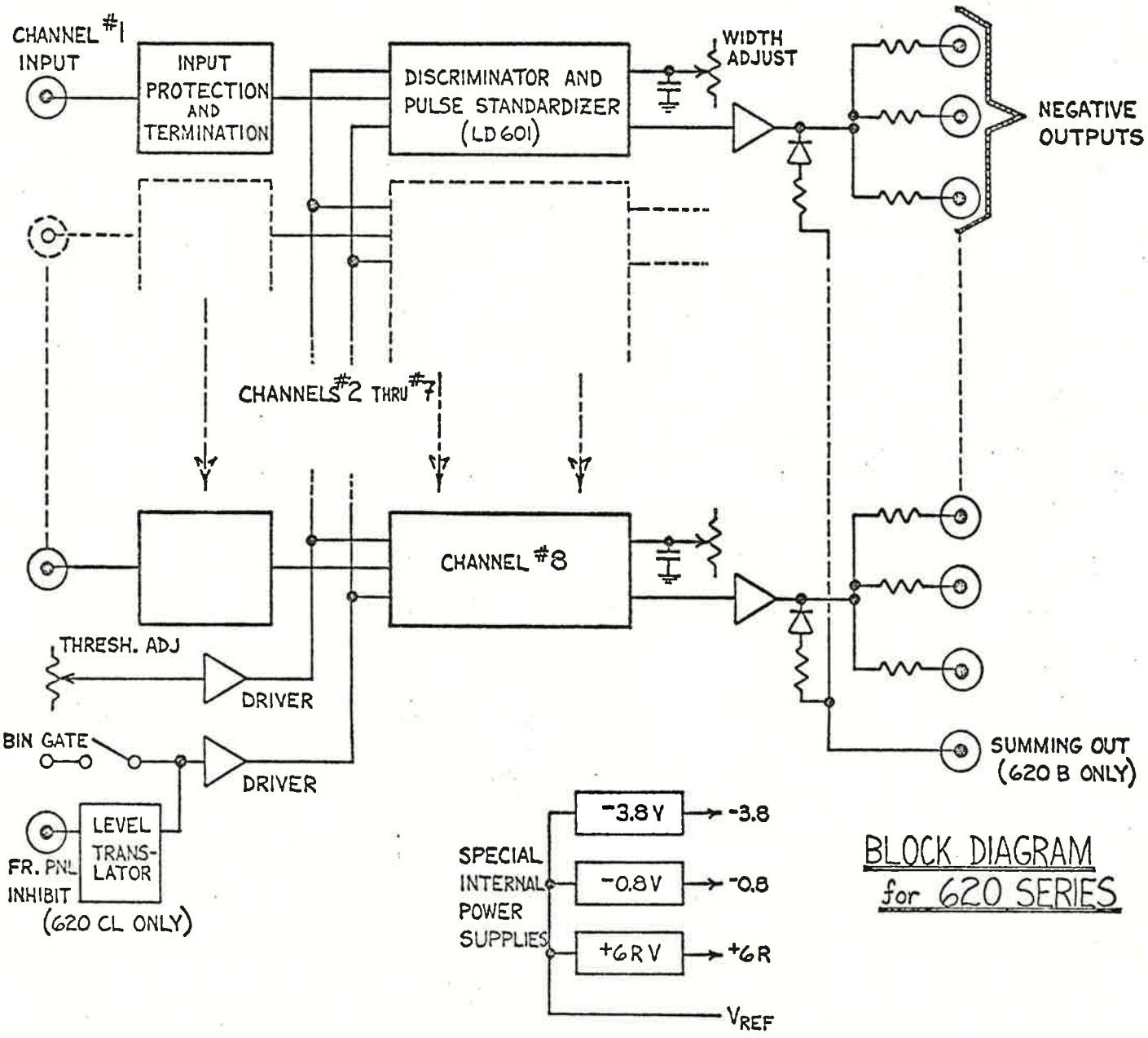
5d. Internal Power Supplies

Three internal power supplies are used to generate the -0.8, -3.8 and +6 V which are special bias voltages used by the eight channels. These stages provide voltage regulation and tracking and provide proper temperature compensation. They depend to some degree on uniform heating of the entire circuit board. Heating local areas of the board may cause drifting, but during operation in a normal bin environment these supplies compensate to stabilize operation. In all cases, the power supply uses a LM301 operational amplifier to maintain the output voltage so a series-pass transistor equal to an input reference voltage. The reference voltages are adjusted via individual potentiometers or trimmed resistors.

5e. Programming in the 620BLP

The Model 620BLP is a standard 620BL which has the critical threshold voltage brought directly out to an added rear panel 20-pin connector. Internal high frequency filtering is provided (i.e., T_{RC} + 0.01 seconds) on each input.

The remote programming voltage source must be low impedance (ideally less than 100 Ω). When using the front panel potentiometers, the rear panel programming should be removed.



BLOCK DIAGRAM for 620 SERIES

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FIGURE 13

6. TEST AND CALIBRATION

This test and calibration section has been included to familiarize the service technician with the areas that should be checked when searching for sources of failures and after replacing components, especially front end hybrids (LD601's). The trouble-shooting section is by no means exhaustive, but it does provide insight into some of the problems that have occurred at LeCroy during the initial testing of the 620L's. The technician should follow the "Trouble-Shooting Guide" for ease in determining the defective component. Replacement of critical components will require some recalibration.

6a. Equipment Required

1. Digital voltmeter.
2. Sampling scope; 50 Ω input impedance.
3. High impedance real time scope with bandwidth of 150 MHz or greater (Tektronix 454, 475, or equivalent).
4. Pulse generator or signal source capable of producing 10 nsec to 50 mV pulse into 50 Ω.

6b. Initial Setup

1. Use NIM power extended cable to power the 620 under test.
2. Set the threshold and all width pots to their full counter-clockwise position (threshold equal to -30 mV and width equal to less than 5 nsec).
3. Apply a 10 nsec negative pulse (approximately equal to -50 mV) in turn to each input. Check output on sampling scope.
4. Follow the "Trouble-Shooting Guide", next page.

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6c. Trouble Shooting Guide for Replacement of LD601

Pin 7/Pin 16 Jumper Consideration

In late 1973, it was determined that for optimum performance of the discriminator front end, (LD601 hybrid), pin 7 of the LD601 should be externally jumpered to pin 16. This external jumper is provided on the circuit boards themselves of the following discriminators:

Model 621AL, 621BL, 621BLP, 621CL, 621S, Quad

Model 620AL, 620BL, 620BLP, 620CL, 623, Octal

For the Model 621L Quad, only units produced after November 28, 1973, have the jumper included.* For the 620L Octal, only units produced after October 10, 1973, have the jumper included.

Therefore, for proper installation of replacement LD601's or LD601C's, we have summarized on the following pages.

6d. Required Recalibration if LD601 Was Replaced

Replacement of LD601: If any LD601 was found to be defective and required replacement, the Threshold and Test Point voltage should be recalibrated.

Procedure:

1. Set front panel Threshold pot to minimum (counterclockwise).

2. Measure Test Point voltage. If not equal to -300 ±5 mV, replace existing trim resistor (across 620 Ω resistor) with proper resistance to bring Test Point voltage into required range.

3. Check Threshold level with a 5 nsec wide pulse; if it is not -30 mV, replace existing trim resistor (pin 12 of the LD601) with proper resistance.

* Approximate production dates can be determined by the dates written on the rear panel Test and Calibration stickers.

TEST & CALIBRATION

Model	LD601C	LD601D	LD601E
620BL	Direct Replacement	Add 3.2 -18 pF trimmer from pin 3 to Gnd. Adjust for optimum output shape. Also remove Min and Max trims. Adjust front panel width control to max (CW). Adjust front panel threshold control to 30 mV (CCW). Adjust trimmer for 22.5 nsec output width.	Direct replacement, but only in units originally containing LD601E.
620BLP	Direct Replacement	Add 3.2 -18 pF trimmer from pin 3 to Gnd. Adjust for optimum output shape. Also remove Min and Max trims. Adjust front panel width control to max (CW). Adjust front panel threshold control to 30 mV (CCW). Adjust trimmer for 22.5 nsec output width.	Direct replacement, but only in units originally containing LD601E.
620CL	Direct Replacement	Add 3.2 -18 pF trimmer from pin 3 to Gnd. Adjust for optimum output shape. Also remove Min and Max trims. Adjust front panel width control to max (CW). Adjust front panel threshold control to 30 mV (CCW). Adjust trimmer for 22.5 nsec output width.	Direct replacement, but only in units originally containing LD601E.
620L	Make sure pins 7 & 16 are jumpered.	Make sure pins 7 & 16 are jumpered. Add 3.2 -18 pF trimmer from pin 3 to Gnd. Adjust for optimum shape.	Cannot be used in 620L.

TEST & CALIBRATION

Model	LD601C	LD601D	LD601E
620AL	Direct Replacement	Add 3.2 -18 pF trimmer from pin 3 to Gnd. Adjust for optimum output shape. Also remove Min and Max trims. Adjust front panel width control to max (CW). Adjust trimmer for 22.5 nsec output width.	Cannot be used in 620AL.

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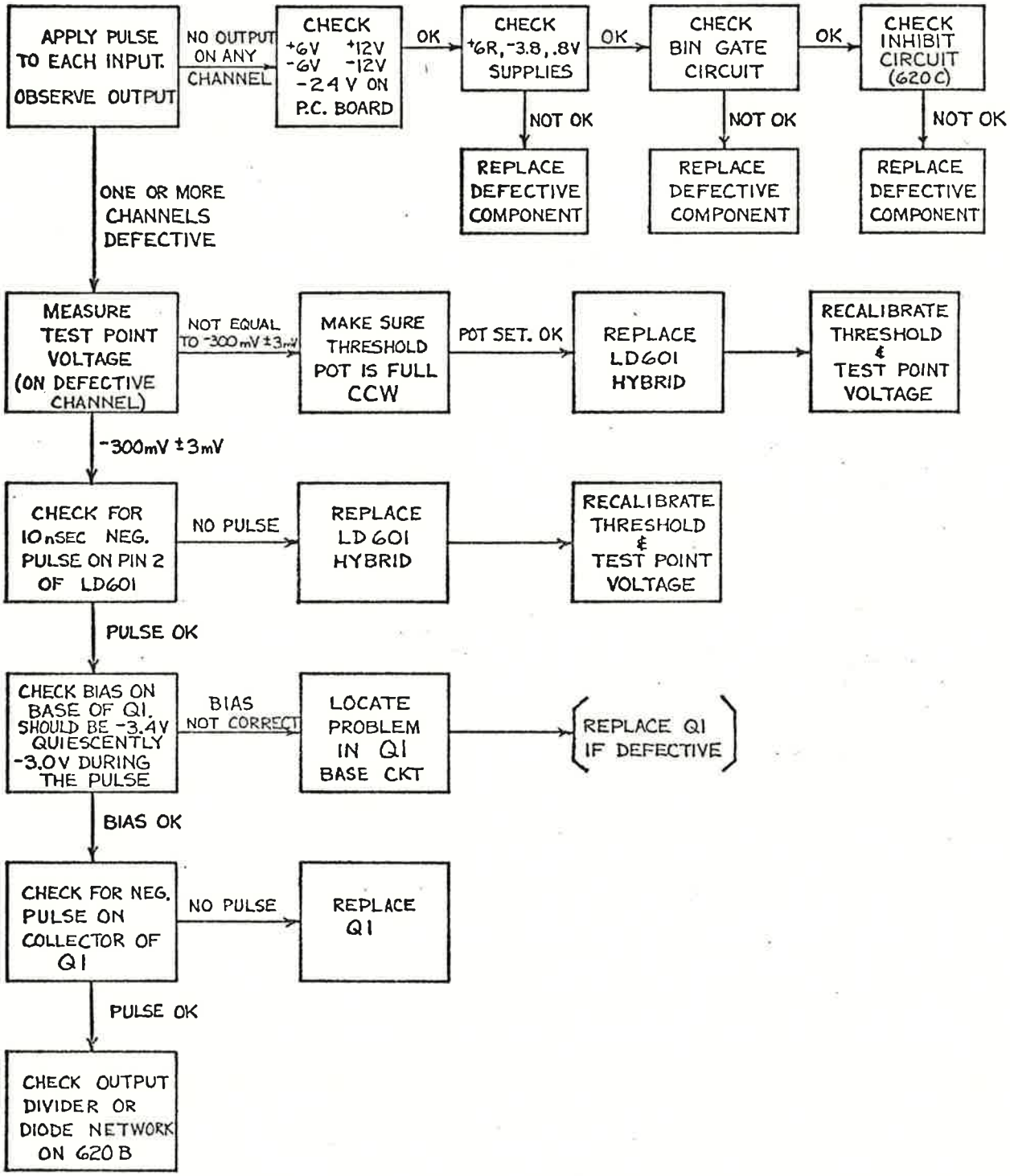
TROUBLE SHOOTING GUIDE



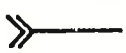
August, 1977 Figure 14

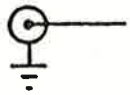
STANDARD DRAFTING SYMBOLS, ELECTRONIC

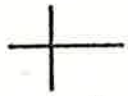

Connection to any given voltage.

Line ending at the edge of the sheet indicates continuance on another sheet.


Male pin or card edge contact.


Female pin, socket or card edge connector.


Coaxial connector.


No connection.

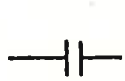

Connection.


Resistor, 1/4 W, ±5%, value in ohms (unless specified otherwise).

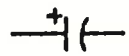
Resistor, 1/4W, ±1%, value in ohms (unless specified otherwise).

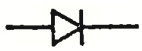

Resistor, variable, any type.

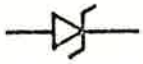

Resistor, variable, any type.


Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).


Capacitor, variable. Values in Picofarads (unless specified otherwise).


Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).

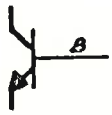

Diode, signal or rectifier.


Diode, zener.

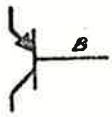

Diode, tunnel.


Diode, snap.

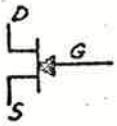

Light emitting diode (LED).



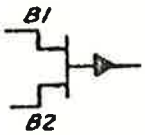
NPN Transistor.



PNP Transistor.



Field effect transistor, P Channel.



Field effect transistor, N.


Air choke.


Ferrite bead.


Ferrite core choke, Z 500 ohms when f > 60 MHz (unless otherwise indicated).


Ferrite core choke, 40 uH, (unless otherwise indicated).

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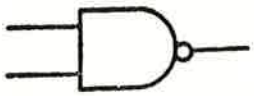
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL).

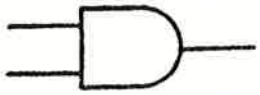
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

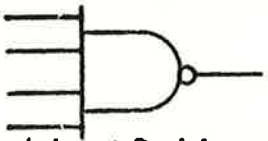
Supply voltages of IC's are shown in a table on each schematic.



2-Input Positive NAND Gate

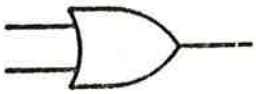


2-Input Positive AND Gate

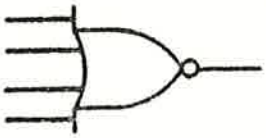


4-Input Positive NAND Gate

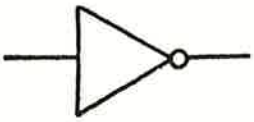
2- Input Positive NOR Gate



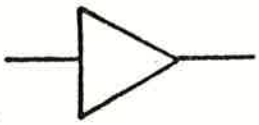
2-Input Positive OR Gate



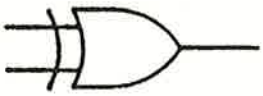
4-Input Positive NOR Gate



Inverter or Inverting Buffer

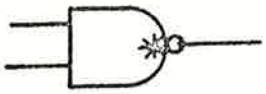


Non-Inverting Buffer

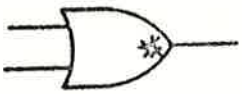


Exclusive OR Gate

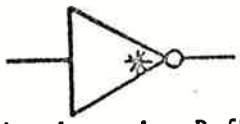
Open collector outputs are identified by an asterisk (*) on the output connection.



2-Input Positive NAND Gate W/Open Collector



2-Input Positive OR Gate W/Open Collector



Non Inverting Buffer W/Open Collector

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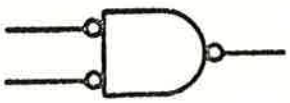
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS EMITTER - COUPLED LOGIC (ECL)

The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

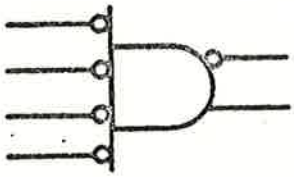
Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

Supply voltages of IC's are shown in a table on each schematic.

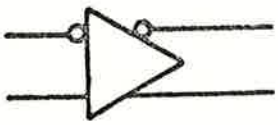


2 - Input Gate.
Negative AND (Positive OR) Gate.

2 - Input Gate.
Negative NAND (Positive NOR) Gate.

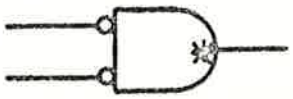


4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.

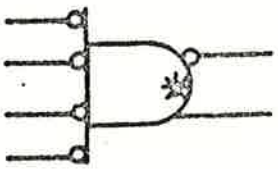


Differential
Amplifier.

Open emitter outputs are identified by an asterisk (*) on the output connection.



2 - Input Negative NAND Gate.
With Open Emitter.



A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.

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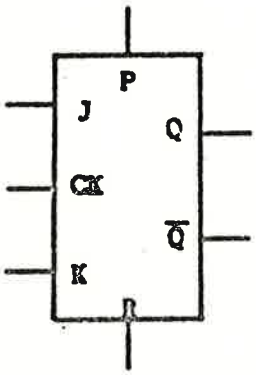
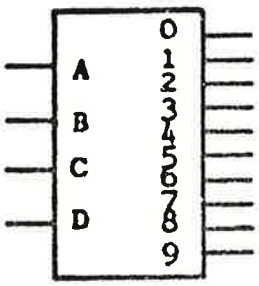
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL) OR EMITTER COUPLED LOGIC (ECL).

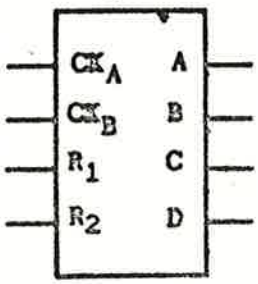
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave Flip-Flop

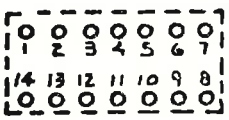


BCD-To-Decimal Decoder-Driver



Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.



Bottom View

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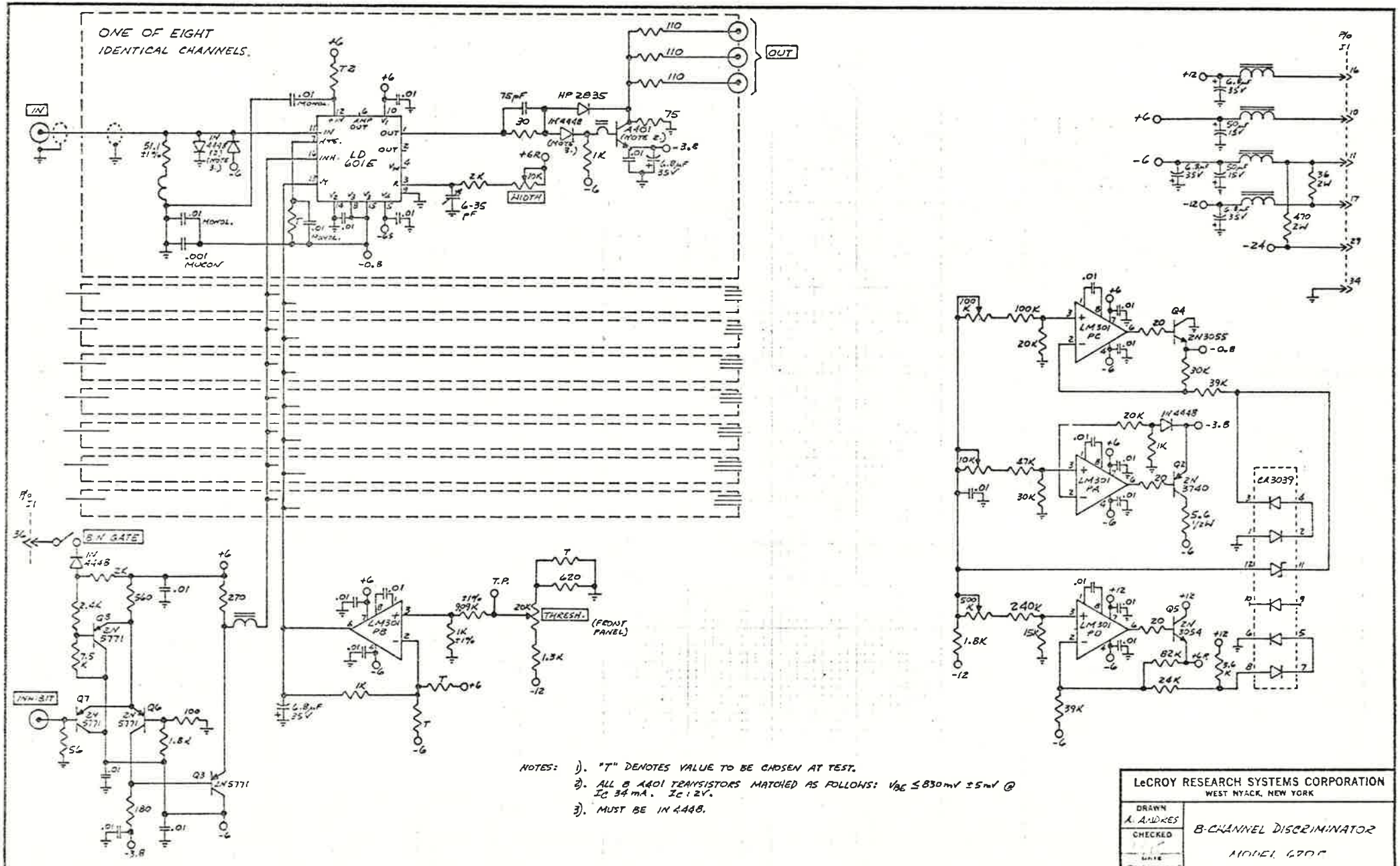

NOTES:
1). "T" DENOTES VALUE TO BE CHOSEN AT TEST.
2). ALL 8 A401 TRANSISTORS MATCHED AS FOLLOWS: $V_{BE} \leq 830mV \pm 5mV$ @ I_C 34 mA. I_C : 2V.
3). MUST BE IN 4448.

LeCROY RESEARCH SYSTEMS CORPORATION WEST NYACK, NEW YORK	
DRAWN A. ANDRES	8-CHANNEL DISCRIMINATOR
CHECKED	MODEL 620C
DATE JAN. 7, 1975	ECO No. 505
DRAWING No. 620C-S1	

ECO NO.	DATE	DESCRIPTION
872	6-17-75	.05 uF COMPENSATION CAPS AT OP AMPS CHANGED TO .01 25V./ AT EACH LD601, PIN 12: CHANGE 12K. TO 12.4 PREC./
898	7-28-75	MINIMUM & MAXIMUM WIDTH TRIMS DELETED/ 2.3 - 18 pF VARIABLE CAP ADDED PIN 3 OF LD601
928	10-7-75	CHANGE TO NEW WRAPAROUND: PARTS LIST. TAPING /A to /B.
959	10-21-75	RELAY AND ASSOCIATED 100 OHM RESISTOR ELIMINATED.
010	12-29-75	LD601C CHANGED TO LD601D/ 18pF MICA CAP REM FROM PIN 3 OF LD 601D AND 2.3 - 18 VARIABLE CAP CH. TO 6 - 35pF/ A430 CHANGED TO A401/ 56pF REMOVED/ SERIES 10 OHMS & 22pF ADDED/ 240 OHMS CHANGED TO 91 OHMS/ 1/2 BEAD ADDED TO BASE OF A401.
067	3-11-76	REMOVED: 22pF CAPACITOR AND 10 OHM RES., NEAR PIN 1 OF LD 601/ 75pF CAP ADDED SAME PLACE, ACROSS 30 OHM RESISTOR.
098	3-19-76	ALL 8 MBD 101 DIODES CHANGED TO HP 2835.
119	4-29-76	TAPING CHANGED FROM /B TO /C. LD601D CHANGED TO LD601E/ FRONT END CIRCUITRY AROUND LD601E CHANGED/ 120 OHM OUTPUT RESISTORS CHANGED TO 110 AND 91 OHMs CHGD TO 75 OHMS/
505	11-1-77	CHANGED 510K ON IC PD PIN 3 TO 240K RESISTOR.
1001	6-7-78	HARDWARE CHANGED TO ACCOMODATE 79P SERIES REPLACEMENTS.
1002	6-21-78	SEPARATED 620CL AND 620CLR PARTS LISTS INTO "BASIC" AND "ADDER" VERSIONS.
1003	8-9-78	PARTS LIST UPDATED ONLY.

REMARKS

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN	ENGINEERING CHANGE ORDERS
CHECKED	MODEL 620 C
DATE	

DRAWING No.