technical information manual

NIM Model 465/466
Triple 4-Fold Coincidence Units

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
West Nyack, New York

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique,reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refine and improve the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Spring Valley, NY, telephone 914-425-2000, or from your local distributor in countries other than the U.S.A.

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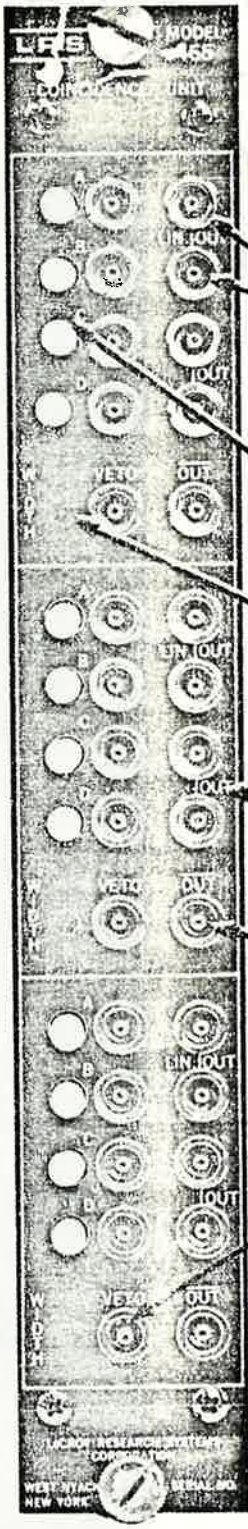
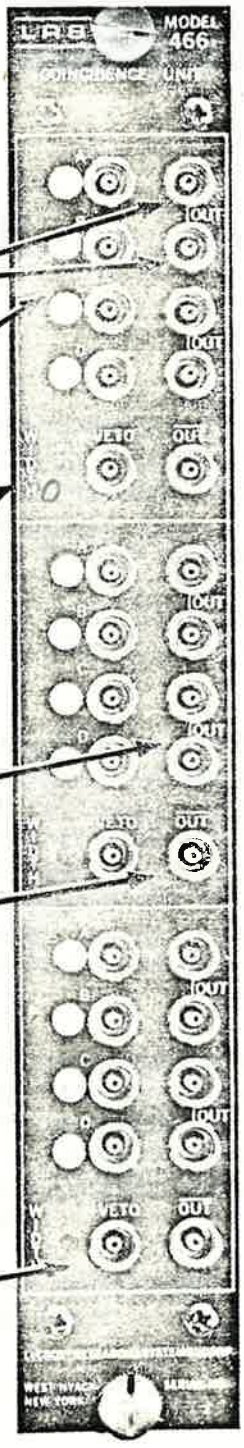
NIM Model 465/466
Triple 4-Fold Coincidence Units





Linear output bridged pair.
Fast NIM output*. Duration =
input overlap duration.

Input Select Buttons
in = select
out = defeat

Width Adjust
<5 nsec to >500 nsec

Preset Output
NIM output* bridged pair.
Duration determined by
setting of width pot.

Complementary Output
(-16 mA quiescently; 0 mA during
pulse). Duration determined
by setting of width pot.

50 Ω; > -600 mV input.
Veto must overlap
entire coincidence
interval.

50 Ω; > -600 mV input.
Veto need overlap
leading edge of coinci-
dence only.

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TECHNICAL DATA

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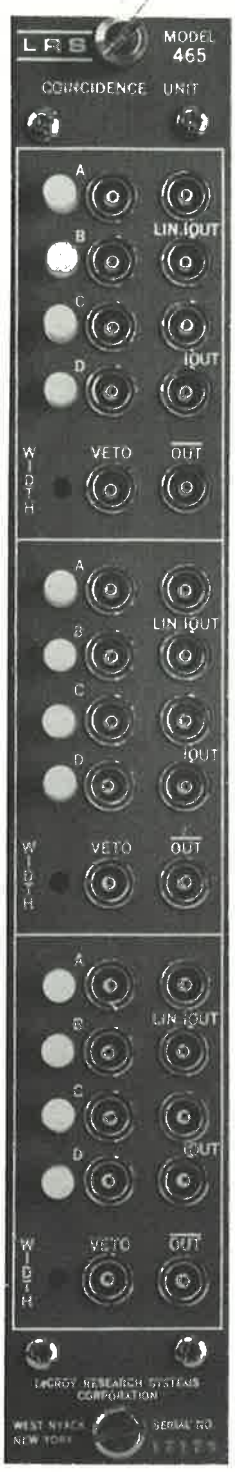


NIM Model 465

Triple 4-Fold Logic Unit

WITH VETO

The LRS Model 465 contains three independent high-speed general-purpose coincidence units in a single-width NIM module. Each channel has four coincidence inputs and a separate veto input which accept standard negative NIM logic levels. The logic inputs may be individually enabled or disabled without altering input cabling or termination by means of front-panel pushbutton switches. With all inputs enabled, four inputs are required. Disabling the logic inputs is equivalent to reducing the number of simultaneous negative inputs required for an output. Thus, each channel may be programmed for 4-fold, 3-fold, or 2-fold logic decisions. With only one input enabled, each channel of the 465 operates as a logic fan-out.

Once triggered by signals satisfying the input coincidence requirements, the 465 generates five NIM fast logic outputs: one pair of −32 mA negative preset outputs, one −16 mA preset complementary output, and one pair of −32 mA overlap outputs. The preset outputs are continuously adjustable from less than 5 ns to greater than 500 ns by means of a front-panel multiturn potentiometer and are independent of input overlap time, amplitude, and rate. Because it is updating, it may be retriggered even before the end of an output pulse that is already present. The overlap outputs are equal in duration to the coincidence overlap and produce outputs up to the maximum input rate capability.

The front-panel fast veto input accepts standard negative NIM-level pulses. To veto the linear outputs, the veto signal must completely overlap any input coincidence; to veto the preset outputs, a prompt overlap of the leading edge of the input signal that would otherwise create the coincidence condition is required. A rear-panel bin-gate switch permits a slower (50 ns response time) inhibiting of the 465 by a clamp to ground from +4 volts through the bin gate pin of the rear power connector.

The Model 465 is packaged in a standard AEC/NIM #1 module (AEC Report TID-20893) and uses exclusively Lemo-type front panel connectors.

December 1975

Innovators In Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION · SPRING VALLEY, N.Y. 10977 · TELEPHONE: (914) 425-2000

SPECIFICATIONS
NIM Model 465
TRIPLE 4-FOLD LOGIC UNIT

INPUT CHARACTERISTICS

Logic Inputs:	4; Lemo-type connectors; 50Ω impedance; negative NIM-level input requirements; each input can be separately enabled or disabled by front-panel pushbuttons.
Veto Input:	Standard negative NIM-level signal, 3.5 ns minimum width. Requires complete overlap of input coincidence for linear outputs and prompt overlap of the leading edge of the input signal that would otherwise create the coincidence condition for the preset outputs. (Veto should precede this leading edge by approximately 5 ns in this case.)
Bin Gate:	Via rear connector; clamp to ground from +4 volts inhibits; risetimes and falltimes < 50 ns.

OUTPUT CHARACTERISTICS

Preset Outputs:	3; one dual negative (quiescently 0 mA, −32 mA during output), one positive (quiescently −16 mA, 0 mA during output). Updating.
Overlap Outputs:	One dual negative; quiescently 0 volts, −32 mA during output; duration equal to coincidence overlap. Non-updating.
Fan-Out:	5-fold, if each output drives a 50Ω load.
Duration:	Continuously adjustable from less than 5 ns to greater than 500 ns by means of front-panel, screwdriver-adjustable potentiometer. Width stability: better than ± 0.2%/°C maximum.
Output Risetimes:*	$\overline{\text{OUT}}$: ≤2.0 ns typical (max. 2.2 ns). OUT: ≤2.2 ns typical (max. 2.5 ns; 3.0 ns with negative output unterminated).
Output Falltimes:*	$\overline{\text{OUT}}$: ≤2.0 ns typical (max. 2.5 ns). Slightly longer on wide output durations. OUT: ≤2.2 ns typical (max. 2.5 ns). Slightly longer on wide output durations.

GENERAL

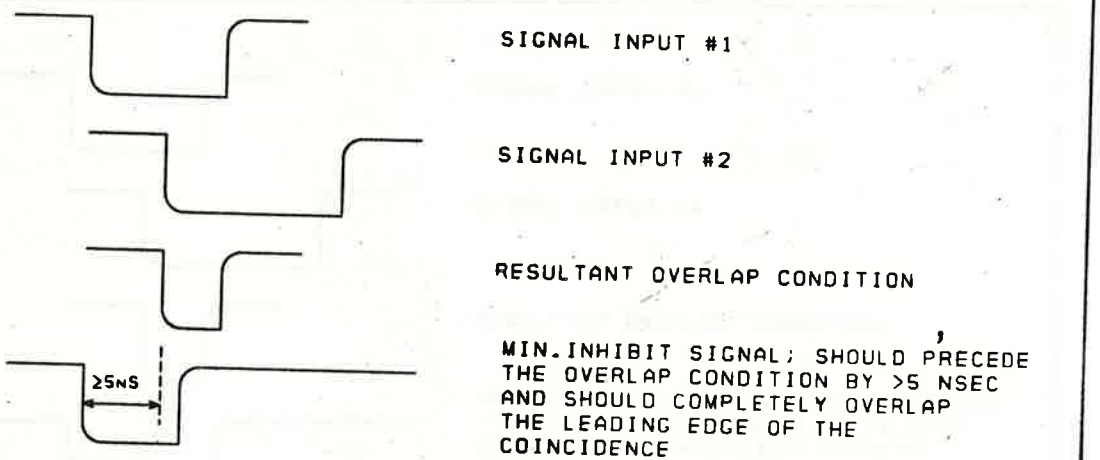
Logic:	2-fold, 3-fold, or 4-fold coincidences plus fan-out determined by selectively disabling logic input.
Coincidence Width:	1 ns up, determined by input pulse durations.
Rate:	120 MHz minimum.
Input-Output Delay:	13 ns preset; 8.5 ns linear.
Multiple-Pulsing:	None; one and only one output pulse of preset duration is produced each time the input conditions are satisfied regardless of the duration of the input pulses or their overlap.
Double-Pulse Resolution:	8 ns.
Packaging:	Single-width AEC/NIM module; in conformance with AEC standard; Lemo-type connectors used for all inputs and outputs.
Current Requirements:	+12 V at 65 mA +6 V at 125 mA −24 V at 5 mA −12 V at 135 mA −6 V at 640 mA

*−100 mV to −700 mV.

INPUT CHARACTERISTICS

Logic Inputs: The Models 465/466 have direct-coupled, 50 Ω impedance inputs which accept fast NIM logic signals (-0.6 V to -1.8 V). These inputs, typically driven from a discriminator or other logic unit, are protected both for transient and DC signals up to ±5 volts. Since the input reflections are less than 7% for signals of as little as 2 nsec risetime, even the maximum level signal in the NIM-specified range for a logic input (i.e. -1.8 volts) will reflect only approximately 125 mV, eliminating the probability of accepting multiple pulses corresponding to only one original input pulse.

Model 466 Veto Inputs: The veto inputs of the Model 466 require NIM logical one input signals as described above. In order to inhibit (veto) a coincidence, the applied veto pulse must overlap the leading edge of the input signal that would otherwise cause the coincidence condition. Due to internal delays, the leading edge of the veto signal should precede the coincidence condition by at least 5 nsec. Consider the diagram below.



INHIBIT INPUT - SIGNAL INPUT OVERLAP REQUIREMENT

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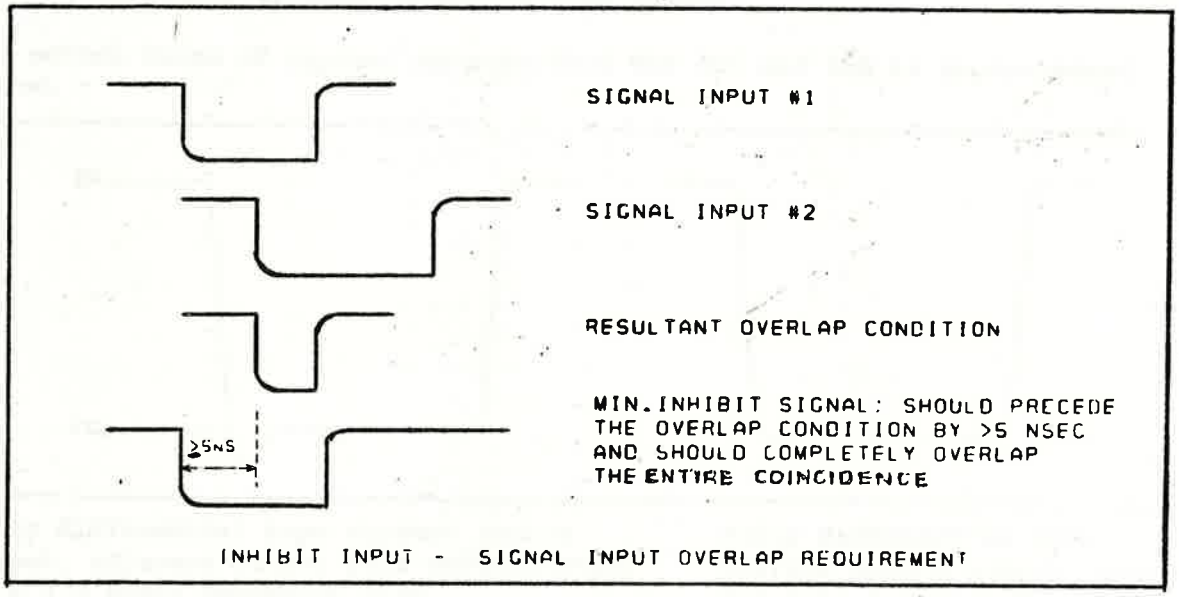
Model 465: Veto Input (for preset outputs only): The veto inputs of the Model 465 require NIM logical one input signals (ie, >-600 mV into 50 Ω). In order to inhibit (veto) a coincidence, the applied veto pulse must overlap the leading edge of the input signal that would otherwise cause the coincidence condition. See description and associated diagram in preceeding section (Model 466: Veto Inputs).

Model 465: Veto Input (for linear outputs only): The veto inputs of the Model 465 require NIM logical one input signals as described above. In order to inhibit (veto) a coincidence, the applied veto pulse must overlap the entire coincidence condition as shown in the diagram below. This requirement is necessary since this linear output is determined only by the output of the front end of the logic unit, as opposed to the preset outputs where the leading edge of the front end output triggers a preset width stage. In the latter case, if the leading edge is vetoed, the entire preset width output stage never sees it, thereby preventing any preset output. In the case of the linear outputs, any portion of the front end output that is not specifically overlapped by the veto pulse will appear at the linear output connectors.



INHIBIT INPUT - SIGNAL INPUT OVERLAP REQUIREMENT

OPERATION

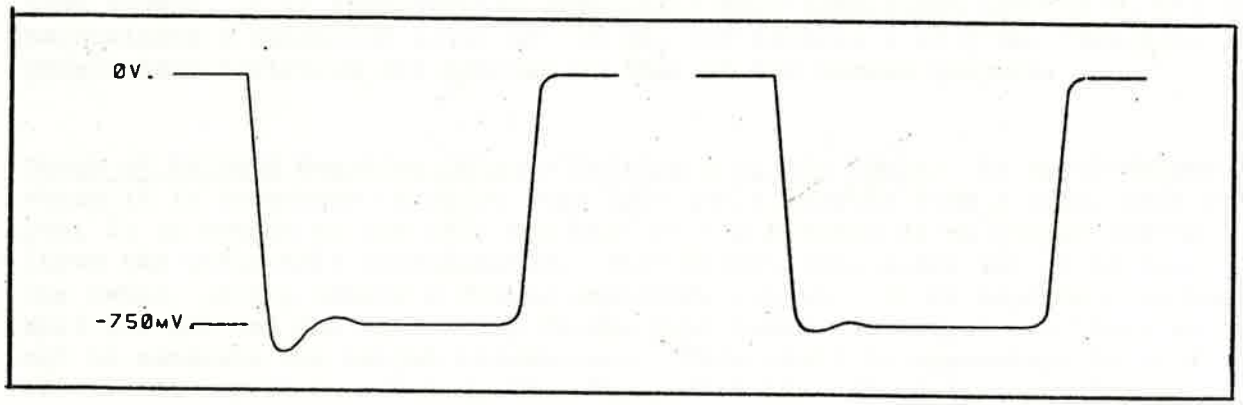
Inputs Select Switches: Any input will be removed from the coincidence requirement without removing its cable if the adjacent "Input Select Button" is in the OUT position.

Usage of 465/466 as a Triple 5-Fold Coincidence: In order to use the 465 or 466 as a 5-fold coincidence unit, a complementary fast NIM signal may be applied to the veto input. This signal will quiescently, then, hold the 465/466 in an off condition. When a pulse is applied to this input, it permits the 465/466 to give an output if the other selected inputs are in coincidence. Such application for the 465 and 466 is possible only at the sacrifice of usage of the veto input for a true inhibiting function.

OUTPUT CHARACTERISTICS

Bridged Negative Outputs: The Models 465 and 466 have two pairs of current source 50 Ω outputs, delivering -32 mA of current during the output and 0 mA quiescently. These outputs are fully differential type current source outputs. These outputs maintain a risetime of approximately 2.0 nsec and a reasonably clean shape, as long as care is taken to terminate at least one half of the other bridged output in that channel.

The actual shape of typical outputs from the 465 and 466 is approximated below.



Fully differential type current source output, adjacent output pair unterminated; tr ≈ 2.5 nsec; overshoot <15%.

Fully differential type current source output, output pair terminated; tr tr ≈ 2.0 nsec; overshoot <10%.

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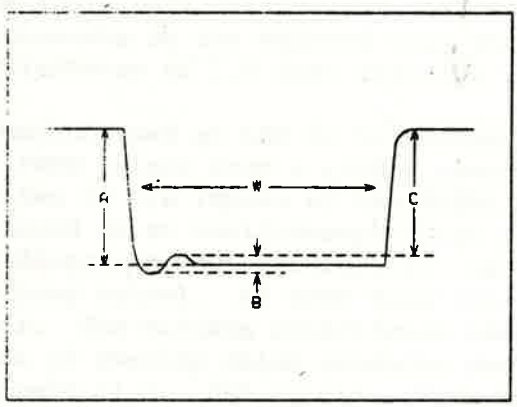
OPERATION

Using the typical output pulse shape following as a visual reference, LRS output shapes for the fully differential type preset outputs on the 465 and 466 are set up to adhere to the following restrictions, with adjancent output pair terminated into 50 Ω:



AMPLITUDE: -700mV<A<-850mV.

OVERSHOOT: B<10% OF A; C DOES NOT REACH -600mV

RISETIME: <2.5 NSEC.

FALLTIME: <2.5 NSEC. AT MINIMUM WIDTH.

MINIMUM WIDTH: WMIN (FWHM) <5.0 NSEC.

MAXIMUM WIDTH: WMAX (FWHM) - 1 USEC.

Complementary Output: The single complementary output is actually the output from the collector of the other half of the differential pair supplying current to one pair of preset outputs. Although it is internally a double amplitude signal, it is subsequently internally back-terminated into 50 Ω, thereby maintaining a quiescent level of -16 mA, and logical 1 of 0 mA. Risetime and other characteristics are similar to that of the normal outputs.

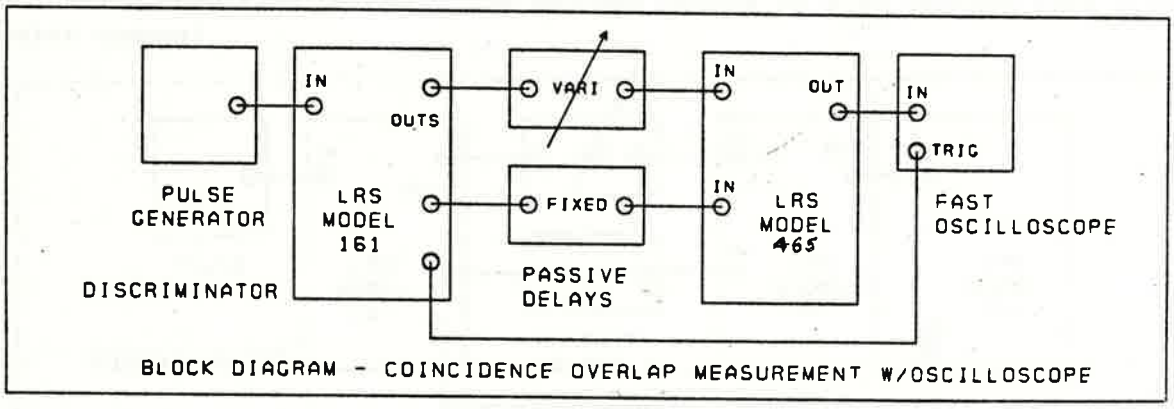
Usage of Bridged Negative Outputs Driving a Single Cable: In applications where it is necessary to drive very long cable lengths from a logic unit output, it is common to use only one half of the bridged 32 mA output and to leave the other half unterminated. This effectively sends all 32 mA into one cable, giving nearly a double amplitude output. It is important to know that the 465 and 466 have clamp diodes that limit the output amplitude so as not to saturate the output transistors. This limit is approximately -1.4 volts. It cannot be assumed, therefore, that the -32 mA into one 50-ohm cable will give a -1.6 volt output signal.

GENERAL

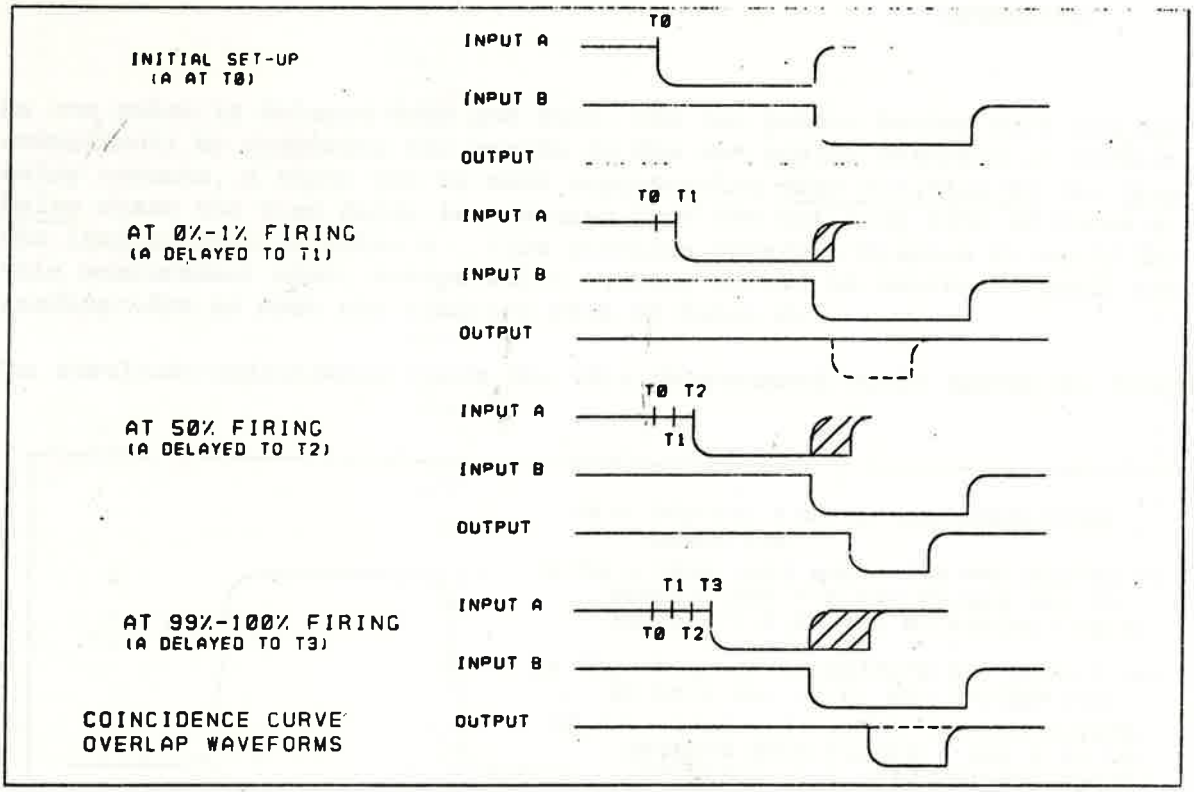
Coincidence Characteristics

Minimum Coincidence Overlap (Coincidence Resolving Time): The required coincidence overlap time of two input signals on the 465/466 is approximately nsec. Although this measurement should be made with two pulses of zero risetime for an absolute result, functionally, no discriminator or other logic unit driving the 465/466 could output such fast pulses. The measurements on the 465/466 were therefore made with an LRS Model 161 Dual Discriminator of 1.5 nsec risetime and falltime.

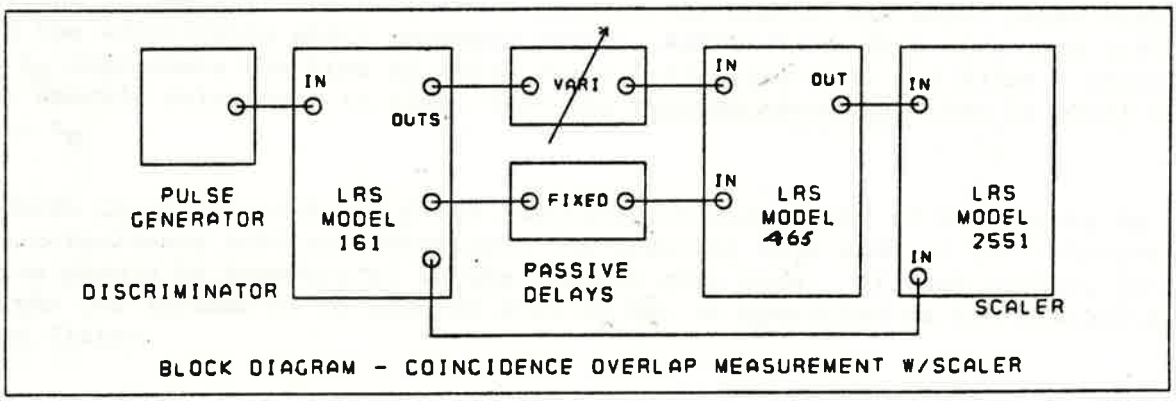
One method used at LRS is to measure the overlap time as follows. Two 10 nsec FWHM pulses from a single source all initially separated in time and fed into two of the inputs of the Model 465 or 466. The output of the 465/466 is displayed on an oscilloscope which is being externally triggered by the source (see diagram below). Initially, no output will appear from the 465/466 (see waveforms below). At some duration of overlap, output pulses will always appear. The minimum coincidence overlap is defined in LRS terminology as that amount of overlap which produces one output on the average for every two sets of inputs (i.e., 50% point). From the waveforms below this is equal to T_3-T_1. The 50% point can be quite accurately estimated on the oscilloscope (externally triggered) by adjusting the second pulse delay for equal intensity of trace (of the output states) for the duration of the output pulse. The minimum resolving time for the Model 465/466 is 1.1 nsec. The resolving time jitter can also be measured by taking the difference between 0% limit and the 100% limit (T_3-T_1). The resolving time jitter for the Model 465/466 is +20 psec.



BLOCK DIAGRAM - COINCIDENCE OVERLAP MEASUREMENT W/OSCILLOSCOPE



Coincidence Curve Method of Measuring Resolving Time: An alternate method used at LRS to measure the resolving time and time jitter involves making a coincidence curve and then measuring its "risetime" and "falltime". Two pulses from a single source are initially separated in time and fed into the inputs of the 465 or 466, at the same time being collectively counted in a scaler (see diagrams below). The 465/466 output is also counted into another scaler channel.



BLOCK DIAGRAM - COINCIDENCE OVERLAP MEASUREMENT W/SCALER

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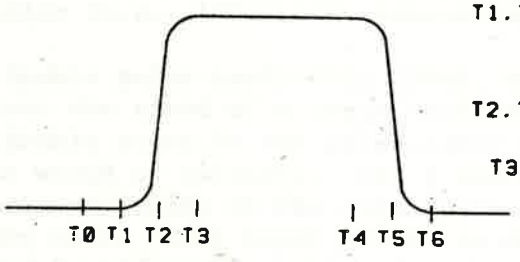
As one pulse is delayed more and more, the two pulses become more and more coincident; by comparing the counts in the two scaler channels at different delay amounts, a curve can be made representing Rate Out/Rate In vs. Time Delay where the time delay is measured from the trailing edge of Pulse A to the leading edge of Pulse B. (The previous waveform diagram is valid for this measurement also, except Pulse A delay should be continued until its leading edge is past the trailing edge of Pulse B.)

The resultant coincidence curve for this measurement would appear as follows:



COINCIDENCE OVERLAP
MEASUREMENT WAVEFORM

T0 - INITIAL TIME OF NON-OVERLAPPED CONDITION

T1.T6 - TIME JUST WHERE THE 465 BEGINS TO DETECT THAT THE TWO PULSES ARE CO-INCIDENT. (I.E. THE 0% FIRING LIMIT)

T2.T5.- TIME AT WHICH RATE OUT EQUALS 50% OF RATE IN. (I.E. 50% TRIGGERING)

T3.T4 - TIME JUST WHERE THE 465 ALWAYS DETECTS BOTH PULSES A AND B IN CO-INCIDENCE (I.E. 100% FIRING POINT) THE COINCIDENCE WIDTH W IS DEFINED AS THE DURATION BETWEEN THE 50% FIRING POINTS (I.E. T5-T2) THE RESOLVING TIME JITTER IS THE TIME DURATION BETWEEN T1 AND T3

The minimum coincidence overlap or minimum resolving time of the logic unit is defined as one-half the difference between the sum of the input pulse widths and the coincidence width measured above. Alternately (but with more difficulty), if t_0 represents the time at which pulse A trailing edge and Pulse B leading edge are exactly coincident in time, then the minimum resolving time is equal to $t_2 - t_0$.

If both input pulses A and B are identical in shape, and if the inputs to the coincidence unit are identical, the trailing edge side of the coincidence curve should be symmetrical to the leading edge side. If they differ, the larger one (either 0% to 100% or 100% to 0%) is specified as the resolving time jitter.

It is important to note that the major contribution toward resolving time jitter in typical logic units is the instability of the "threshold" level of the differential amplifier following the input "AND" stage, particularly for inputs with slow inherent risetimes (i.e., $\geq$ 2 ns). In the 465 and 466, a true high sensitivity discriminator is used which has a very stable and jitter-free threshold (the LD601C hybrid used in all LRS multichannel NIM discriminators). For this reason, the resolving time jitter of the 465/466 is quite small.

Timing Characteristics: Maximum CW rate capability of the 465/466 is guaranteed at 110 MHz. Typically, the maximum rate is 120 MHz, with some units being capable of operation beyond 130 MHz for small bursts of input pulses. The measurement for maximum rate is made by applying pulses to one of the inputs, with the other three inputs either disconnected or set in the OFF position (i.e., internally always enabled at a DC logical 1).

The double pulse resolution (DPR), as opposed to CW rate capability, actually defines the speed of a logic unit in high energy physics applications, since the double pulse or the pulse burst is apt to occur whereas a CW input pulse train would be unlikely. For a coincidence unit like the 465 or 466, the coincidence width of the input pulses would limit the double pulse resolution of the unit. Each input itself is capable of responding to input pulses spaced 8 nsec apart, measured at the FWHM points of the leading edge (i.e., -375 mV point for -750 mV input pulses). Since the minimum coincidence width of the 465/466 is approximately 5 nsec (defined by a 1.1 nsec minimum overlap of two 3.5 nsec pulses in coincidence), the 465 and 466 can actually function as a coincidence circuit, resolving coincidences spaced as narrow as 8 nsec apart.

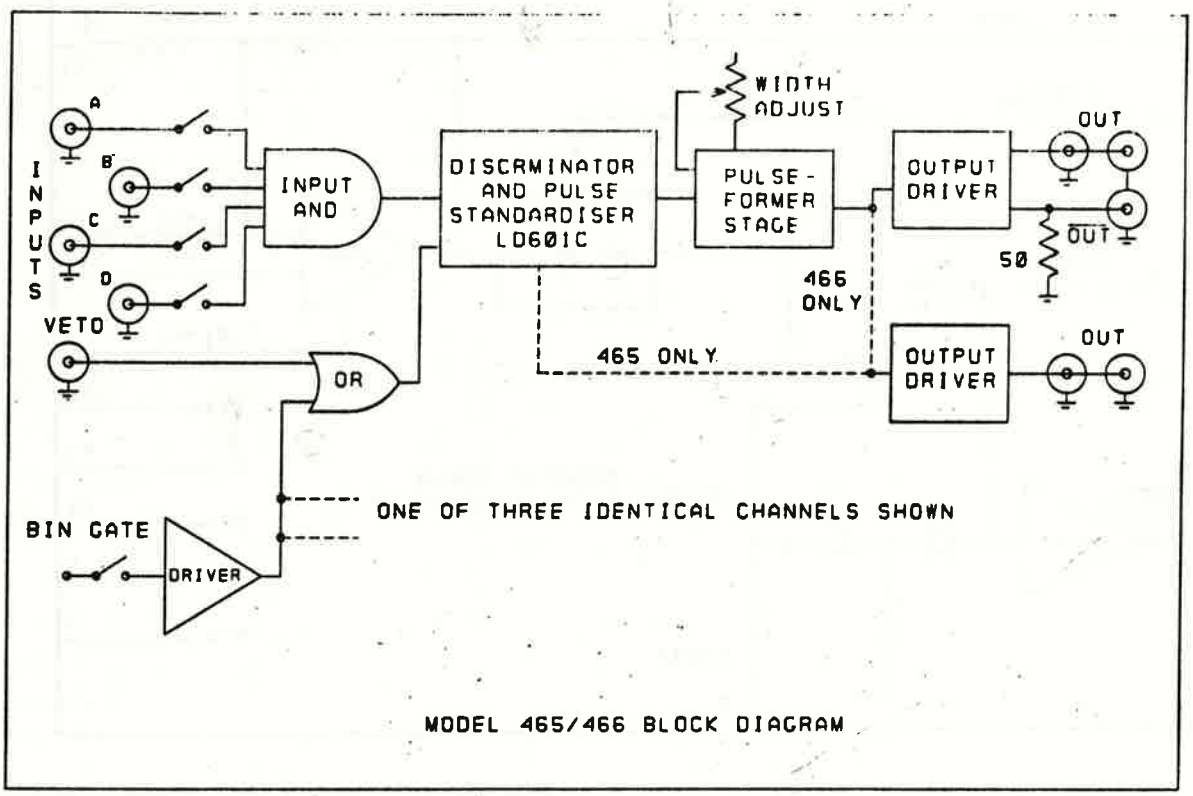
Packaging: The 465 and 466 Triple Coincidence Units are packaged in #1 NIM modules with Lemo-type connectors. Due to front panel space limitations, the 465/466 is not offered with BNC's.

Current Requirements: The current usage of the 465 and 466 will permit the use of modules per standard NIM bin offering 5 A of $\pm$6 V, 2 A of $\pm$12 V, and 1 A of $\pm$24 V. Power calculation works out to 7.1 watts, which does not exceed the 8 watts recommended by the NIM standard for the maximum power dissipation for a single NIM slot. It is recommended that additional -6 volt current be supplied to permit maximum usage of NIM Bin space or that the 465's and 466's are powered in the same NIM bin with other modules not requiring -6 volts.

Recommended Use of the NIM Power Bins: It is highly recommended to keep any NIM bin at as constant a temperature as possible, using air conditioning in the trailer or experimental station and definitely using fans to assure an air flow through all modules in every bin. Elimination of large temperature variations removes the worry of temperature drift effects upon modules of any manufacturer, and the forced air flow is good insurance against the potential failure of components in the modules due to excessive heating for extended periods of time. Despite the fact that all components are pre-aged and burned-in before insertion into LRS modules, and the modules themselves are temperature cycled for days under power between initial test and final test, it is recommended to aviod subjecting any modules to adverse operating conditions if it could be avoided.

General

Each of the three channels of the Models 465 and 466 are composed of four basic sections: the Input AND Stage, the Discriminator and Pulse-Standardizer Stage, the Timing or Pulse-Former Stage, and the Output Stage. A block diagram of the Models 465 and 466 can be seen below, and a complete schematic of the specific model can be found at the end of this manual.

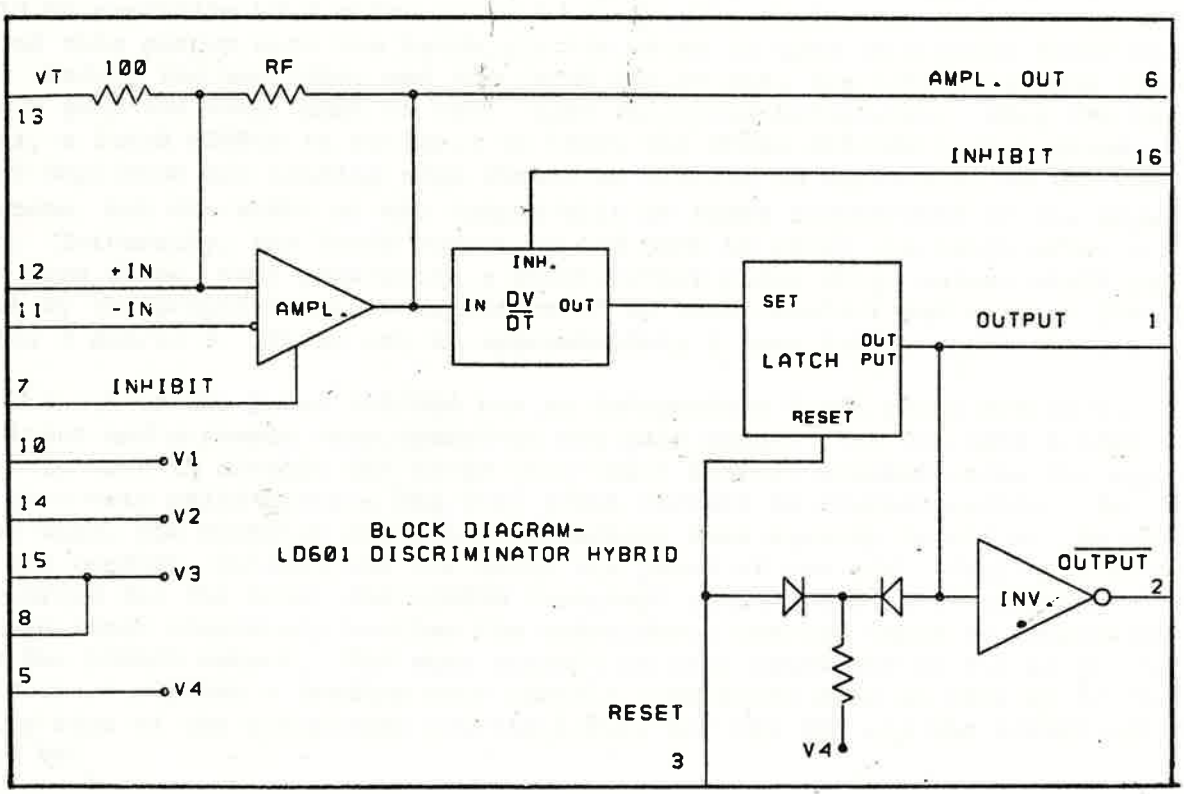


MODEL 465/466 BLOCK DIAGRAM

Input AND Stage

The input stage accepts up to four inputs, each of which can be switched such that the input is disconnected from the internal logic AND gate and a DC logic "1" continuously enables the internal input. The result is the equivalent of a switch-selectable 1-input, 2-input, 3-input, or 4-input AND. This is accomplished with four emmiter-ORed followers driving a discriminator stage which is biased at a negative voltage to compensate for

the base-emitter drop of the transistors while sensing the NIM outputs at the full-width-half-amplitude point when a coincidence overlap occurs. In the special case where all four inputs are switch-disabled, to prevent the LINEAR (Overlap) output of the Model 465 from going high, a diode OR senses the condition and disables the input.



BLOCK DIAGRAM-
LD601 DISCRIMINATOR HYBRID

Discriminator and Pulse Standardizer

The discriminator stage is based on the LRS Model LD601C hybrid. This unit contains all of the circuitry of the discriminator. The LD601C is functionally presented above. The threshold level is set by the voltage bias on a fast differential amplifier which has positive feedback to provide regeneration at threshold. In actual operation the V_T input is tied to -0.8 V and the threshold level is determined primarily by the 19:1 voltage divider composed of the external 1.8 K resistor to -6 V (the 1N4448 diode is not conducting unless a veto or bin gate is present) and the internal 100 Ω resistor. When an input

signal applied to -IN from the Input is equal to the threshold voltage at +IN, the saturating amplifier output will begin to go positive. This will force +IN closer to 0 volts, which increases the differential input voltage in such a direction that the output locks and then the cycle reverses. The amplifier output thus provides a time-over-threshold pulse with fixed amplitude. This pulse can be monitored at the AMPL. OUT point (pin 6). The quiescent level should be nominally -2.4 volts going to -1.6 volts during the pulse. The leading edge of this output sets the latch circuit which is used as a pulse width standardizer. Before the amplifier and the latch can be set, the inhibit inputs (used for the bin gate and veto) must be off. (See following paragraph.) Once the latch is set, a latch OUTPUT is avilable to start the Model 465/466 timing stage. The OUTPUT amplitude and leading edge should be similar in appearance to the AMPL. OUT above, but the width of the output will be fixed independent of the input width. Internally, the latch output is fed back to reset the latch after a short time delay, thus generating a short output pulse whose actual width can be set by the proper external selection of RC time constant and voltage levels at Pins 3 and/or 4. It is set at approximately 3 nsec in the Model 465/466.

Each channel of the Model 465/466 has an independent front panel NIM-level veto input and a common rear connector bin gate input. The bin gate driver output is used to disable the three veto input stages, accomplishing the equivalent to a veto pulse causing the veto input circuit to current-switch. In either case, the normally off diode connecting this circuit to +IN of the LD601C will now conduct, pulling the +IN below the level of the -IN. This type inhibit is required for the Model 465 LINEAR (overlap) output, and it is important that the veto input completely overlap the coincidence overlap input to completely block the LINEAR output. The veto circuit is also connected to Pin 16 of the LD601C to accomplish a leading edge inhibit (requiring only an overlap of the leading edge of the coincidnec overlap input) for the 466 and the PRESET outputs of the 465.

Older Models 465 and 466 units use the LD601B hybrid, while more recent units use LD601C's. These two hybrids are identical and interchangeable.

Timing Stage

The timing or pulse-forming stage of the Models 465 and 466 utilize three stages of MECL MC1692 receiver for amplifying and shaping. The timing is done by first charging a 33 pf capacitor with the pulse from the LD601 (via one MC1692 stage and the differential stage , composed of two A430 transistors) until it is clamped by the FD777 diode to a voltage set indirectly by the front-panel width

potentiometer (via two stages of 747). The discharge rate is set by the current source stage composed of the width potentiometer, one stage of 747, the current source transistor, and its associated 604-ohm emitter resistor. The actual current is varied from near zero (for the 1 μsec maximum width) to about 10 mA for the 5 nsec minimum width). Thus, simultaneously, as the width is increased, the clamp voltage is increased (allowing more initial charge to be stored on the timing capacitor) and the current is decreased (reducing the rate of discharge), thus multiplying the effect of the width control. An internal trim resistor, T_W, sets the minimum width to 5 μsec. The effect of the 2N5962 and the diodes associated with it are to provide fast recovery of the timing capacitor. The MC1692 ECL amplifiers are interconnected in a manner to provide stable leading edge timing and fast risetimes and falltimes of the output pulse. The first amplifier (output pin 3) provides final shaping and standardization of the pulse from the LD601 to the timing stage, as well as driving the preset output stage directly via a second 1692 amplifier (output pin 14). This provides a prompt output pulse for the duration of the 601 output, independent of the delay encountered in initializing the timing stage. Before the 601 output is over, the timing capacitor is charged, causing the third amplifier (output pin 15) to now maintain the pulse level to the output stage (using emitter ORing) until the timing capacitor subsequently discharges to a sufficiently low level (approximately -2.0 volts). At this point, (because of regeneration, the third amplifier promptly switches back to its quiescent off condition, terminating the output pulse.

The Model 465 has one set of bridged outputs which completely bypass the timing stage, receiving their timing and drive directly from the AMPL. OUT of the LD601C. Thus, the output duration is just equal to the FWHM of the overlap of the input pulses.

Output Stage

One output stage of the Model 465 and both outputs of the 466 all utilize a conventional differential stage. This stage requires a continuous 32 mA of current of which 16 mA is quiescently available at the complementary back-terminated output connector. During an output pulse, the MC1692 will switch from the quiescent level of -2.4 volts to a higher level of -1.6 volts, causing the differential stage to switch the 32 mA current from the complementary half of the stage to the normal output connectors for the duration of the pulse. All outputs are diode clamped so they will provide proper operation even without output loads. Without the diode path for the current during the pulse, the

current would have to be supplied via the transistor base, which would severely load the driver and not allow proper drive to the remaining stages. In all cases, the dual bridged outputs should both be terminated in 50 ohms for normal output amplitudes and shape.

The other output stage of the 465 output stages is connected directly to the AMPL. OUT of the LD601. The voltage levels of the LD601 are the same as the MC1692, so the operation is as above.

Internal Power Supplies

Three internal power supplies are used to generate the -0.8, and -2.2, and -11.5V which are special bias voltages used by the three channels. These stages provide voltage regulations and tracking and provide proper temperature compensation for the other sections, particularly the width and threshold circuits. They depend to some degree on uniform heating of the entire circuit board. Heating local areas of the board may cause drifting, but operating in a normal bin environment these supplies compensate to stabilize operation. In all cases, the power supply uses a LM301 operational amplifier to maintain the output voltage of a series-pass transistor equal to an input reference voltage. The reference voltages are adjusted via individual potentiometers or trimmed resistors.

If the -6 voltage is DC sequenced on before the +6 voltage, the LD601C may be forced into a DC latched condition. To prevent this, a relay contact does not supply the -6 VDC until the relay coil, operating from the +6 VDC is energized. This insures that the +6 is up before the -6 in any power-on sequence.

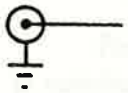
STANDARD DRAFTING SYMBOLS, ELECTRONIC

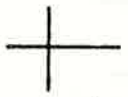

Connection to any given voltage.

Line ending at the edge of the sheet indicates continuance on another sheet.


Male pin or card edge contact.


Female pin, socket or card edge connector.

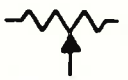

Coaxial connector.


No connection.

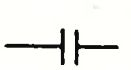

Connection.


Resistor, 1/4 W, ±5%, value in ohms (unless specified otherwise).

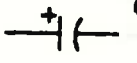
Resistor, 1/4W, ±1%, value in ohms (unless specified otherwise).

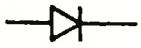

Resistor, variable, any type.


Resistor, variable, any type.

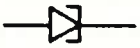

Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).

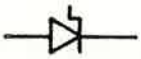

Capacitor, variable. Values in Picofarads (unless specified otherwise).


Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).

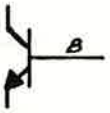

Diode, signal or rectifier.


Diode, zener.


Diode, tunnel.

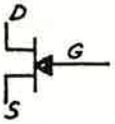

Diode, snap.


Light emitting diode (LED).

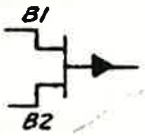


NPN Transistor.

PNP Transistor.



Field effect transistor, P Channel.



Field effect transistor, N.


Air choke.


Ferrite bead.


Ferrite core choke, Z 500 ohms when f ≥ 60 MHz (unless otherwise indicated).


Ferrite core choke, 40 uH, (unless otherwise indicated).

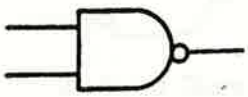
ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
West Nyack, New York

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL).

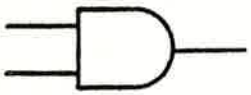
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

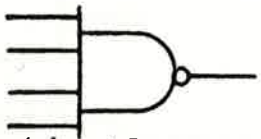
Supply voltages of IC's are shown in a table on each schematic.



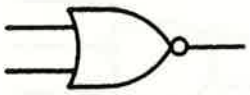
2-Input Positive NAND Gate



2-Input Positive AND Gate

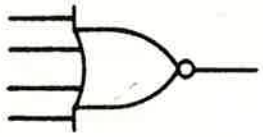


4-Input Positive NAND Gate

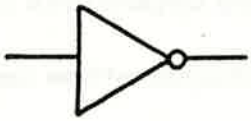


2- Input Positive NOR Gate

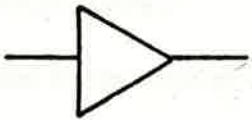
2-Input Positive OR Gate



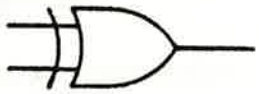
4-Input Positive NOR Gate



Inverter or Inverting Buffer

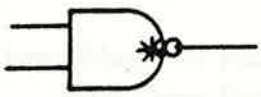


Non-Inverting Buffer

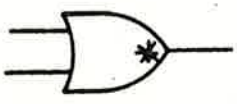


Exclusive OR Gate

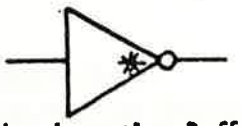
Open collector outputs are identified by an asterisk (*) on the output connection.



2-Input Positive NAND Gate W/Open Collector



2-Input Positive OR Gate W/Open Collector



Non Inverting Buffer W/Open Collector

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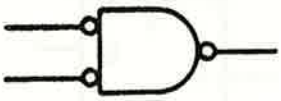
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS
EMITTER - COUPLED LOGIC (ECL)

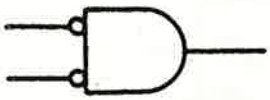
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

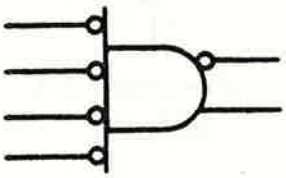
Supply voltages of IC's are shown in a table on each schematic.



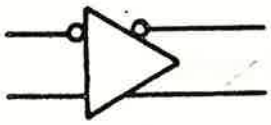
2 - Input Gate.
Negative AND (Positive OR) Gate.



2 - Input Gate.
Negative NAND (Positive NOR) Gate.

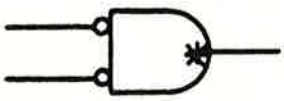


4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.

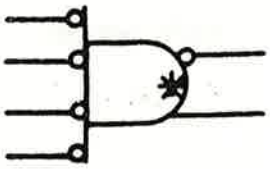


Differential
Amplifier.

Open emitter outputs are identified by an asterisk (*) on the output connection.



2 - Input Negative NAND Gate.
With Open Emitter.



A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.

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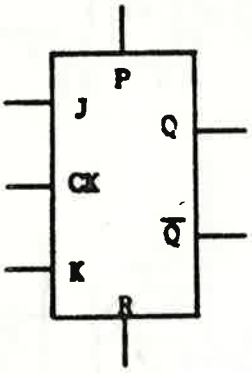
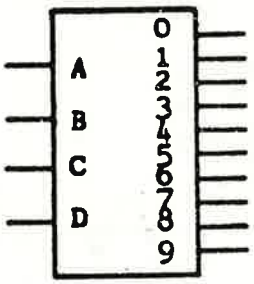
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL) OR EMITTER COUPLED LOGIC (ECL).

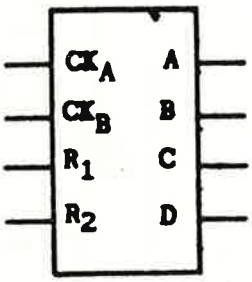
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave Flip-Flop



BCD-To-Decimal Decoder-Driver



Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.

Bottom View

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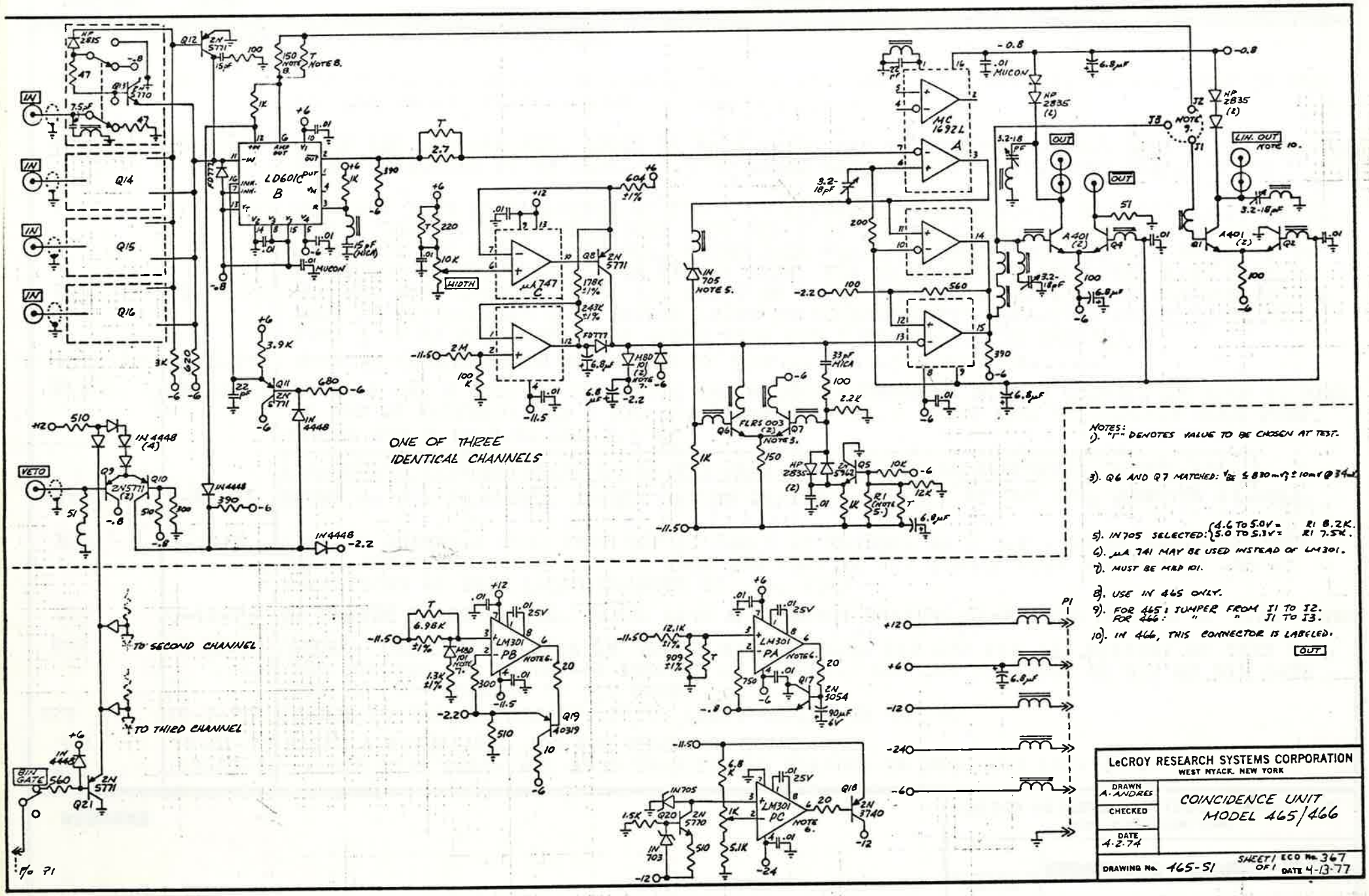

NOTES:
1). "T" DENOTES VALUE TO BE CHOSEN AT TEST.

3). Q6 AND Q7 MATCHED: $V_{BE} \leq 830\,mV$; $\pm 10mV$ @ 3mA

5). IN705 SELECTED: (4.6 TO 5.0V = R1 8.2K.
5.0 TO 5.3V = R1 7.5K.

6). µA 741 MAY BE USED INSTEAD OF LM301.

7). MUST BE MBD 101.

8). USE IN 465 ONLY.

9). FOR 465: JUMPER FROM J1 TO J2.
FOR 466: " " J1 TO J3.

10). IN 466, THIS CONNECTOR IS LABELED. OUT

LeCROY RESEARCH SYSTEMS CORPORATION, WEST NYACK, NEW YORK	
DRAWN A. ANDRES	COINCIDENCE UNIT MODEL 465/466
CHECKED	
DATE 4-2-74	
DRAWING No. 465-51	SHEET 1 OF 1 ECO No. 367 DATE 4-13-77

ECO NO.	DATE	DESCRIPTION
776	8-29-74	FRONT END CIRCUIT CHANGED.
782	10-3-74	SWITCH CONNECTIONS REDESIGNED./ ONE 620 OHM RES., FOUR HPA 2835 DIODES, ONE 3K RES. AND ONE 2N5771 TRANS. ADDED IN EACH CHANNEL.
788	10-31-74	15 pF AND 100 OHM RES. ADDED AT EACH LD601 PIN 11 TO GROUND./ ALL TWENTY FOUR 51 OHM TERM. RESISTORS TO 47 OHMS./ 7.5 pF ADDED EACH SWITCH INPUT, WITH BEAD, TO GND.
792	11-21-74	DELETED: 3-18 pF CAPACITOR AT PIN 6 OF MC1692L./ BEAD REMOVED FROM OUT OUTPUT LINE./ ADDED: 300 OHM & "T" RESISTORS FROM PIN 2 OF LD601B./ CHANGED: 82 OHMS AT PIN 6 OF LD601B TO 150 OHMS - TRIM RES. ADDED SAME PLACE./ CIRCUIT BETWEEN PIN 16 AND Q 10 COLLECTOR ADDED./ CONNECTION BROKEN BETW. PIN 16 OF LD601B AND OTHER PINS SAME IC.
805	1-24-75	500 OHM POT. CHANGED TO 1K (AT PIN 2 OF LM301 "PC")/8.2K AT Q5-BASE CHANGED TO R1, NOTE #5 REVISED/BIN GATE SWITCH SHOWN IN SCHEMATIC/"T" CAPACITOR ADDED TO IC "A" PINS 3 TO 6/ 22pF CAPACITOR ADDED FROM PIN 1 OF MC1692L TO GROUND/
812	2-6-75	NOTE #5 CORRECTED TO READ: 4.6 TO 5.0V.....5.0 TO 5.3V...../
813	2-12-75	NOTES 2 AND 8 OMITTED SCHEMATIC AND ASSEMBLY DRAWING. NOTE 3 CHANGED ON BOTH TO READ Q6 AND Q7 MATCHED: V_{BE} 830 mV; ±10mV @ 34 mV./ PARTS LIST TO INCLUDE BOTH POSS. VALUES FOR R 1: 8.2K AND 7.5 K/
		ALL ABOVE ECOS REFER TO MODEL 465 ONLY. ALL FOLLOWING ECOS REFER TO 465/466.
819	2-26-75	NOTES 8, 9 & 10 ADDED. JUMPER OPTION J1/J2/J3 ADDED./ 27 OHM RES. REMOVED Q2-COLL.
824	3-5-75	IN EACH CHANNEL: CHG. TRIM CAP AT PIN 6 OF MC1692L TO A 3.2 - 18 pF VARIABLE/ RES. BETW. "B"-2 AND "A"-7 CHANGED FROM 300 OHMS TO 2.7 OHMS./ NOTE 4 DELETED/ .05 uF CAPACITORS AT EACH LM301 CHANGED TO .01, 25V/
827	3-12-75	NO CHANGE TO SCHEMATIC. PARTS LIST & ASSEMBLY DRAWING CORRECTED (NUMBER OF 6.8uF USED)
878	6-26-75	ADDED: 100 OHM RESISTOR IN SERIES W/33 pF MICA CAP OFF PIN 13, MC1692/ AT BASE Q11: 680 OHM RES. TO GO TO -6V INSTEAD OF GROUND./ 680 OHM RESISTOR AT END OF BIN GATE BUS TO +12V CHANGED TO 510 OHMS/
929	10-7-75	CHANGE TO NEW WRAPAROUND: PARTS LIST. TAPING /A to /B.
961	10-21-75	RELAY & ASSOCIATED 100 OHM RESISTOR ELIMINATED.
995	12-22-75	PARTS LIST ONLY: ALL 2430 TRANSISTORS CHANGED TO FLRS 003 (FMT1190).

REMARKS

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN
CHECKED
DATE

ENGINEERING CHANGE ORDERS

MODEL 465/466
SHEET 1 OF 2

DRAWING No.

ECO NO.	DATE	DESCRIPTION
059	2-19-76	FOLLOWUP OF ECO 995: ALL OUTPUT TRANSISTORS CHANGED TO A 401, WITH A FULL BEAD ON EACH BASE/ Q6 & Q7 (MATCHED PAIR) CHANGED TO FLRS 003/ ALL OUTPUT BEADS REMOVED/ A 3.2 - 18 pF TRIMMER ADDED IN SERIES WITH BEAD FROM EACH BRIDG. OUTPUT TO GROUND.
075	3-16-76	ALL DOCUMENTATION: MBD 101 CHANGED TO HP2835, - IN 18 PLACES./ PRINTED CKT. ONLY: TAPING CORRECTIONS/ PARTS LIST ONLY: HARDWARE CORRECTED/ SCHEMATIC ONLY: CONNECTION FROM J3 CORRECTED _ MUST GO TO PIN 14 OF MC1692L.
195	6-23-76	AT MC1692, betw. Pins 14 AND 15: TWO FULL BEADS ADDED/ OFF BASE OF Q3: ONE BEAD DELETED, 18 pF CAPACITOR CHANGED TO 3.2 - 18pF TRIMMER/
367	4-13-77	REMOVED 1.8K RESISTOR AT PIN 12 OF LD-601C(ONE PER CHANNEL).

REMARKS

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN	ENGINEERING CHANGE ORDERS
CHECKED	MODEL 465/466
DATE	SHEET 2 OF 2
DRAWING No.	