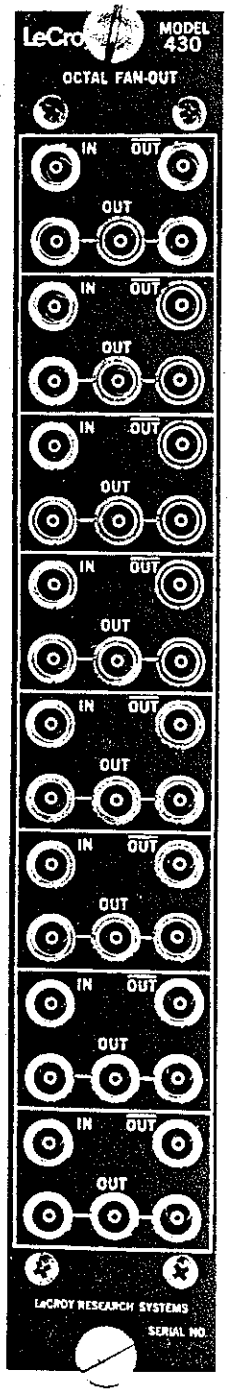
4426

TECHNICAL DATA

LeCroy
RESEARCH SYSTEMS



NIM Model 430

Octal Logic Fan-Out

* **8 channels in a single-width module**
* **4 outputs per channel**
* **Maximum rate >150 MHz**
* **Direct coupled**
* **Stage delay <2.5 nsec**
* **Low power dissipation permits up to 96 fan-out channels (384 outputs) per standard bin**

The LeCroy Model 430 Octal Logic Fan-out provides a unique combination of high fan-out and performance in an exceptionally compact unit. Designed for flexibility in both small and large scale experiments, the 430 offers eight independent channels, each of which supplies three normal and one inverted outputs.

The input to each channel is terminated in 50 Ω and may be driven with either single or double amplitude NIM level signals. The output amplitude is independent of input signal overdrive and the high-speed circuitry accurately restandardizes amplitudes of all input signals of width greater than 4 nsec. The normal outputs are generated by a current source which delivers −48 mA into three bridged connectors. The voltage swing is limited to approximately −900 mV, and unused outputs do not require termination to control signal amplitude. The complementary output delivers −16 mA in a 50 Ω load.

The circuitry of the Model 430 is completely direct coupled and compatible with normal or complementary logic signals in any duty ratio. The wideband design permits operation at rates in excess of 150 MHz. Stage delays of less than 2.5 nsec assist in minimizing logic system decision time and provide good time resolution (absolute delay and jitter) between all channels.

The 430 is packaged in an RF-shielded single-width NIM Module utilizing LEMO connectors. Power dissipation is within standard limits, permitting 12 modules (96 independent fan-out channels) to be housed in one bin.

October 1977

TELEPHONE: (022) 34 39 23 • TELEX: 28230
LeCROY EUROPEAN PRODUCTS DIVISION • 81, AVENUE LOUIS CASAI • 1216 COINTRIN-GENEVA, SWITZERLAND

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, NEW YORK 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPONE: (914) 425-2000

Innovators in Instrumentation

SPECIFICATIONS
NIM Model 430
OCTAL LOGIC FAN-OUT

Number of Sections:	Eight.
INPUT CHARACTERISTICS	
Number of Inputs:	One per section.
Impedance:	50 Ω ± 5%.
Reflections:	<10% for input risetimes ≥ 2nsec.
Quiescent Level:	0 volts dc.
Signal Level Requirements:	Standard NIM logical 1 input levels; −12 mA to −36 mA into 50 Ω.
Signal Width Requirements:	4 nsec minimum, FWHM.
Coupling:	Direct.
OUTPUT CHARACTERISTICS	
Number of Outputs:	3 normal (bridged); 1 complementary.
Output Levels:	Normal: quiescently 0 volts, >−700 mV into 50 Ω during output; complementary; quiescently >−700 mV into 50 Ω, 0 volts during output.
Risetimes & Falltimes:	<2.5 nsec.
Duration:	Equal to the input duration.
Time Variation Between Channels:	<0.5 nsec.
GENERAL	
Rate:	>150 MHz.
Stage Delay:	<2.5 nsec.
Duty Cycle Limitations:	None.
Packaging:	Single-width NIM module; in conformance with AEC standard for nuclear modules (AEC Report TID-20893): Lemo-type connectors.
Current Requirements:	+6 V at 100 mA −6 V at 510 mA

technical information manual

NIM Model 430
Octal Logic Fan-Out

WARRANTY

All LeCroy instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform with in specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

LeCroy
RESEARCH SYSTEMS SA

EUROPEAN PRODUCTS DIVISION

AVENUE LOUIS-CASAI 81
1216 COINTRIN-GENÈVE SUISSE

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refine and improve the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Geneva, telephone 022/98.97.97, or from your local distributor in countries other than Switzerland.

LeCROY RESEARCH SYSTEMS

OPERATION

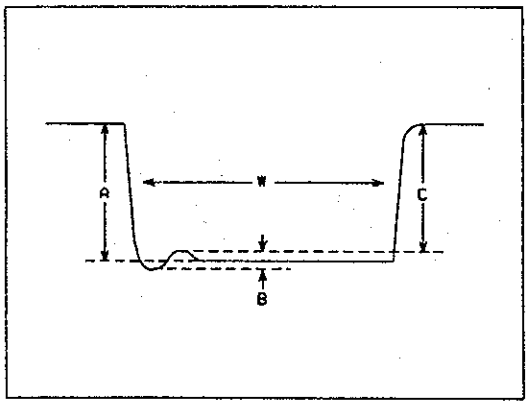
Input Characteristics

Logic Inputs: The Model 430 has direct-coupled, 50 Ohm impedance inputs which accept fast NIM logic signals (-0.6 V to -1.8V). These inputs, typically driven from a discriminator or other logic unit, will accept transient and DC signals up to -2.5 volts. Since the input reflections are less than 7% for signals of as little as 2nsec risetime, even the maximum level signal in the NIM-specified range for a logic input (i.e., -1.8 volts) will reflect only approximately 125mV, eliminating the probability of accepting multiple pulses corresponding to only one original input pulse.

Output Characteristics

Negative Outputs: The Model 430 has a common current source output, delivering -48 mA of current during the output and 0 mA quiescently. Diode limiters hold the maximum output swing to -1.2V into 50 Ohm. These outputs are of the switched current source type. The standard switched current outputs maintain a risetime of 2.5 nsec. and unused outputs need not be terminated.

The specifications of the output shape are indicated below.



AMPLITUDE: -700mV<A<- 1.2V

OVERSHOOT: B<10% OF A; C DOES NOT REACH -600mV

RISETIME: <2.5 NSEC.

FALLTIME: <2.5 NSEC.

MINIMUM WIDTH. WMIN (FWHM) <4.0 NSEC.

Complementary Output: The single complementary output is obtained from the collector of the differential pair supplying current to the outputs. Its quiescent level is at -16mA and logical 1 at 0 mA. Risetime and other characteristics are similar to that of the negative outputs.

Output Width: The output duration of the Model 430 is equal to the input signal duration. It maintains this equilivance at ± 1 ns for all durations from > 4ns to dc.

Timing Characteristics: Maximum CW rate capability of the 430 is guaranteed at 150 MHz. Typically, the maximum rate is 200 MHz. The measurement for maximum rate is made by applying 4ns FWHM pulses to the input and observing the output.

The double pulse resolution (DPR), as opposed to CW rate capability, actually defines the speed of a logic unit in high energy physics applications, since the double pulse or the pulse burst is apt to occur, whereas a CW input pulse train would be unlikely. This is measured by putting in two 4 nsec maximum FWHM pulses spaced approximately 10 nsec apart at the half maximum points (i.e., -375mV for a -750mV input signal) and finding how far this 10 nsec time difference can be lowered before the 430 output pulses merges together and can not be separated according to NIM standard. Care should be taken to use pulses of as narrow a width as possible when measuring minimum double pulse resolution.

Packaging: The 430 Octal Logic Fan-Out is packaged in a no.1 NIM module with Lemo-type connectors. Due to front panel space limitations, the 430 is not offered with BNC's.

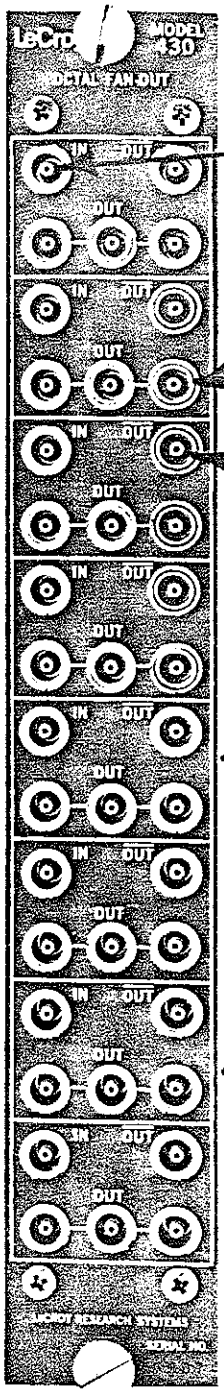
Power Requirements: The current usage of the 430 is low enough to permit the use of the 12 modules per NIM bin offering 6.5 A of -6 V,1A of +6V. The power dissipation is < 4.5 watts, which does not exceed the 8 watts recommended by the NIM standard for the maximum power dissipation for a single NIM slot.

GENERAL :

Recommended Use of the NIM Power Bins: It is highly recommended to keep any NIM bin at as constant a temperature as possible, using air conditioning in the trailer or experimental station and definitely using fans to assure an air flow through all modules in every bin. Elimination of large temperature variations removes the worry of temperature drift effects upon modules of any manufacturer, and the forced air flow is good insurance against the potential failure of components in the modules due to excessive heating for extended periods of time. Despite the fact that all components are pre-aged and burned-in before insertion into LRS modules, and the modules themselves are temperature cycled for days under power between initial test and final test, it is recommended to avoid subjecting any modules to adverse operating conditions if it could be avoided.

CIRCUIT DESCRIPTION

The input stage of the 430 is a PNP differential pair consisting of Q1 and Q2. Resistor R2 provides 10 mA of quiescent current to Q1. The base of Q1 is biased by hot carrier diode CR1 at approximately -400 mV. A NIM level input signal of 600 millivolts or greater at the base of Q2 switches the standing current from Q1 to Q2. The collectors of Q1 and Q2 drive the bases of Q3 and Q4 respectively. Q3 and Q4 are also a differential pair, made up of high current NPN transistors. Resistors R4 and R9 provide a standing emitter current of approximately 50 mA. Q3 is quiescently off and drives a resistor to GND in parallel with a single complementary output. Q4 is quiescently off and drives three normal outputs in parallel. Series diodes CR2, CR3 and CR4 from ground limit the amplitude of the normal outputs when less than three outputs are used.



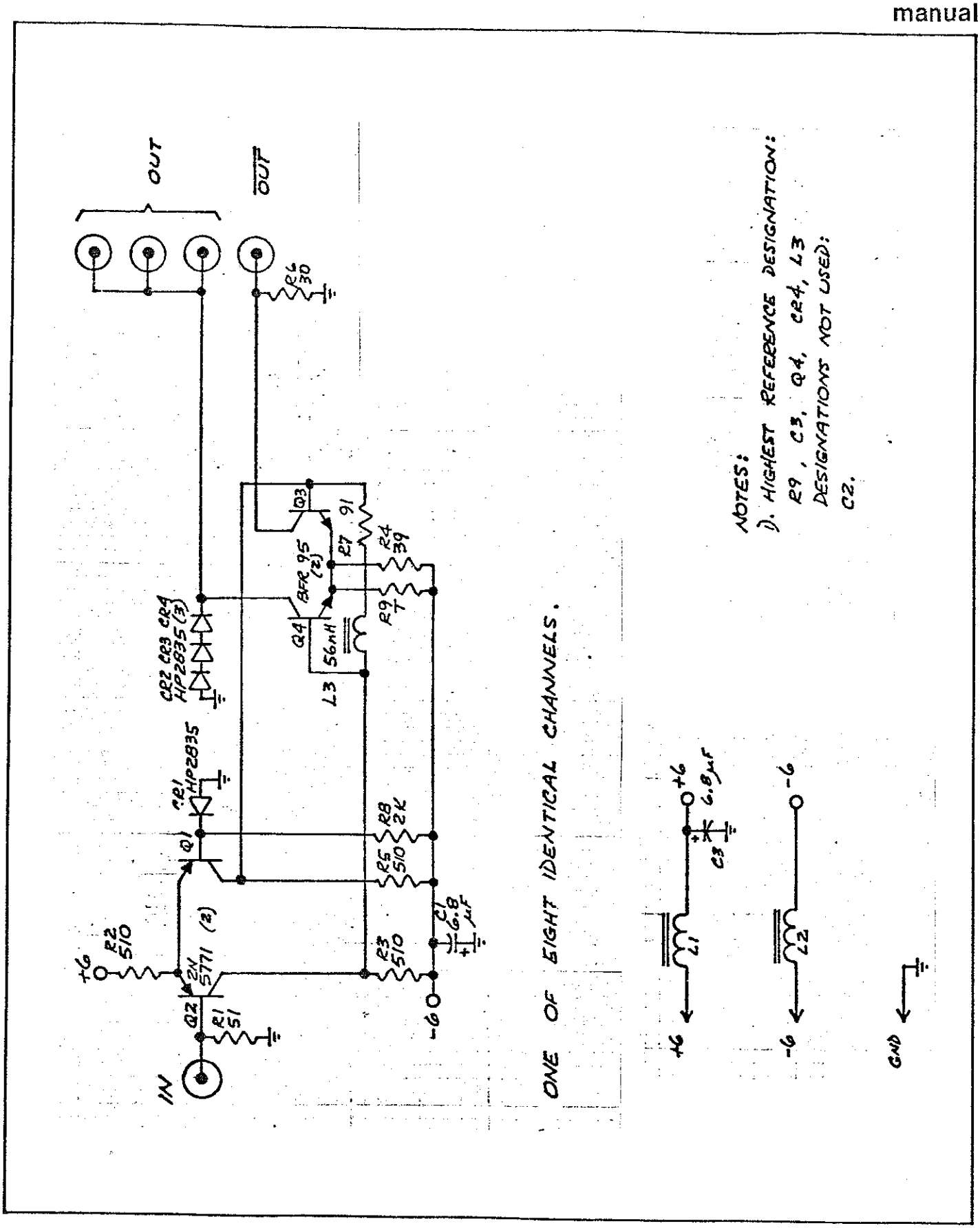
50 Ohm inputs; require NIM fast logic level (< - 600 mV)

3 negative outputs; quiescently OmA, - 16 mA during output

1 complementary output; quiescently - 16 mA, O mA during output

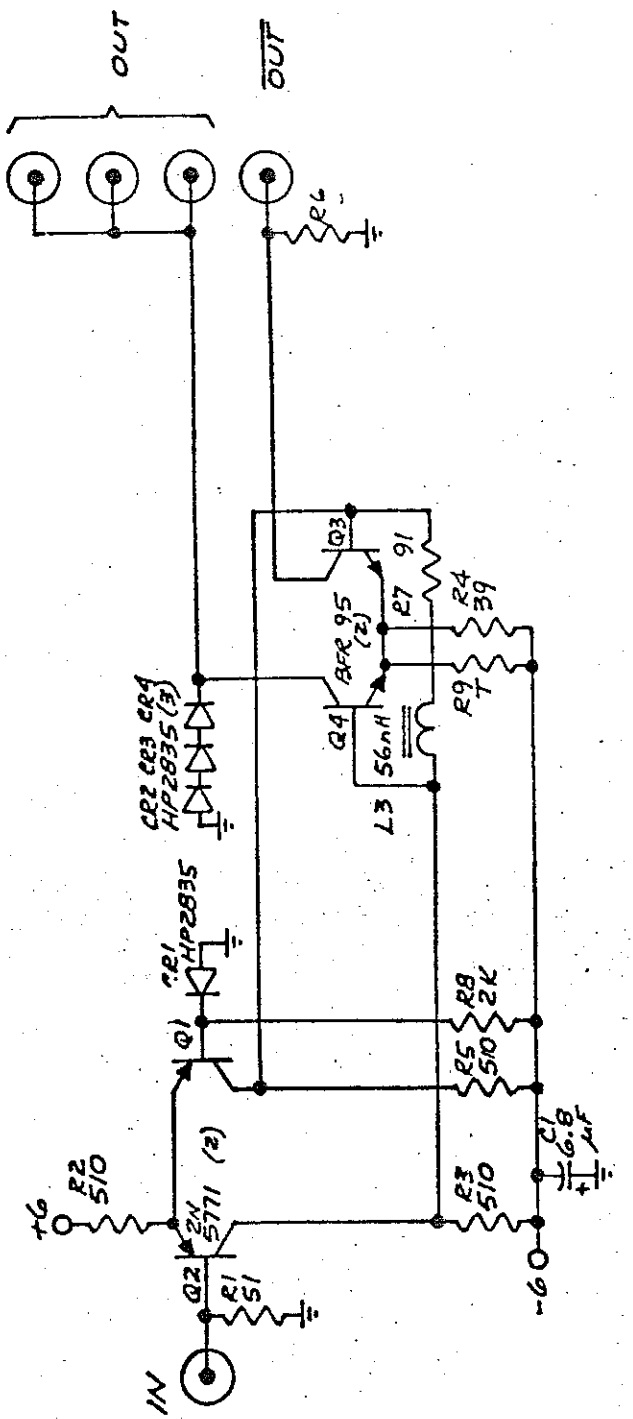
Stage delay < 2.5 ns

Single width NIM module;
requires 90 mA of + 6 V, 540 mA of -6V.

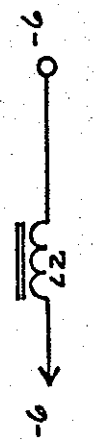


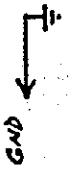
ONE OF EIGHT IDENTICAL CHANNELS.

NOTES:
1). HIGHEST REFERENCE DESIGNATION:
R9, C3, Q4, C24, L3
DESIGNATIONS NOT USED:
C2.



ONE OF EIGHT IDENTICAL CHANNELS.





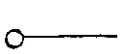
NOTES:

1). HIGHEST REFERENCE DESIGNATION:
R9, C3, Q4, C24, L3
DESIGNATIONS NOT USED:
C2.

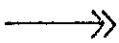
OUT
OUT
RL
CR2 CR3 CR4
HP2835 (3)
CR1
HP2835
Q1
2N
5711 (2)
Q2
R2
510
+6
IN
Q3
R7
91
R4
39
Q4
BFR 95
(2)
56nH
L3
R9
T
R8
2K
R5
50
R3
510
C1
6.8
µF
-6
NOTES:
1). HIGHEST REFERENCE DESIGNATION:
R9, C3, Q4, L24, L3
DESIGNATIONS NOT USED:
C2.
ONE OF EIGHT IDENTICAL CHANNELS.
+6
6.8µF
C3
L1
+6
-6
L2
-6
GND

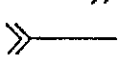
430N

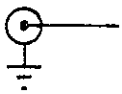
STANDARD DRAFTING SYMBOLS, ELECTRONIC


Connection to any given voltage.

Line ending at the edge of the sheet indicates continuance on another sheet.


Male pin or card edge contact.


Female pin, socket or card edge connector.


Coaxial connector.


No connection.


Connection.

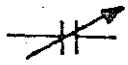

Resistor, 1/4 W, ±5%, value in ohms (unless specified otherwise).

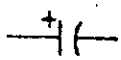
Resistor, 1/4W, ±1%, value in ohms (unless specified otherwise).

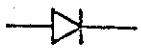

Resistor, variable, any type.

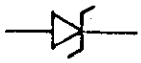

Resistor, variable, any type.

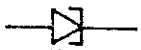

Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).


Capacitor, variable. Values in Picofarads (unless specified otherwise).


Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).

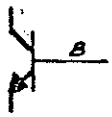

Diode, signal or rectifier.


Diode, zener.

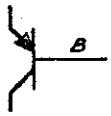

Diode, tunnel.


Diode, snap.

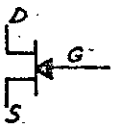

Light emitting diode (LED).



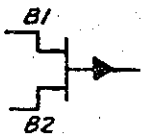
NPN Transistor.



PNP Transistor.



Field effect transistor, P Channel.



Field effect transistor, N.


Air choke.


Ferrite bead.


Ferrite core choke, Z 500 ohms when f > 60 MHz (unless otherwise indicated).

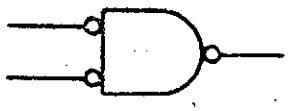

Ferrite core choke, 40 uH, (unless otherwise indicated).

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS EMITTER - COUPLED LOGIC (ECL)

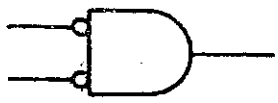
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

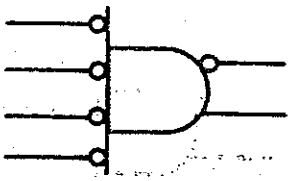
Supply voltages of IC's are shown in a table on each schematic.



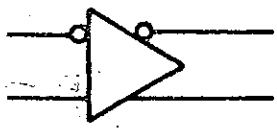
2 - Input Gate.
Negative AND (Positive OR) Gate.



2 - Input Gate.
Negative NAND (Positive NOR) Gate.

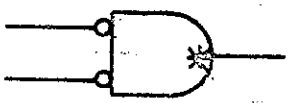


4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.

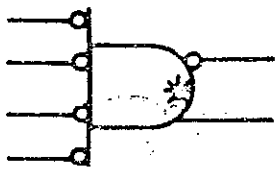


Differential
Amplifier.

Open emitter outputs are identified by an asterisk (*) on the output connection.



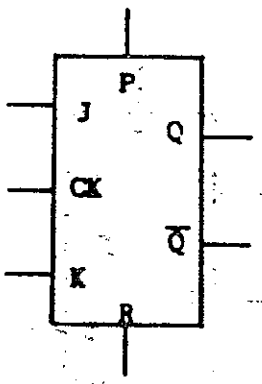
2 - Input Negative NAND Gate.
With Open Emitter.



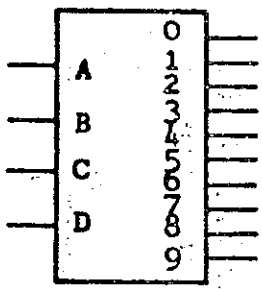
A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL) OR EMITTER COUPLED LOGIC (ECL).

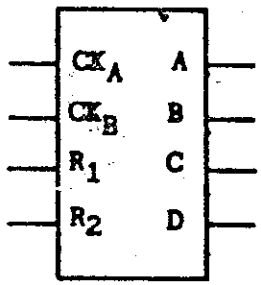
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave Flip-Flop

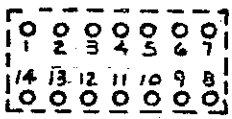


BCD-To-Decimal Decoder-Driver



Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.



Bottom View

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL).

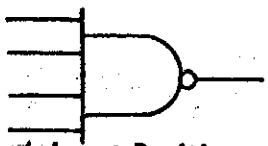
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

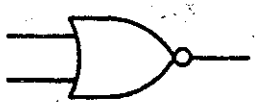
Supply voltages of IC's are shown in a table on each schematic.

2-Input Positive NAND Gate

2-Input Positive AND Gate

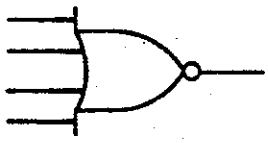


4-Input Positive NAND Gate

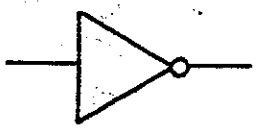


2- Input Positive NOR Gate

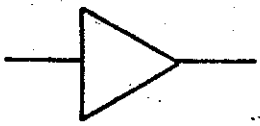
2-Input Positive OR Gate



4-Input Positive NOR Gate



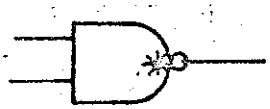
Inverter or Inverting Buffer



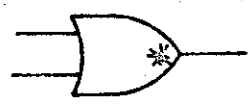
Non-Inverting Buffer

Exclusive OR Gate

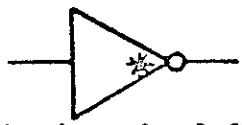
Open collector outputs are identified by an asterisk (*) on the output connection.



2-Input Positive NAND Gate W/Open Collector



2-Input Positive OR Gate W/Open Collector



Non Inverting Buffer W/Open Collector