

22 MARS 1976

TECHNICAL DATA

LRS

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NIM Model 429

Quad Logic Fan-In/Fan-Out



The LRS Model 429 represents a new advance in efficient fast logic signal handling. It combines in one low cost unit three functions formerly available only separately: fan-in, fan-out, and polarity inversion. Each channel of the Model 429 contains four independent logic inputs, four normal logic outputs, and two complementary logic outputs. Channels may be paralleled to provide up to 16 inputs and 24 outputs by means of a front-panel switch. An efficient circuit design holds the power dissipation of the entire module to within the NIM standard.

The Model 429 eliminates the extra cabling and time delay involved when conventional fan-ins and fan-outs must be cascaded. In addition, it eliminates the common use of expensive logic units to perform logical OR-ing with adequate fan-out. The ability to conveniently parallel channels permits the 429 a degree of flexibility and efficiency heretofore unavailable.

Inputs are 50Ω impedance. Unused inputs need not be terminated. Inputs may be driven with either single or double amplitude NIM signals without affecting output amplitude. The three pairs of bridged outputs are direct-coupled current sources which deliver -32 mA into two 50Ω loads. Output duration is equal to the logical sum of the input durations.

The circuitry of the Model 429 is completely direct-coupled and compatible with either normal or complementary logic signals in any duty ratio. Channel paralleling is accomplished by means of a single front-panel locking switch that is not in the signal path and hence permits switching with minimal effect on signal fidelity. Front-panel lamps located between channels light to indicate channels that are combined, providing a clear, easily interpreted display of the unit's status.

December 1974

Innovators In Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • WEST NYACK, NEW YORK 10994 • TELEPHONE: (914) 358-7900

SPECIFICATIONS

NIM Model 429

QUAD LOGIC FAN-IN/FAN-OUT

Number of Sections: Four; may be cascaded by means of front-panel switch to form dual 8-fold fan-in/12-fold fan-out or single 16-fold fan-in/24-fold fan-out, with LED indication.

INPUT CHARACTERISTICS

Number of Inputs: Four per section.

Impedance: $50\Omega \pm 5\%$.

Reflections: $< 10\%$ for input risetimes ≥ 2 ns.

Quiescent Level: 0 volts dc.

Signal Level Requirements: Standard NIM logical 1 input levels: -12 mA to -36 mA into 50Ω .

Signal Width Requirements: 4 ns minimum, FWHM.

Coupling: Direct.

OUTPUT CHARACTERISTICS

Number of Outputs: 4 normal (2 bridged pairs); 2 complementary (1 bridged pair).

Output Levels: Normal: quiescently 0 volts, > -700 mV into 50Ω during output; complementary: quiescently > -700 mV into 50Ω , 0 volts during output.

Risetimes and Falltimes: < 2 ns.

Duration: Equal to the logical sum of the input durations.

Time Variation of Output with Input Amplitude: < 1 ns worst case between inputs of -600 mV and -1.6 volts; typically < 0.5 ns.

Time Variation Between Outputs: 4 channels, 4 x 6 operation: < 0.2 ns;
2 channels, 8 x 12 operation: < 0.4 ns;
1 channel, 16 x 24 operation: < 0.6 ns.

GENERAL

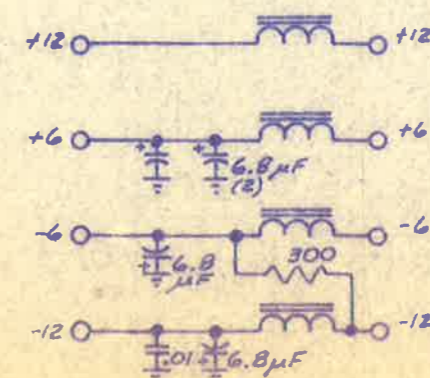
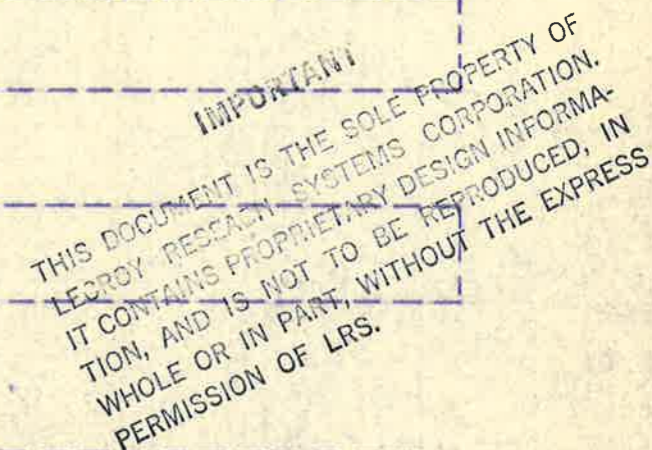
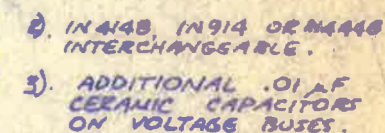
Rate: > 100 MHz.

Stage Delay: < 6.5 ns.

Duty Cycle Limitations: None.

Packaging: Single-width AEC/NIM module; in conformance with AEC standard for nuclear modules (AEC Report TID-20893); Lemo-type connectors.

Current Requirements: $+12$ V at 40 mA $+6$ V at 130 mA
 -12 V at 45 mA -6 V at 410 mA



SHEET / ECO No. 900
Of / PAGE 7-24-7

ECO NO.	DATE	DESCRIPTION
783	10-3-74	EMITTERS OF Q1 THRU Q5: 390 OHM RES. TO +6V CHANGED TO 330 OHMS.
785	10-11-74	PARTS LIST ONLY: COMPONENT COUNT CORRECTED.
800	12-12-74	ONE MBD 101 EACH OUTPUT CHANGED TO TWO HP 2835-s.
856	5-14-75	ONE SWITCHING DIODE ADDED TO EACH LED TO PREVENT REVERSE BIAS BREAKDOWN.
866	6-12-75	EMITTER RESISTOR OF Q6 CH. FROM 1.5 K TO 1.2 K/ EMITTER RESISTOR OF Q7 FROM 68 TO 91
887	7-11-75	BASE RESISTOR FOR Q10 & Q11 CHANGED FROM 390 OHMS TO 820 OHMS.
900	7-24-75	CHANGE 330 OHM RES AT Q1, 2, 3, 4 & 5 TO 200 OHMS/ ADD 91 OHMS FROM Q1, 2, 3, 4 & 5 TO -3 VOLTS/ CHANGE 68 OHMS AT Q 6 BASE TO 91 OHMS/ CHANGE 620 OHMS AT Q 7 EMITTER TO 470 OHMS/ REMOVE 91 OHMS AT Q7 EMITTER/ ADD 91 OHMS AT Q 8 & Q 9 BASE TO -3 VOLTS /CHANGE 820 OHMS AT Q 11 & Q 10 BASE TO 430 OHMS/ REMOVE 7.5 pF WITH BEAT FROM Q 12 & Q 15, ALSO FROM Q 13 & Q 14/ CHANGE Q 1, 2, 3, 4 & 5 FROM 2N5771 TO SAB 4113/ DELETE MATCHING OF ALL TRANSISTORS/ ***** ALL 2N5054 TRANSISTORS CHANGED TO A430 TO COMPLY WITH ECO #873, A BLANKET ECO TO MAKE THIS CHANGE IN ALL MODULES. *****
925	10-7-75	CHANGE TO NEW WRAPAROUND: PARTS LIST. TAPING FROM /C to /D.

REMARKS

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN

ENGINEERING CHANGE ORDERS









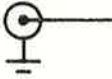


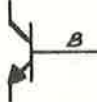

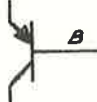

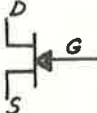

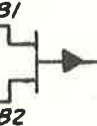








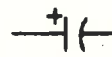
CHECKED

MODEL 429

DATE

DRAWING No.

STANDARD DRAFTING SYMBOLS, ELECTRONIC

	Connection to any given voltage.		Diode, signal or rectifier.
	Line ending at the edge of the sheet indicates continuance on another sheet.		Diode, zener.
	Male pin or card edge contact.		Diode, tunnel.
	Female pin, socket or card edge connector.		Diode, snap.
	Coaxial connector.		Light emitting diode (LED).
	No connection.		NPN Transistor.
	Connection.		PNP Transistor.
	Resistor, 1/4 W, ±5%, value in ohms (unless specified otherwise).		Field effect transistor, P Channel.
	Resistor, 1/4 W, ±1%, value in ohms (unless specified otherwise).		Field effect transistor, N.
	Resistor, variable, any type.		Air choke.
	Resistor, variable, any type.		Ferrite bead.
	Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).		Ferrite core choke, Z 500 ohms when $f > 60$ MHz (unless otherwise indicated).
	Capacitor, variable. Values in Pico-farads (unless specified otherwise).		Ferrite core choke, 40 uH, (unless otherwise indicated).
	Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).		

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL).

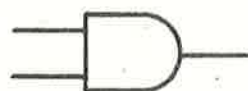
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

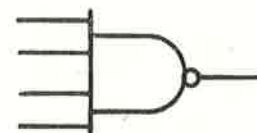
Supply voltages of IC's are shown in a table on each schematic.



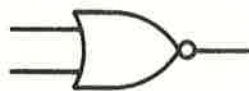
2-Input Positive
NAND Gate



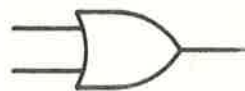
2-Input Positive
AND Gate



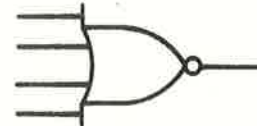
4-Input Positive
NAND Gate



2- Input Positive
NOR Gate



2 -Input Positive
OR Gate



4-Input Positive
NOR Gate



Inverter or
Inverting Buffer



Non-Inverting
Buffer

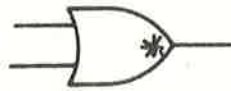


Exclusive
OR Gate

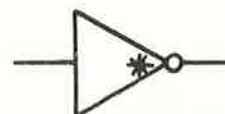
Open collector outputs are identified by an asterisk (*) on the output connection.



2-Input Positive NAND
Gate W/Open Collector



2-Input Positive OR
Gate W/Open Collector



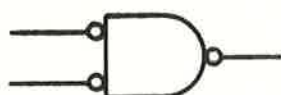
Non Inverting Buffer
W/Open Collector

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS EMITTER - COUPLED LOGIC (ECL)

The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

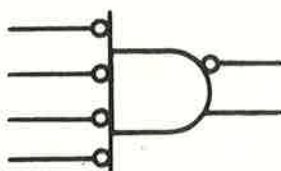
Supply voltages of IC's are shown in a table on each schematic.



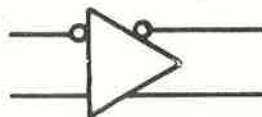
**2 - Input Gate.
Negative AND (Positive OR) Gate.**



**2 - Input Gate.
Negative NAND (Positive NOR) Gate.**

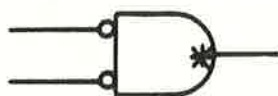


**4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.**

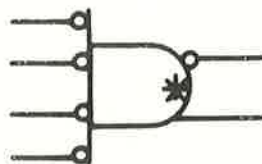


**Differential
Amplifier.**

Open emitter outputs are identified by an asterisk (*) on the output connection.



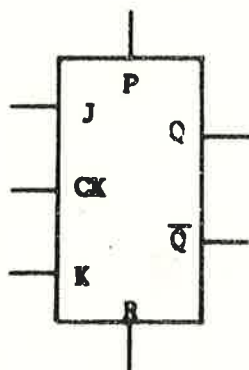
**2 - Input Negative NAND Gate.
With Open Emitter.**



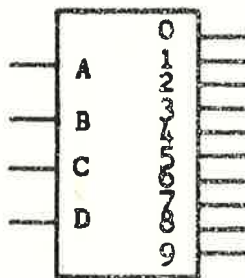
**A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.**

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS.
TRANSISTOR - TRANSISTOR LOGIC (TTL) OR
EMITTER COUPLED LOGIC (ECL).

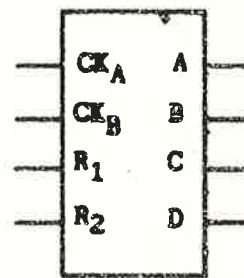
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave
Flip-Flop



BCD-To-Decimal
Decoder-Driver



Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.



Bottom View