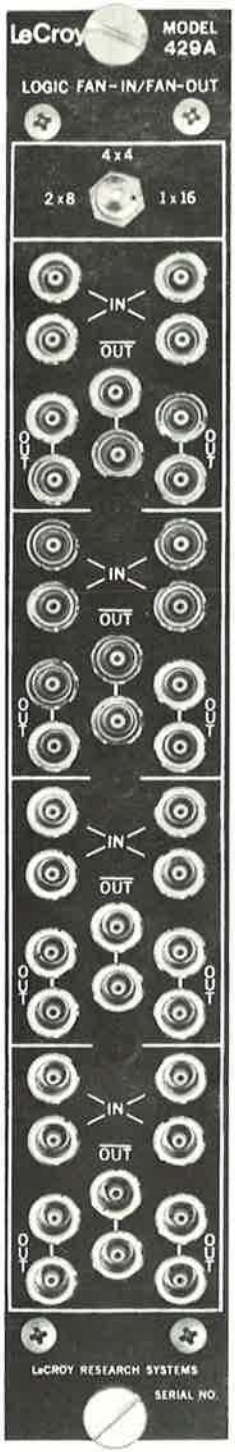
TECHNICAL DATA

LeCroy RESEARCH SYSTEMS



NIM Model 429A

Quad Mixed Logic Fan-In/Fan-Out

The LeCroy Model 429A is a *multifunctional* fast logic module designed to fulfill a wide variety of signal handling needs. It combines the operations of TTL-to-NIM level translation, logic fan-in, logic fan-out, and polarity inversion in one low-cost module. Each of the four channels of the Model 429A has four inputs which accept both NIM and TTL levels. This is particularly important for present generation experiments involving MWPC systems and elaborate digital triggers.

Each channel of the Model 429A contains four independent logic inputs, four normal logic outputs, and two complementary logic outputs. Channels may be paralleled to provide up to 16 inputs and 24 outputs by means of a front-panel switch. An efficient circuit design holds the power dissipation of the entire module to within the NIM standard.

The Model 429A eliminates the extra cabling and time delay involved when conventional fan-ins and fan-outs must be cascaded. In addition, it eliminates the common use of expensive logic units to perform logical OR-ing with adequate fan-out. The ability to conveniently parallel channels permits the 429A a degree of flexibility and efficiency heretofore unavailable.

Inputs are 50 Ω impedance for NIM or TTL signals. Unused inputs need not be terminated. Inputs may be driven with single or double amplitude NIM signals or TTL signals without affecting output amplitude. The three pairs of bridged outputs are direct-coupled current sources which deliver −32 mA into two 50 Ω loads. Output duration is equal to the logical sum of the input durations.

The circuitry of the Model 429A is complete direct-coupled and compatible with either normal or complementary logic signals in any duty ratio. Channel paralleling is accomplished by means of a single front-panel locking switch that is not in the signal path and hence permits switching with minimal effect on signal fidelity. Front-panel lamps located between channels light to indicate channels that are combined, providing a clear, easily-interpreted display of the unit's status.

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, NEW YORK 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPONE: (914) 425-2000

technical information manual

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

FUNCTIONAL DESCRIPTION

General:

Each channel of the four-channel Model 429 Logic Fan-In/Fan-Out can be divided into two basic sections, the 4-fold Fan-In and the four normal-two complement Fan-Out. Also, there is a cross-coupling network to allow merging of channels. These sections are shown on the block diagram and are easily identified on the schematic at the end of this manual.

The following is a general description of these sections.

Four-Fold Fan-In:

Each Fan-In is composed of a 25 mA differential stage, having four parallel transistors with independent input bases in place of the normal single "off" transistor. Any time that one or more of the inputs (transistor bases) are brought below the reference level, the normally "on" transistor base will switch the 25 mA of emitter current to the common collector, driving the terminated 90 Ω strip line with a 1.1 Volt pulse. This signal is then buffered by an emitter follower. In addition to driving its own output stage, the follower allows emitter-Oring of adjacent Fan-In stages, and is therefore able to drive adjacent output stages.

Fan-Out:

Each Fan-Out stage is composed of an emitter follower driving a terminated 90 Ω strip line which in turn drives two differential stages. Each differential stage provides 32 mA of output current during the pulse which can be used to drive two 50 Ω loads per stage. The output of one of the complementary transistors (normally "on") is also brought to the front panel and can drive two 50 Ω loads. All outputs are coupled to ground with three Schottky diodes to voltage-clamp the outputs at approximately -1.5 Volts if no output terminations are used.

Cross-Coupling Section:

Four FET switches are used to couple the channels into two groups of two or one group of four. A front panel switch is used to turn the proper FET's on or off, (along with associated front panel LED's), by connecting the appropriate FET's and LED's (through resistors) from the -12 Volt level they are at in the individual channel (4x4) mode to +12 Volts for cross connecting of channels. When cross connected, the output emitter followers of the input stage are emitter-ORed, so any one can drive the common "cross bus", and the input emitter followers of the output stages provide high impedance pickoffs for each of the output stages tied to the common "cross bus".

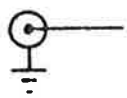
STANDARD DRAFTING SYMBOLS, ELECTRONIC

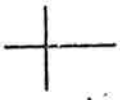

Connection to any given voltage.

Line ending at the edge of the sheet indicates continuance on another sheet.


Male pin or card edge contact.

Female pin, socket or card edge connector.

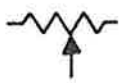

Coaxial connector.


No connection.


Connection.


Resistor, 1/4 W, ±5%, value in ohms (unless specified otherwise).

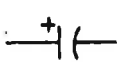
Resistor, 1/4W, ±1%, value in ohms (unless specified otherwise).

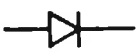

Resistor, variable, any type.

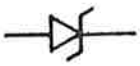

Resistor, variable, any type.

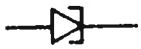
Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).


Capacitor, variable. Values in Picofarads (unless specified otherwise).


Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).

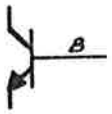

Diode, signal or rectifier.


Diode, zener.

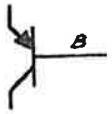

Diode, tunnel.


Diode, snap.

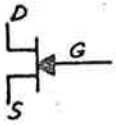

Light emitting diode (LED).



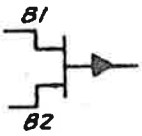
NPN Transistor.



PNP Transistor.



Field effect transistor, P Channel.



Field effect transistor, N.


Air choke.


Ferrite bead.


Ferrite core choke, Z 500 ohms when f > 60 MHz (unless otherwise indicated).


Ferrite core choke, 40 uH, (unless otherwise indicated).

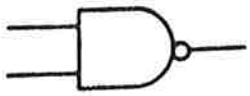
ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL).

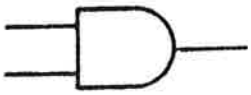
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

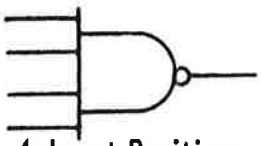
Supply voltages of IC's are shown in a table on each schematic.



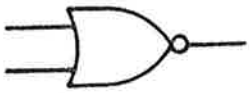
2-Input Positive NAND Gate



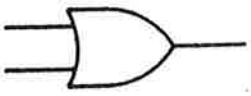
2-Input Positive AND Gate



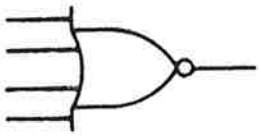
4-Input Positive NAND Gate



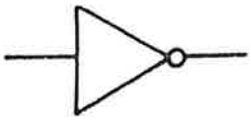
2- Input Positive NOR Gate



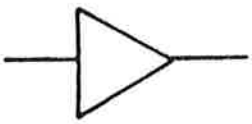
2 -Input Positive OR Gate



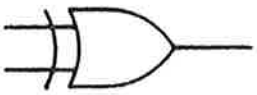
4-Input Positive NOR Gate



Inverter or Inverting Buffer

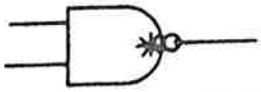


Non-Inverting Buffer

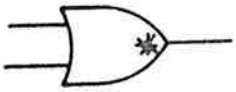


Exclusive OR Gate

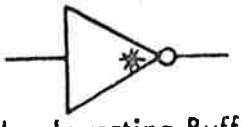
Open collector outputs are identified by an asterisk (*) on the output connection.



2-Input Positive NAND Gate W/Open Collector



2-Input Positive OR Gate W/Open Collector



Non Inverting Buffer W/Open Collector

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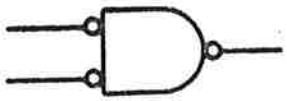
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS EMITTER - COUPLED LOGIC (ECL)

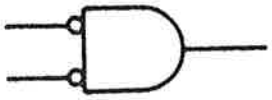
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

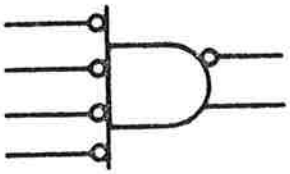
Supply voltages of IC's are shown in a table on each schematic.



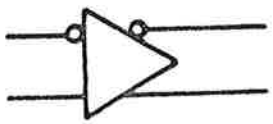
2 - Input Gate.
Negative AND (Positive OR) Gate.



2 - Input Gate.
Negative NAND (Positive NOR) Gate.

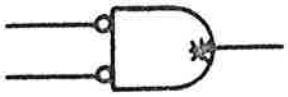


4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.

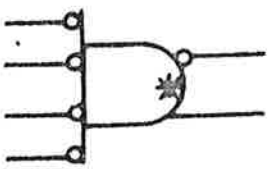


Differential
Amplifier.

Open emitter outputs are identified by an asterisk (*) on the output connection.



2 - Input Negative NAND Gate.
With Open Emitter.



A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.

ENGINEERING DEPARTMENT
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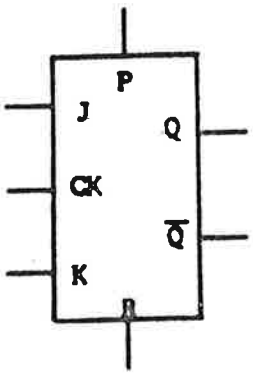
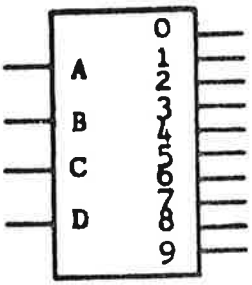
Spring Valley, New York

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL) OR EMITTER COUPLED LOGIC (ECL).

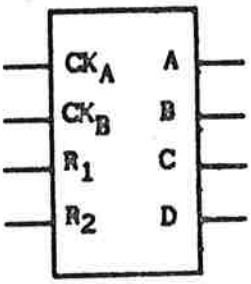
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave Flip-Flop

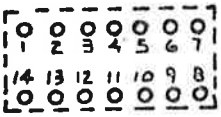


BCD-To-Decimal Decoder-Driver



Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.



Bottom View

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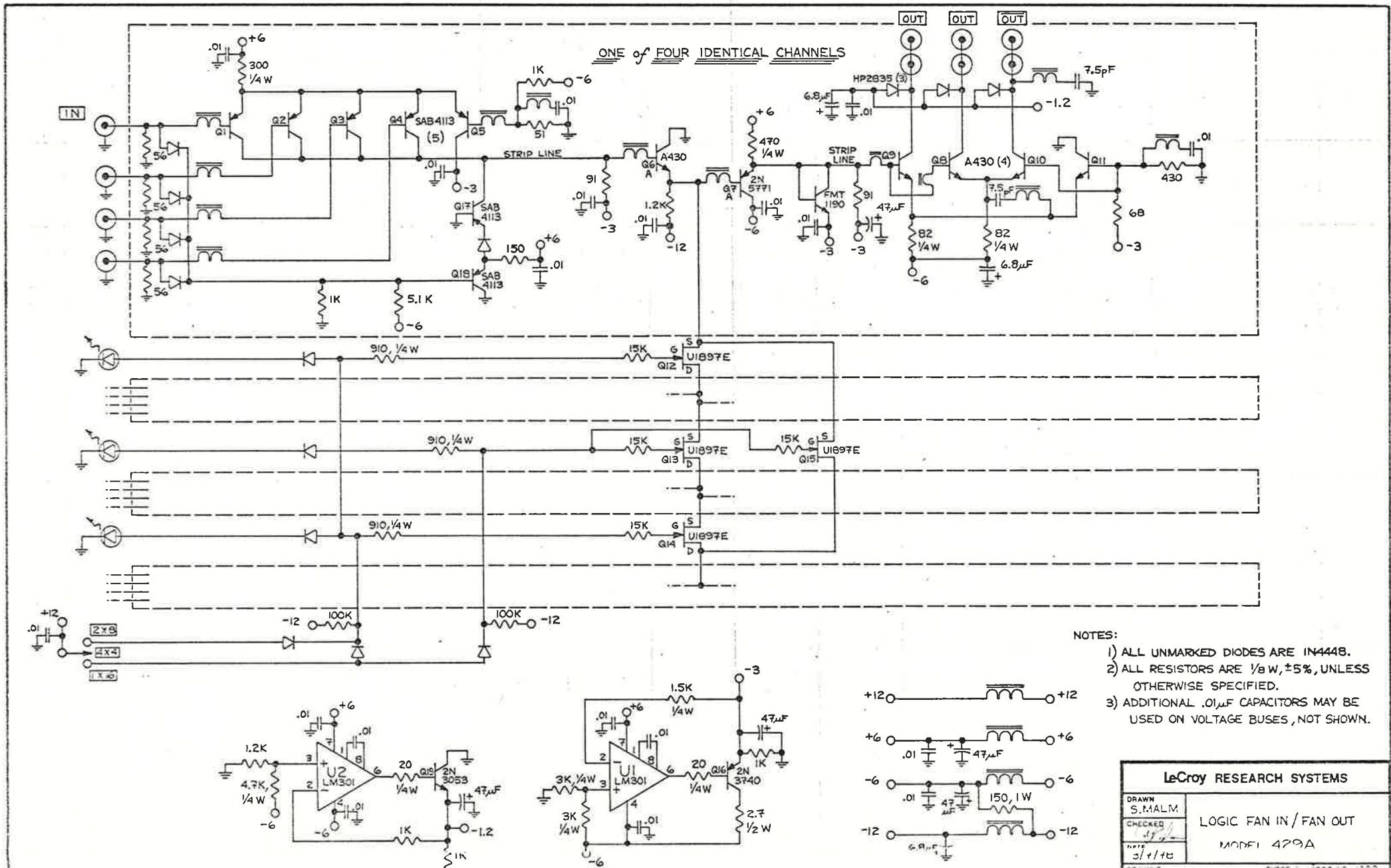
ONE of FOUR IDENTICAL CHANNELS
IN
OUT
OUT
OUT
STRIP LINE
STRIP LINE
HP2835 (3)
A430
A430 (4)
SAB4113
(5)
2N 5771
FMT 1190
U1897E
Q12
Q13
Q14
Q15
Q16
Q17
Q18
U1
U2
LM301
2N 3053
2N 3740
SAB 4113
910, 1/4 W
15K
100K
1K
5.1 K
1.2K
4.7K, 1/4 W
3K, 1/4W
1.5K
1/4 W
1/2 W
2.7
150, 1 W
47μF
6.8μF
7.5pF
2X8
2X4
1X8
NOTES:
1) ALL UNMARKED DIODES ARE IN4448.
2) ALL RESISTORS ARE 1/8 W, ±5%, UNLESS OTHERWISE SPECIFIED.
3) ADDITIONAL .01μF CAPACITORS MAY BE USED ON VOLTAGE BUSES, NOT SHOWN.
LeCroy RESEARCH SYSTEMS
DRAWN S.MALM
CHECKED
DATE 3/1/78
LOGIC FAN IN / FAN OUT
MODEL 429A

ECO NO.	DATE	DESCRIPTION
1000	4-12-78	FINALIZED DOCUMENTATION.

REMARKS

LeCROY RESEARCH SYSTEMS CORPORATION

DRAWN	ENGINEERING CHANGE ORDERS
CHECKED	MODEL 429A
DATE	

DRAWING No.