technical information manual

NIM Models 380 & 380A
Multiplicity Logic Units

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique,reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refine and improve the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Spring Valley, NY, telephone 914-425-2000, or from your local distributor in countries other than the U.S.A.

LeCROY RESEARCH SYSTEMS

See pocket in back of manual for schematics, parts lists, and additional addenda with any changes to manual.

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

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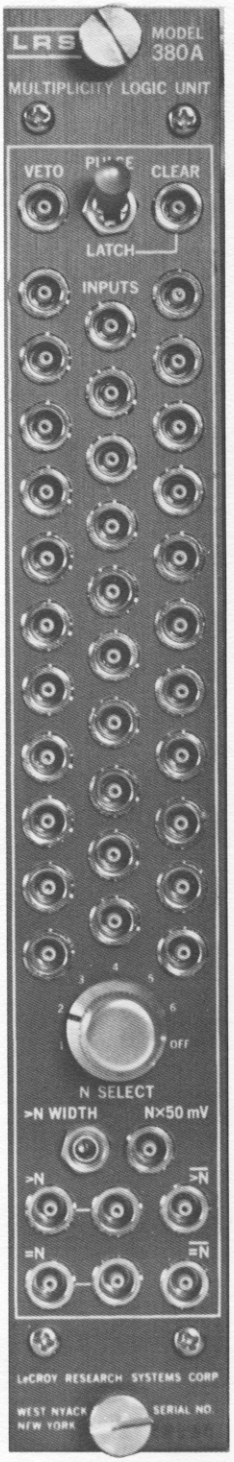
ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

TECHNICAL DATA

LeCroy
RESEARCH SYSTEMS



NIM Model 380A

Multiplicity Logic Unit

The LRS Model 380A Multiplicity Logic Unit for the first time allows easy generation of higher order multiplicity decisions from a large number of counter or chamber logic signals. The unit produces an output whenever N (or > N) out of M input pulses are present, where N is switch-selectable from 1 to 6, and M is any number up to 32. Two sets of outputs are provided, one set for the = N condition and one set for the > N condition. An additional analog summing output is provided giving an amplitude of −50 mV into 50 Ω for each coincident input pulse and a duration equal to the overlap time of the coincident input signals. Since the unit can operate in an ungated mode, and does not require a master strobe signal, it is very useful in trigger pulse generation systems. In systems where a master trigger already exists (e.g., with wire chambers), the Model 380A may be operated in a strobed mode with either pulse or latched outputs. Input speed is compatible with normal 100 MHz logic and maximum output rate is determined by output width.

In the pulse mode, the duration of the = N outputs is preset to 20 ns, but is internally adjustable up to 50 ns. The duration of the > N outputs is front-panel adjustable from 25-100 ns and must be set equal to the maximum possible overlap time of the logic inputs. The > N outputs are generated approximately 12 ns after the > N condition is satisfied. The = N outputs appear somewhat later, approximately 8 ns after the end of the = N input condition, because of the logical necessity of waiting to insure no > N condition occurs.

A clear input is provided to reset the unit in the latched mode. For strobed operation, the veto is driven by a complementary logic signal which goes to zero volts during the strobe interval.

December 1975

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, NEW YORK 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
NIM Model 380A
MULTIPLICITY LOGIC UNIT

INPUT CHARACTERISTICS

Logic Inputs:	32; reflections < 7% for inputs of 2 ns risetime; input range − 650 mV to − 900 mV (NIM level); minimum input width 6 ns.
Veto:	Common to all channels; direct-coupled; − 600 mV or greater inhibits; impedance 50 Ω; reflections < 7% for inputs of 2 ns risetime. Veto must overlap logic inputs.
Slow (Bin) Gate:	Via rear connector, with rear-panel On-Off switch; risetimes and falltimes approximately 20 ns; quiescently above + 4 volts, clamping to ground inhibits; direct-coupled.
Clear:	NIM level; minimum duration 10 ns.

OUTPUT CHARACTERISTICS

> N Outputs:	2 bridged negative outputs (quiescently 0 mA, − 32 mA during output); one complement (quiescently − 16 mA, 0 mA during output); duration variable from 25-100 ns by means of front panel-multiturn potentiometer in pulsed mode, dc level in latched mode. Must be set ⩾ maximum possible overlap time of the logic inputs (since it serves to inhibit the = N outputs when present).
= N Outputs:	2 bridged negative outputs (quiescently 0 mA, −32 mA during output); one complement (quiescently −16 mA, 0 mA during output); duration 20 ns (internally adjustable) in pulse mode, dc level in latched mode.
Risetimes and Falltimes:	3 ns.
Analog Summing Output:	One; amplitude − 50 mV into 50 Ω for each coincident input pulse; duration equal to the overlap time of the coincident input signals; impedance approx. 6 Ω.

GENERAL

Coincidence Level Control:	From 1 to 6 plus "off"; front-panel switch.
Input Double-Pulse Resolution:	< 10 ns.
Output Double-Pulse Resolution:	< 30 ns.
Modes:	Pulse or latched; controls output duration.
Delay:	Input-Output, 12 ns for > N output, 8 ns following end of = N condition for = N output.
Packaging:	In conformance with AEC standard for nuclear modules (AEC Report TID-20893); RF shielded AEC #1 module fitting 12/bin; dimensions 1.375 x 8.75 x 10 inches deep.
Current Requirements:	+ 6 V at 95 mA − 6 V at 400 mA + 24 V at 45 mA

Logic Input Characteristics

Because of the large number of inputs and the high multiplicity level offered by the 380, there are important constraints on input amplitude and width. These are particularly important at the higher N settings, and can be relaxed somewhat if the unit is to be used only for lower multiplicities. These constraints can be summarized by saying that the input signals should be between -650 and 900 mV in amplitude and remain above -650 mV for more than 4 nsec. Under no circumstances should double-amplitude signals be used. Normal standard amplitude outputs from LRS discriminators and logic units satisfy these requirements provided output widths are set sufficiently long (in general, a few nsec larger than absolute minimum).

The specified reflection coefficient applies for standard amplitude NIM inputs. Larger than normal inputs (and in particular, double-amplitude inputs) will be clamped by an input-limiting diode and produce very large reflections which can interfere with subsequent events. Again, input amplitude requirements of the unit should be observed.

Inhibit Input

The inhibit input should arrive no later than coincident with the leading edge of the ≥N condition, and should be at least as long in duration as the largest possible ≥N condition. If all the multiplicity inputs are of the same duration (the most usual case), this means simply that the inhibit input should be coincident and of the same duration. If, however, some of the multiplicity inputs are shorter than others, and these short pulses are required to achieve an =N condition, then the inhibit input need only overlap the short pulses. In all situations, the inhibit pulse must be long enough to cover the time dispersion in the inputs in addition to the above minimums. The inhibit input may also be used as an enable by driving it with a complementary (quiescently negative) logic level.

=N Outputs

These outputs are internally preset to approximately 20 nsec. They may be set to other widths from approximately 7 to 100 nsec by changing internal components, as described in the Functional Description section of this manual. These outputs occur approximately 8 nsec after the end of the =N input overlap condition. The =N outputs cannot be produced more promptly, because they

must be inhibited if a >N condition occurs at any time during the concidence; and this information is not available until the coincidence is over. So =N outputs are produced by triggering from the trailing edge of an ≥N condition during which no >N condition occurs either early or late.

>N Outputs

These outputs must be set at least as large as the maximum possible =N overlap condition (see the Functional Description section of the manual). Otherwise, >N conditions that occur early in a coincidence will fail to inhibit the =N discriminator, resulting in the production of both =N and >N outputs. Whenever this symptom is observed, the first thing to check is the duration of the >N outputs. If increasing this duration eliminates the effect, then either the duration of, or the time dispersion between, the multiplicity inputs must be reduced, or the >N output duration setting must simply be maintained long.

Double-Pulse Resolution

The maximum permissible rate on any multiplicity input is approximately 110 MHz, limited by the bandwidth of the input limiter circuitry, the rather stringent input width requirements imposed by the high multiplicities and input count of the 380, and the DPR of the ≥N LD601 discriminator input stage. The output DPR of the 380 is limited by the =N and <N LD601's. The output DPR for =N outputs is approximately 5 nsec plus the =N output width setting, or nominally 25 nsec. Similarly, the DPR for >N outputs is 5 nsec plus the >N output width setting, or roughly 30 to 100 nsec.

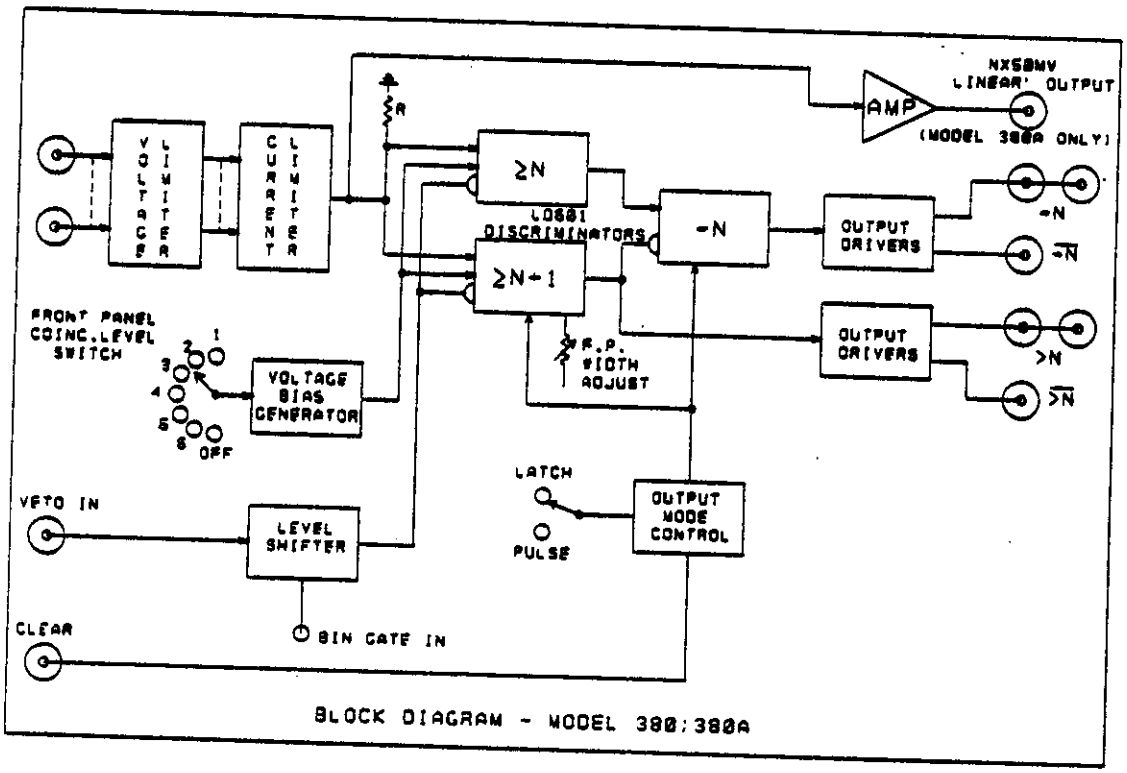
Pulsed and Latched Modes

The Model 380 is normally used with outputs of preset duration as described above. However, it is also compatible with register or "DC logic" systems through inclusion of a latch mode in which outputs remain on a DC basis until they are reset by means of the front panel "Clear" input.

Linear Sum Output (Model 380A only)

In addition to all the features of the Model 380, the Model 380A includes linear output proportional to the number of inputs present. Its output is

low impedance, and the proportionality constant is -50 mV per active input. Risetimes and falltimes are approximately 2 nsec. This output permits external variable threshold discriminators to be used to determine several simultaneous multiplicity levels, or, with care, to extend the maximum multiplicity obtainable above 6.



BLOCK DIAGRAM - MODEL 380/380A

In the following discussions, reference will be made to the Block Diagram above and, occasionally, to the Circuit Diagram. All comments apply to both the 380 and the 380A unless the 380 is specifically excluded.

Logic input signals are first voltage limited at about -700 mV by means of a diode to ground at the input. This limiting is intended to reduce the effects of overshoots or small overloads. It will not take care of double amplitude NIM inputs and such inputs must not be used because of danger of leading edge feedthrough and consequent failure of the coincidence level selection logic, particularly at higher coincidence (N) settings. Also, double amplitude inputs will produce large inverted reflections which will not be absorbed at the source and may cause subsequent valid events to be lost.

After voltage limiting (to about -600 mV) the logic input signals drive precision diode current switches. Each switch delivers -1.00 mA into a 15 Ω summing resistor, resulting in 15 mV developed across this resistor for each active input. This summed voltage is applied to two LD-601 discriminators,

one of which is biased to trigger at (N-½) x 15 mV and the second at (N+½) x 15 mV. The first gives an output for ≥N simultaneous inputs and the second for ≥N + 1 (or equivalently, >N).

The second (>N) discriminator drives directly an output stage which delivers the >N outputs at the front panel. The duration of these outputs is presettable at the front panel by means of a potentiometer which controls the pulse width of the LD601 discriminator.

The first (≥N) discriminator produces a positive-going time-over-threshold output that is applied to the input of a third LD601 discriminator. Because this ≥N output is positive-going, the LD601 that it drives triggers on its trailing (negative-going) edge. This edge occurs, of course, at the end of the ≥N condition of the inputs. If during this time there was no >N condition, so that the >N discriminator did not fire, the =N discriminator triggers, delivering an =N output pulse to the front panel via an output stage. If, however, a >N condition occurred, the resulting output of the >N discriminator holds the =N discriminator inhibited, and there is no =N output. Note that the >N output must be long enough to completely overlap the entire ≥N time in order to assure inhibition of the =N output. In practice, this means that the >N output duration must be set no less than the duration of the longest possible =N overlap time, usually equivalent to the duration of the input pulses. This is the reason for the adjustable output duration for the >N output provided on the Model 380.

The width of the =N outputs is internally set to about 20 nsec. It may be altered by changing the resistor to +6 V and/or capacitor to ground at pin 3 of the =N LD601. The resistor should be kept in the range from 3 to 15 K, and the capacitor from 18 to 100 pf.

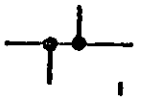
The bias levels for the first two LD601's (≥N and >N) are set by a unity gain op amp whose input is connected to taps on a precision voltage divider by the front panel N-select switch. An internal trimmer pot for each LD601 permits compensation for offset voltages in the op amp and in the 601's themselves. In addition, the trimmer pot for the >N LD601 is used to offset its threshold setting approximately -15 mV from the reference voltage.

In the Latch mode, the width circuits of the >N and =N discriminators are biased off, so that once triggered these discriminators remain locked on until they are reset by application of a pulse to the Clear input.

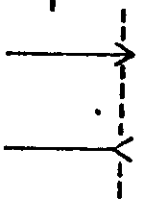
CONNECTION JUMPS TO SPECIFIED PAGE.

LINE ENDING AT THE EDGE OF THE SHEET INDICATES CONTINUANCE ON ANOTHER SHEET.

NO CONNECTION

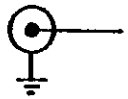


CONNECTION



MALE PIN OR CARD-EDGE CONTACT.

FEMALE PIN, SOCKET, OR CARD-EDGE CONNECTOR.

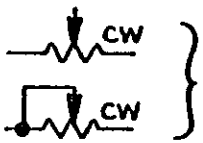


CO-AXIAL CONNECTOR

CONNECTION TO ANY GIVEN VOLTAGE.

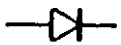
FUSE

RESISTOR, VALUE IN OHMS

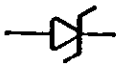


RESISTOR, VARIABLE (ANY TYPE)

RESISTOR, THERMAL (THERMISTOR)



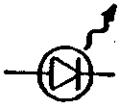
DIODE, SIGNAL OR RECTIFIER



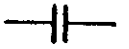
DIODE, ZENER

DIODE, TUNNEL

DIODE, SNAP

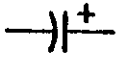


DIODE, LIGHT-EMITTING (LED)



CAPACITOR (CERAMIC, W/VALUE IN μF, UNLESS OTHERWISE SPECIFIED)

CAPACITOR, VARIABLE (VALUE IN pF, UNLESS OTHERWISE SPECIFIED)



CAPACITOR, POLARIZED (VALUE IN μF/VOLTS, UNLESS OTHERWISE SPECIFIED)

AIR CHOKE

FERRITE BEAD, HALF

FERRITE BEAD, FULL

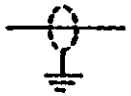
FERRITE CORE CHOKE

LeCroy RESEARCH SYSTEMS	
DRAWN S.MALM CHECKED GALLANT DATE 3/13/79	STANDARD DRAFTING SYMBOLS, ELECTRONIC

GROUND (ALSO USED AS SIGNAL GND.)

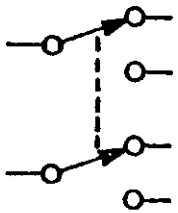
CHASSIS GND.

POWER GND.

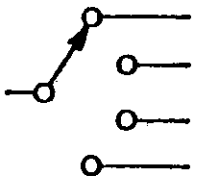


CO-AXIAL CABLE

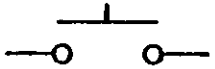
SPST SWITCH



DPDT SWITCH

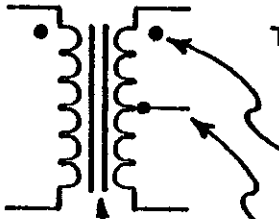


ROTARY SWITCH



NORMALLY OPEN MOMENTARY SWITCH

NORMALLY CLOSED MOMENTARY SWITCH

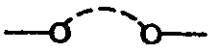


TRANSFORMER

BLACK DOT SHOWS PHASE OF WINDINGS

TAP (CENTER, UNLESS OTHERWISE SPECIFIED)

FERRITE OR IRON CORE



JUMPER

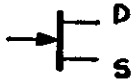
TEST POINT

LeCroy RESEARCH SYSTEMS		
DRAWN S.MALM	STANDARD DRAFTING SYMBOLS, ELECTRONIC	
CHECKED GALLANT		
DATE 3/13/79		
DRAWING NUMBER:	SHEET 2 OF 6	ECO NO DATE

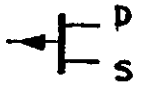
NPN TRANSISTOR

PNP TRANSISTOR

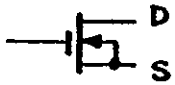
FIELD EFFECT TRANSISTORS (FET)



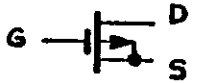
JUNCTION GATE
N CHANNEL
DEPLETION TYPE



JUNCTION GATE
P CHANNEL
DEPLETION TYPE



INSULATED GATE
N CHANNEL
DEPLETION TYPE



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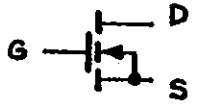
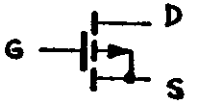


INSULATED GATE
N CHANNEL
ENHANCEMENT TYPE



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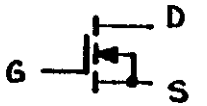
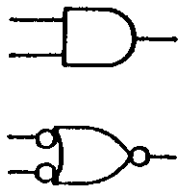
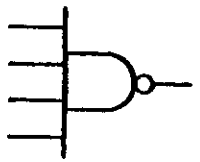
ENHANCEMENT TYPE

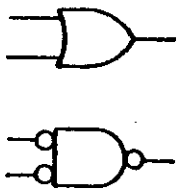


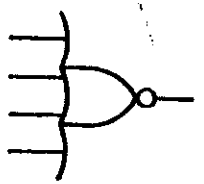
VMOS (INSULATED V GATE)
N CHANNEL
ENHANCEMENT TYPE

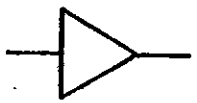
LeCroy RESEARCH SYSTEMS	
DRAWN S.MALM	STANDARD DRAFTING SYMBOLS, ELECTRONIC
CHECKED GALLANT	
DATE 3/13/79	

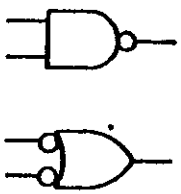


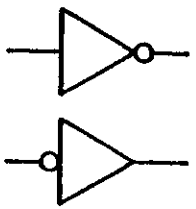


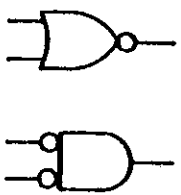




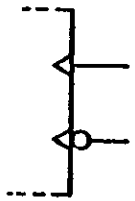






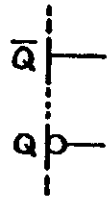


LeCroy RESEARCH SYSTEMS		
DRAWN S. MALM	STANDARD DRAFTING SYMBOLS	
CHECKED GALLANT		
DATE 3/13/79	DIGITAL I.C.s -TTL	
DRAWING NUMBER:	SHEET 4 OF 6	ECO NO DATE



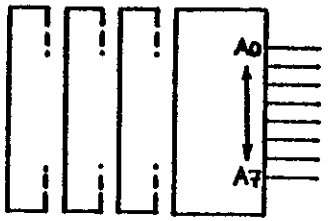
POS. EDGE-TRIGGERED CLK. INPUT

NEG. EDGE-TRIGGERED CLK. INPUT

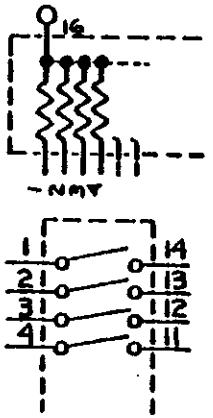


TO INDICATE INVERTED SIGNAL, USE EITHER THE BAR OVER THE SIGNAL NAME, OR THE INVERSION "BUBBLE", BUT NOT BOTH.

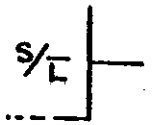
SHOW THE NORMAL (STD.) POSITION OF A JUMPER OPTION AS A SOLID ARC. OTHER POSITIONS ARE SHOWN AS DASHED ARCS.



MEMORY ARRAYS (OR OTHER I.C.s) WITH COMMON CONNECTIONS MAY BE SHOWN IN THIS COMPRESSED FASHION.

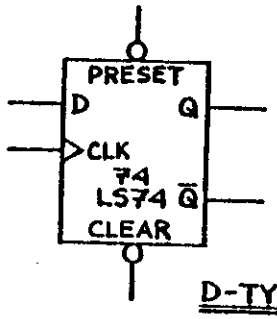


DIP RESISTOR ARRAYS AND SWITCHES ARE SHOWN AS ONE DEVICE.

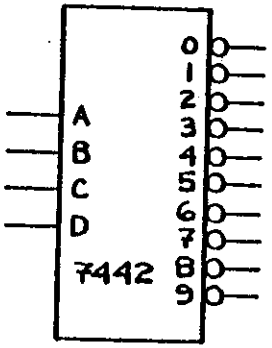


THIS LABEL INDICATES THAT A HIGH STATE ENABLES THE SHIFT MODE, AND A LOW STATE ENABLES THE LOAD MODE.

LeCroy RESEARCH SYSTEMS	
DRAWN S.MALM	STANDARD DRAFTING SYMBOLS, ELECTRONIC
CHECKED GALLANT	
DATE 3/13/79	

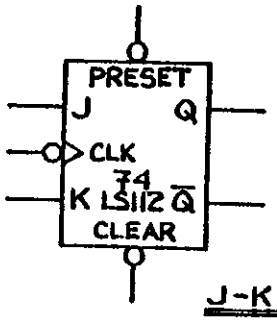


D-TYPE FLIP-FLOP

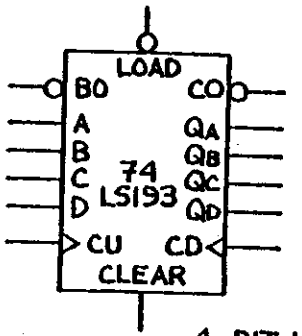


BCD TO DECIMAL DECODER

POSITIVE LOGIC CONVENTION IS OBSERVED.
THE HIGH STATE (LOGICAL "1") IS MORE POSITIVE THAN THE LOW STATE

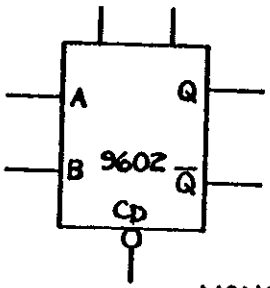


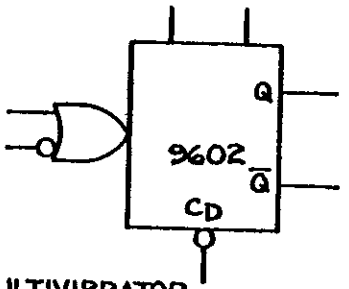
J-K FLIP-FLOP



4-BIT UP/DOWN COUNTER

THESE ARE EXAMPLES OF COMMONLY USED SYMBOLS FOR TTL DEVICES.





MONOSTABLE MULTIVIBRATOR

LeCroy RESEARCH SYSTEMS		
DRAWN S.MALM	STANDARD DRAFTING SYMBOLS, DIGITAL I.C.s -TTL	
CHECKED GALLANT		
DATE 3/13/79		
DRAWING NUMBER:	SHEET 6 OF 6	ECO NO DATE

MODEL NO 380A MULTIPL LOGIC UNIT PRINTED 04-Nov-80
LAST REVISION NO 1005 REVISION DATE 24-Jun-80

101	246	**2	PC STOCK DBL SIDED	1 OZ			59M
102	245	103	CAP CERA DISC 25V	.01 UF	20% Y5F		22
102	444	560	CAP CERA DISC 100V	56 PF	10% S3N		1
102	944	*75	CAP CERA DISC 1KV	7.5 PF	10% S2L		2
103	327	103	CAP CERA MONO 50V	.01 UF	20% GENERAL PURPOSE		1
105	228	103	CAP MUCON RIBB LD	.01 UF	SUPER-K CERA 25V 30%		4
116	515	101	CAP DIP MICA DM10	100 PF			1
116	515	270	CAP DIP MICA DM10	27 PF			1
142	124	476	CAP TANT DIP CASE	47 UF	6.3 VOLT 20 %		5
142	824	685	CAP TANT DIP CASE	6.8 UF	35V 20%		11
158	819	**1	CAP VARI CERA	3.2-18 PF			1
161	335	*27	RES COMP 1/4W 5%	2.7 OHMS			1
161	335	101	RES COMP 1/4W 5%	100 OHMS			8
161	335	102	RES COMP 1/4W 5%	1 K			3
161	335	105	RES COMP 1/4W 5%	1 MEG			1
161	335	111	RES COMP 1/4W 5%	110 OHMS			2
161	335	122	RES COMP 1/4W 5%	1.2 K			1
161	335	152	RES COMP 1/4W 5%	1.5 K			1
161	335	153	RES COMP 1/4W 5%	15 K			1
161	335	162	RES COMP 1/4W 5%	1.6 K			1
161	335	182	RES COMP 1/4W 5%	1.8 K			1
161	335	200	RES COMP 1/4W 5%	20 OHMS			4
161	335	202	RES COMP 1/4W 5%	2 K			1
161	335	240	RES COMP 1/4W 5%	24 OHMS			2
161	335	241	RES COMP 1/4W 5%	240 OHMS			1
161	335	301	RES COMP 1/4W 5%	300 OHMS			3
161	335	302	RES COMP 1/4W 5%	3 K			1
161	335	331	RES COMP 1/4W 5%	330 OHMS			1
161	335	332	RES COMP 1/4W 5%	3.3 K			2
161	335	391	RES COMP 1/4W 5%	390 OHMS			1
161	335	471	RES COMP 1/4W 5%	470 OHMS			2
161	335	510	RES COMP 1/4W 5%	51 OHMS			6
161	335	560	RES COMP 1/4W 5%	56 OHMS			33
161	335	562	RES COMP 1/4W 5%	5.6 K			1
161	335	621	RES COMP 1/4W 5%	620 OHMS			1
161	335	821	RES COMP 1/4W 5%	820 OHMS			1
161	335	822	RES COMP 1/4W 5%	8.2 K			1
168	531	201	RES PREC RN55D	10.0 OHMS			6
168	531	209	RES PREC RN55D	12.1 OHMS			1
168	531	247	RES PREC RN55D	30.1 OHMS			2
168	531	326	RES PREC RN55D	200 OHMS			1
168	531	338	RES PREC RN55D	267 OHMS			1
168	531	403	RES PREC RN55D	1.27 K			1
168	531	460	RES PREC RN55D	4.99 K			2
168	531	477	RES PREC RN55D	7.50 K			1
168	531	481	RES PREC RN55D	8.25 K			1
168	531	518	RES PREC RN55D	20.0 K			32
168	531	535	RES PREC RN55D	30.1 K			1
168	531	554	RES PREC RN55D	47.5 K			1
181	447	103	RES VARI CERMET	10 K	1/2W 10% 3/8"SQ .150 WIDE TOP ADJUST		2
181	457	103	RES VARI CERMET	10 K	1/2W 10%		2
181	457	501	RES VARI CERMET	500 OHMS	1/2W 10%		1
182	527	103	RES VARI CERMET	10 K	3/4W 10%		1
208	*11	**1	IC SINGLE OP AMP	UA741C	DIP-8		1

MODEL NO 380A MULTIPL LOGIC UNIT PRINTED 04-Nov-80
LAST REVISION NO 1005 REVISION DATE 24-Jun-80

208	*11	**3	IC SINGLE OP AMP	LM301AN	DIP-8	3
208	*74	**2	IC DIFF AMPL	CA3049	DUAL PKG/12-LEAD "TO" CAN	1
210	*40	**2	IC AMPLITUDE DISCR	LD601C	DIP-16	3
230	110	**3	DIODE SWITCHING	FD 777		32
230	110	**5	DIODE SWITCHING	1N4448		6
235	*10	**5	DIODE RECTIFIER	1N4005		1
240	225	703	DIODE ZENER 3.45V	1N703A	250MW	3
240	225	705	DIODE ZENER 4.85V	1N705A	250MW	1
253	*10	835	DIODE HOT CARRIER	HP2835	H-P CASE 15	74
270	130	401	TRANSISTOR NPN	A401	TO-72	5
270	150	**1	TRANSISTOR NPN	2N3053	TO-5	2
275	150	**3	TRANSISTOR PNP	40319	TO-5	1
275	170	**2	TRANSISTOR PNP	2N5771	TO-92 SEE 275-170-004(MPS3640)	5
300	*10	**1	BEAD SHIELDING	FERRITE		41
300	*50	**1	CHOKE FERRITE SINGLE LEAD			4
400	*10	**8	SOCKET IC ST	DIP-8	BONDED TIN CONTACTS/COPP-NICKEL PINS	4
400	*30	*16	SOCKET IC ST	DIP-16	BONDED TIN CONTACTS/COPP-NICKEL PINS	3
402	*30	**0	CONNECTOR CO-AXIAL	LEMO		41
402	*30	**2	SPANNER NUT SMALL OD	LEMO		41
402	*30	**3	GROUND LUG NONLOCK	LEMO		A/R
402	*30	**4	GROUND STRAP "H"	LEMO		A/R
405	112	**1	CONNECTOR BLOCK	(PIN)	42 "MIXED"	1
405	212	**2	GUIDE PIN	(MALE)	CADMIUM PLATED BRASS	1
405	213	**1	GUIDE PIN	(MALE)	BRASS	1
405	312	**1	GUIDE PIN	(FEMALE)	CADMIUM PLATED BRASS	2
405	410	*16	CONNECTOR PIN	(MALE)		A/R
405	613	**1	CONNECTOR HOOD		CADMIUM PLATED STEEL/INT CLOSED END	1
410	112	102	SWITCH TOGGLE	SPDT	ON-NONE-ON/2 POS LOCKING	1
412	111	**1	SWITCH ROTARY	1P7T	36 DEGR	1
500	120	**2	TRANSIPAD	"LARGE"		3
536	111	**1	KNOB, SKIRTED W/POINTER		ALU KNURLED FOR 1/8-INCH SHAFT	1
540	102	**1	FRONT PANEL	NIM SIZE #1		1M
540	103	102	SIDE COVER	NIM LEFT		1
540	103	103	SIDE COVER	NIM RIGHT		1
540	104	101	WRAPAROUND	NIM SIZE #1	WITH BIN GATE	1M
540	105	**1	BRACKET NIM WRAP	SIZE #1		2
555	611	**1	CAPTIVE SCREW	6-32		2
555	621	**2	CAPTIVE SCREW RETAINER		STAINLESS STEEL (FORMERLY PLATED BRA	2
555	632	**1	SET SCREW HEX	6-32X3/16	USED W 536 111 001/STAINL/CUP POINT	1
567	256	**4	SCREW FLAT PHIL	2-56X1/4		4
585	141	237	RIVET "POP" ALU	1/8X.237	BUTTONHEAD 1/8 DIA .237 LONG	2
710	380	*13	PC BD PREASS'Y	380A		1
710	380	*23	PC BD PREASS'Y	380A-1		1
720	380	*13	FRONT PNL PREASS'Y	380A	540102001(1)555621002(2)	1
740	**0	**2	WRAPAROUND NIM 1 BIN GATE		540104101(1)	1

NOTES 1 USES TWO PC BOARDS
NOTES 2
NOTES 3
NOTES 4
NOTES 5
NOTES 6
NOTES 7
NOTES 8
NOTES 9
NOTES 10
NOTES 11
NOTES 12
NOTES 13

ECO NO.	DATE	DESCRIPTION
975	11-19-75	PARTS LIST CHANGES ONLY
008	2-22-75	PARTS LIST ONLY: ALL 430 TRANSISTORS CH. TO A401.
018	1-5-76	PARTS LIST CORRECTION ONLY
022	1-7-76	PARTS LIST CORRECTION ONLY: .01 ERIE REDCAP ADDED.
091	3-19-76	ALL 10 MBD 101 DIODES CHANGED TO HP2835/ PARTS LIST ONLY: HARDWARE CORRECTION.
233	9-15-76	LD601D CHANGED TO LD601C.
325	2-16-77	CORRECTED ASSEMBLY DRAWING.
396	5-18-77	CORRECTED ASSEMBLY DRAWING AND PARTS LIST
399	5-20-77	CHANGED 33 pF TO 50 pF ON SMALL BOARD/ REMOVED WIRE WITH 3 BEADS AND REPLACED WITH 50 OHM RESISTORS AT IC'S A&B PIN 11/ ADDED 7.5 pF CAP TO TOP SIDE OF BOARD NEAR IC's A&B PIN 11 TO GROUND AS SHOWN ON CHART SHORTEST POSSIBLE LEADS/ REPLACED WIRE WITH 3 BEADS WITH SHORT BUS WIRE ON SMALL WIRE.
449	8-26-77	ADDED 6.8 uF CAP TO ASSEMBLY DRAWING ONLY.
503	10-18-77	ASSEMBLY CORRECTION ONLY.
563	1-9-78	CORRECTED PARTS LIST ONLY.
1001	2-2-78	CHANGED 1N4001 DIODE TO 1N4005.
1002	5-5-78	REPLACED 43.2K ±1% RESISTOR(IN SEREIS WITH THE 10K POT FROM PIN3 IC TO PIN 2 IC E (SHEET 1 OF SCH. AFFECTED).
1003	8-9-78	PARTS LIST UPDATED ONLY.
1004	6-1-79	PARTS LIST CORRECTED ONLY. (PRIORITY 4)
1005	6-24=80	REPLACED ALUMINUM SET SCREW WITH STEEL ONE PART #555-632-001

REMARKS

Remarks: On Priorities
1-Recall, field retrofit
2-Rework shippable units
3-Rework units in fabrication, assembly or test
4-Improvements for future MO's

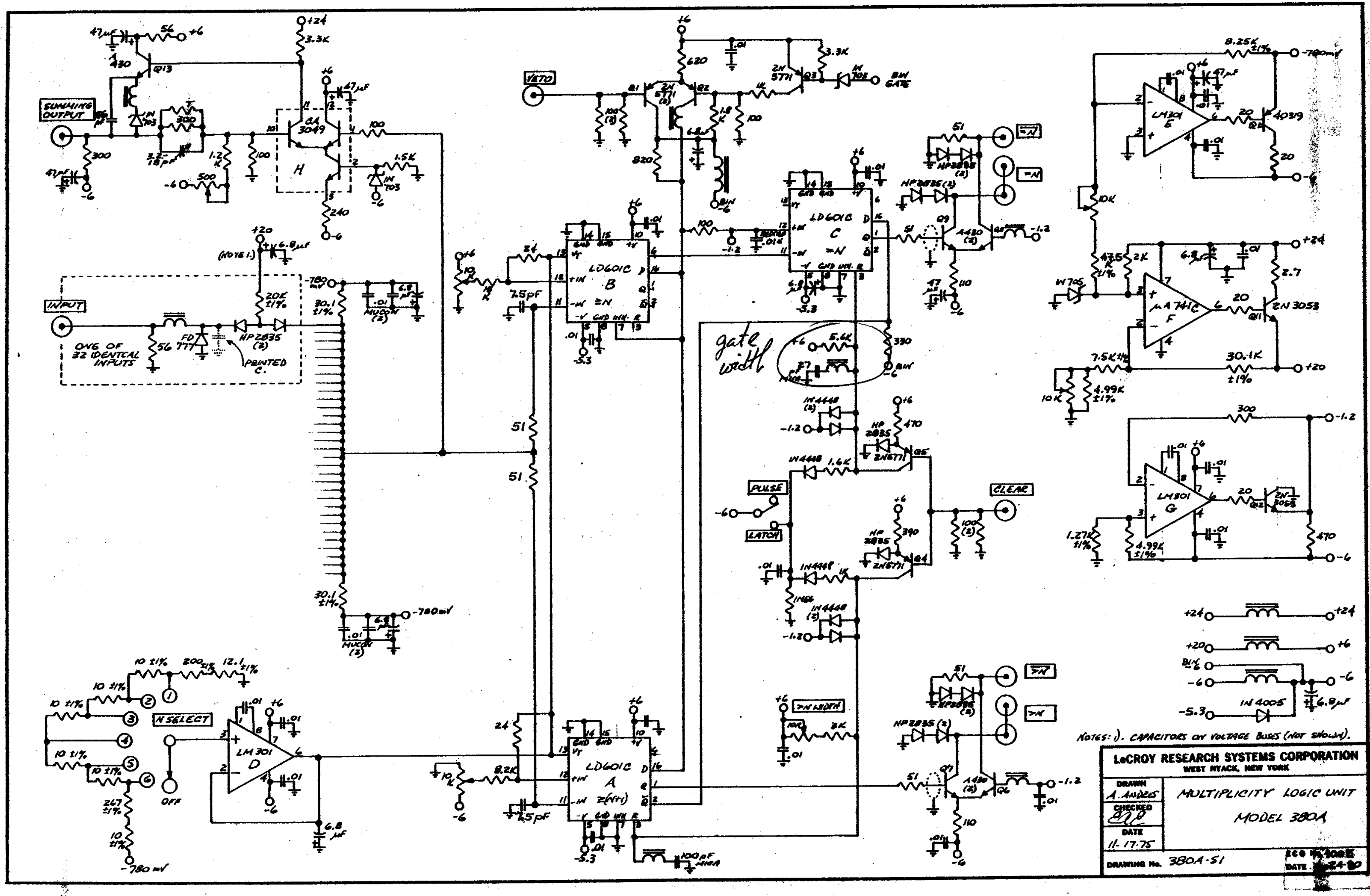
LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN
CHECKED
DATE

ENGINEERING CHANGE ORDERS

MODEL 380A

DRAWING No.


SUMMING OUTPUT
INPUT
ONE OF 32 IDENTICAL INPUTS
PRINTED C.
(NOTE 1.)
VETO
BIN GATE
LD601C B
LD601C C
LD601C A
LM301 E
µA741C F
LM301 G
LM301 D
N SELECT
OFF
PULSE
LATCH
CLEAR
>N WIDTH
=N
≥N
>N
gate width
NOTES: 1). CAPACITORS ON VOLTAGE BUSES (NOT SHOWN).
LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK
DRAWN A. ANDRES
CHECKED
DATE 11-17-75
MULTIPLICITY LOGIC UNIT
MODEL 380A
DRAWING No. 380A-51