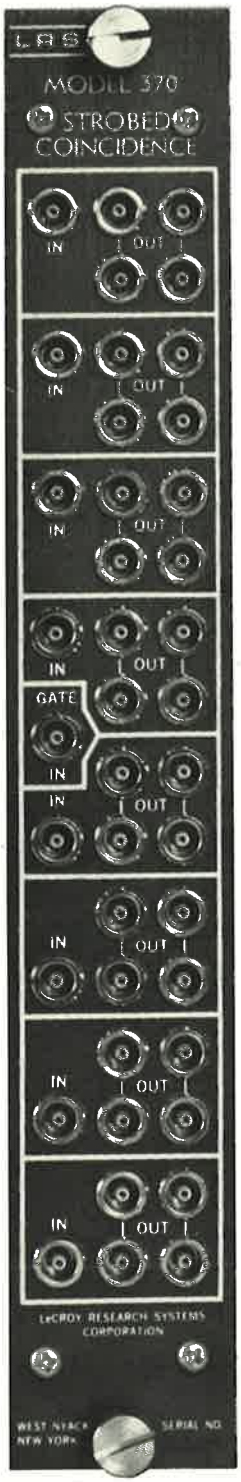
TECHNICAL DATA

LeCroy
RESEARCH SYSTEMS



NIM Model 370C
8-Channel Strobed Coincidence

- **8 channels in single-width module**
- **Four logic outputs per channel**
- **Direct-coupled**
- **Output duration equal to input overlap**
- **Double-pulse resolution < 8 nsec**
- **Stage delay 3 nsec**
- **Within NIM power dissipation requirements**

The LeCroy Model 370C 8-Channel Strobed Coincidence accepts standard NIM logic signals at the eight independent logic inputs and the common gate input. Channel inputs which are simultaneous with the common gate signal satisfy the two-fold coincidence condition and generate four NIM level fast logic outputs of duration equal to the overlap time of the coincident signals, and of risetimes and falltimes less than 2.5 nsec. A full amplitude output will be produced by gate and signal overlap of < 1.8 nsec. Since internal delay through the gate circuit is approximately 1 nsec longer than through the logic input circuit, the gate signal should precede the logic input by 1 nsec to permit accurate coincidence determination of input signals.

The Model 370C is a compact, state-of-the-art design employing MECL III integrated circuits to provide coincidence resolving times under 1.8 nsec and a maximum rate greater than 125 MHz. The basic simplicity of the Model 370C can be verified by its parts count, manifest in its 3.2 nsec input-output delay. Such simplicity of circuit design, coupled with full pretesting and burn-in of all active components, creates a highly stable and reliable instrument coincident with the demanding requirements of today's larger experiments.

Packaged in a #1 NIM module, the Model 370C provides 8 coincidence channels without exceeding power limits imposed by the NIM standard. Its compactness permits more flexible use of available experimental areas and eliminates the waste of bin space caused by front panel limitations typical of the past.

January 1976

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, NEW YORK 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
NIM Model 370C
8-CHANNEL STROBED COINCIDENCE

INPUT CHARACTERISTICS

Logic Inputs: Eight; one for each of eight independent channels; impedance 50 Ω; protected to ± 5 volts; -600 mV minimum amplitude; reflections < 7% for inputs of 2 nsec risetime.

Gate: Common to all eight channels; direct-coupled; -600 mV or greater enables (standard AEC fast logic level); impedance 50 Ω; protected to ± 5 volts; reflections < 7% for inputs of 2 nsec risetime. Gate input should precede logic inputs by 1 nsec to compensate for internal delay.

Slow (Bin) Gate: Via rear connector, with rear-panel On-Off switch; risetimes and falltimes approximately 20 nsec; quiescently above + 4 volts, clamping to ground inhibits; direct-coupled.

Signal Duration: Approximately 2 nsec minimum; no maximum.

OUTPUT CHARACTERISTICS

Fast Logic Outputs: 4 negative per channel; quiescently 0 mA, -16 mA during output; duration equal to overlap between input logic signal and fast gate.

Risetimes and Falltimes: < 2.5 nsec, -100 mV to -700 mV. At least one output of the adjacent output pair must be terminated to provide optimum pulse shape.

GENERAL

Double-Pulse Resolution: < 8 nsec.

Delay: Input-Output, 3.2 nsec.

Coincidence Overlap: Minimum overlap of 1.8 nsec produces full amplitude output.

Packaging: In conformance with AEC standard for nuclear modules (AEC Report TID-20893); RF shielded AEC #1 module fitting 12/bin; dimensions 1.375 × 8.75 × 10 inches deep.

Power Requirements: -6 V at 260 mA; -12 V at 3 mA; + 12 V at 10 mA.

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique,reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refine and improve the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Spring Valley, NY, telephone 914-425-2000, or from your local distributor in countries other than the U.S.A.

LeCROY RESEARCH SYSTEMS

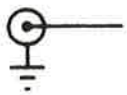
STANDARD DRAFTING SYMBOLS, ELECTRONIC


Connection to any given voltage.

Line ending at the edge of the sheet indicates continuance on another sheet.

Male pin or card edge contact.


Female pin, socket or card edge connector.

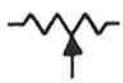

Coaxial connector.


No connection.

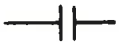

Connection.


Resistor, 1/4 W, ±5%, value in ohms (unless specified otherwise).

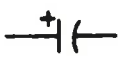

Resistor, 1/4W, ±1%, value in ohms (unless specified otherwise).


Resistor, variable, any type.


Resistor, variable, any type.


Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).


Capacitor, variable. Values in Picofarads (unless specified otherwise).


Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).

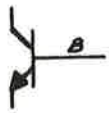

Diode, signal or rectifier.


Diode, zener.

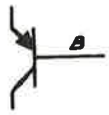

Diode, tunnel.


Diode, snap.

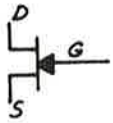

Light emitting diode (LED).



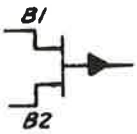
NPN Transistor.



PNP Transistor.



Field effect transistor, P Channel.



Field effect transistor, N.


Air choke.


Ferrite bead.


Ferrite core choke, Z 500 ohms when f ≥ 60 MHz (unless otherwise indicated).

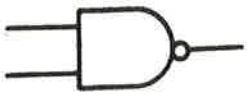

Ferrite core choke, 40 uH, (unless otherwise indicated).

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL).

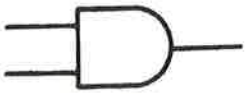
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

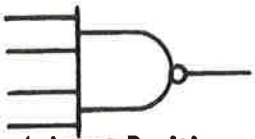
Supply voltages of IC's are shown in a table on each schematic.



2-Input Positive NAND Gate



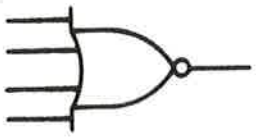
2-Input Positive AND Gate



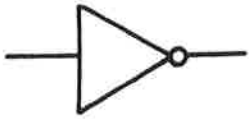
4-Input Positive NAND Gate

2- Input Positive NOR Gate

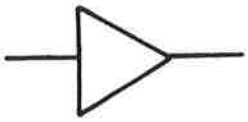
2-Input Positive OR Gate



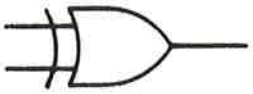
4-Input Positive NOR Gate



Inverter or Inverting Buffer



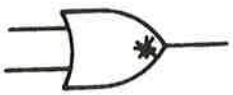
Non-Inverting Buffer



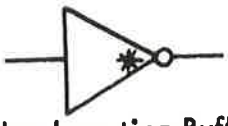
Exclusive OR Gate

Open collector outputs are identified by an asterisk (*) on the output connection.

2-Input Positive NAND Gate W/Open Collector



2-Input Positive OR Gate W/Open Collector



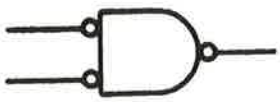
Non Inverting Buffer W/Open Collector

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS
EMITTER - COUPLED LOGIC (ECL)

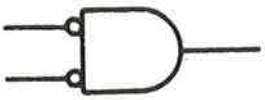
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

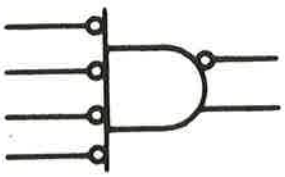
Supply voltages of IC's are shown in a table on each schematic.



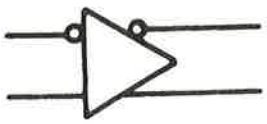
2 - Input Gate.
Negative AND (Positive OR) Gate.



2 - Input Gate.
Negative NAND (Positive NOR) Gate.

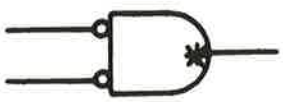


4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.

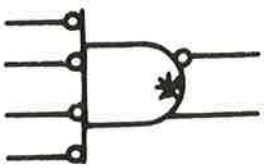


Differential
Amplifier.

Open emitter outputs are identified by an asterisk (*) on the output connection.



2 - Input Negative NAND Gate.
With Open Emitter.

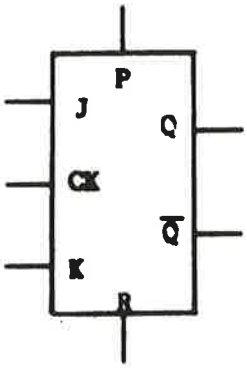


A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.

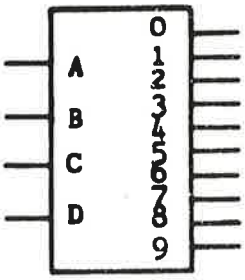
ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL) OR EMITTER COUPLED LOGIC (ECL).

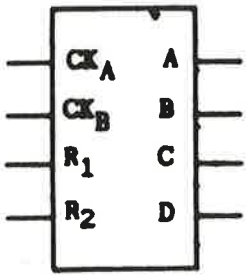
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave Flip-Flop

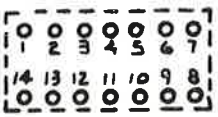


BCD-To-Decimal Decoder-Driver



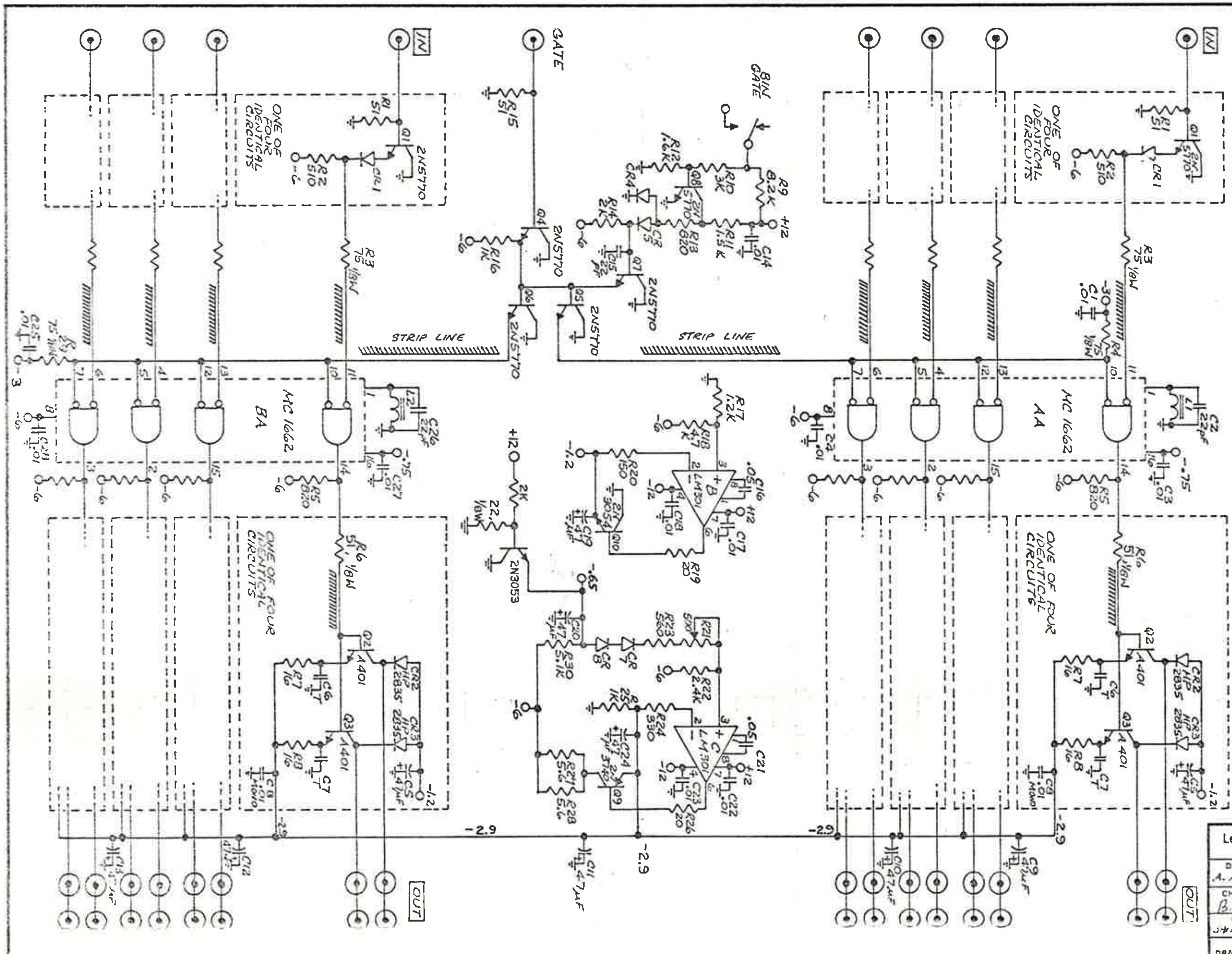
Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.



Bottom View

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York



21 NOV. 1978

+12 C33 6.8 µF L3
-6 C34 90µF L4
-12 C35 6.8 µF L5

NOTES:

1). ALL UNIDENTIFIED DIODES ARE 1N4448.
2). COMPONENTS MARKED "T" ARE TO BE CHOSEN AT TEST.
3). ADDITIONAL .01 µF OR 6.8µF CAPACITORS NOT SHOWN, MAY BE USED ALONG VOLTAGE BUSES.
4). Q2 AND Q3 TO BE MATCHED: VBE TO ±5mV @ IC = 34 mA, IC = 2V (VBE MUST BE ≅ 830 mV). ALL SIXTEEN MUST BE MATCHED TOGETHER.
5). HIGHEST REFERENCE DESIGNATIONS USED: R30 C28 CR9 Q10 L5

OMITTED: —

LeCROY RESEARCH SYSTEMS CORPORATION WEST NYACK, NEW YORK	
DRAWN A. ANKES	8-CHANNEL STROBED COINCIDENCE MODEL 370?
CHECKED B.M.Y.	
DATE JAN. 5, '77	
DRAWING No. 370 C-S1	SHEET/ECO No. 544 OF 1 DATE 12/6/77

ECO NO.	DATE	DESCRIPTION
173	5-27-76	ASSEMBLY DRAWING ONLY: A430 TRANSISTORS CHANGED TO A401/ "T" RESISTOR ADDED TO Q2-BASE/ 6.8uF CAP REPLACED WITH 47uF AT EACH EMITTER RESISTOR OF Q3 TO -3V/ ALL BEADS ON OUTPUTS DELETED/ OFF IC "B" Pin 3 (THRU DIODE) 200 OHMS TO GROUND CHANGED TO 2.7 OHMS.
236	9-21-76	SCHEMATIC REDRAWN. FIVE 47uF CAPS ADDED ON -3V LINE. Q9 ISOLATED FROM GROUND. SOME 47uF CAPS CHANGED TO .01 MONO.
304	12-30-76	FOLLOW-UP OF ECO #236: NEW BOARD LAYOUT. (FROM /B TO /C)
544	12-6-77	CHANGED 75 OHM 1/8 W RESISTOR TO 51 OHM AT IC AA PINS 2,3,14 & 15 AND IC BA - 2,3,14 &15; ADDED 2N3053 DIODE, 22 OHM AND 2K RESISTORS; CHANGED PC VOLTAGE DESIGNATIONS, -.75 TO -.65 and -3 to -2.9
1001	2-2-78	CORRECTED PARTS LIST.

21 NOV. 1978

REMARKS

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN
CHECKED
DATE

ENGINEERING CHANGE ORDERS

MODEL 370C

DRAWING No.