technical information manual

NIM MODEL 222/222N
DUAL GATE GENERATOR

Project Engineer: B. Yamrone
Operations: A. Michalowski
December, 1976

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

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Spring Valley, New York

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refine and improve the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Spring Valley, NY, telephone 914-425-2000, or from your local distributor in countries other than the U.S.A.

LeCROY RESEARCH SYSTEMS

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NIM Model 222/222N
Dual Gate Generator

FULL SCALE WIDTH switch: Selects output width range. In conjunction with Vernier Width, provides an output continuously variable from 100 nsec to 11 sec. Also selects LATCH mode.

Vernier Width potentiometer

Test Point: Provides a DC voltage related to the gate width in % of FULL SCALE WIDTH switch setting. See conversion chart.

START and STOP Inputs: Each accepts fast NIM or TTL levels.

OR Input(fast NIM level): Extends the preset gate output duration by the amount of time that the OR signal exceeds the preset width.

BLANK Input (fast NIM level): The portion of the output overlapping this pulse is suppressed. Delayed output is also suppressed, but this may be disabled by factory option.

BUSY Indicator: Red LED which lights when gate output is present, even if extended by OR input.

Complementary fast NIM level output.

Fast NIM level output.

Standard TTL level output (quiescently Logical 0).

Delayed Output: Fast NIM level pulse, 10 nsec wide, delivered at the trailing edge of the gate.

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TECHNICAL DATA

LeCroy RESEARCH SYSTEMS

NIM Model 222/222N/222NL

Dual Gate and Delay Generators

* **No deadtime**
* **Responds to TTL or fast NIM inputs**
* **"OR" input to permit extending gate with external signal**
* **Fast NIM (normal and complement) and TTL outputs**
* **NIM level blanking input**
* **NIM level delayed output**
* **Built-in bin gate drivers**
* **Presettable gate durations from < 100 nsec to > 11 sec**
* **Front-panel monitor point to permit determination of gate duration with standard voltmeter***
* **Does not require 6-volt NIM bin**

The LeCroy Model 222 Dual Gate and Delay Generator provides two complete delay/gate channels in a single NIM module, combining in one compact package many important features formerly requiring separate expensive circuits.

The Model 222 eliminates the problems exhibited by previously available gate generators. There is negligible recovery time associated with the unit at any width setting; it may be retriggered immediately after the gate returns to its quiescent state in all ranges. Each channel of this single module can also be used to provide delays and gate outputs and to drive bin gates in its own bin and several external bins. In addition, an "OR" input for each channel permits the gate and delay interval to be extended by an external input.

The Model 222 provides a range switch and a screwdriver-adjustable potentiometer to permit continuous adjustment of gate durations from less than 100 nsec to greater than 11 seconds. The approximate gate setting may be easily determined without an oscilloscope by means of the front-panel monitor point which provides a DC voltage related to the gate duration. A conversion graph is enclosed with the unit.* In addition to preset width ranges, the range switch has a "latch" position to provide a continuous gate controllable by either the "Start" and "Stop" inputs or by the "Start" and "Stop" pushbuttons.

The Model 222 is packaged in a NIM standard #1 width module with Lemo-type connectors. It is also available in a #2 width module with BNC or Lemo connectors as the Model 222N and Model 222NL respectively.

October 1977

* Front-panel monitor point available only in single-width version. BNC version has front-panel locking potentiometer.

Innovators in Instrumentation

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SPECIFICATIONS
NIM Model 222/222N/222NL
DUAL GATE AND DELAY GENERATORS

EACH CHANNEL

INPUT CHARACTERISTICS

Start Input:

One: responds to both fast NIM-level and TTL-level inputs.

Fast NIM Input Requirements: Greater than −600 mV enables; minimum width 5 nsec; 50 Ω impedance for any input from + 100 mV to −5.0 V.

TTL Input Requirements: Greater than +2.5 volts enables; minimum width approx. 20 nsec; high impedance for any input from +400 mV to +6 volts. (Requires +5 mA at +2.5 V.)

Stop Input:

One: Characteristics same as for "Start" input. Used when range switch is in Latch position. Can be used in Preset position but will cause a "delayed stop".

Blanking Input:

One: Requires fast NIM-level inputs (≥ −600 mV) 50 Ω impedance; blanks all outputs which occur during its presence, including the delayed output.* Maximum blanking rate, 80 MHz.

"OR" Input:

One: Requires fast NIM-level inputs (≥ −600 mV); 50 Ω impedance; extends preset gate duration by the portion of its input signal that occurs after the preset output time.

OUTPUT CHARACTERISTICS

Gate Outputs:

One standard fast NIM-level output (quiescently 0 volts; −750 mV during pulse) of approx. 2 nsec risetime; falltime slightly longer on wide widths.

One complementary fast NIM-level output (quiescently −750 mV; 0 volts into 50 Ω during pulse).

One TTL-level output (quiescently 0 volts; > +2.5 volts into 50 Ω during pulse).

Delayed Output:*

Delivers 10 nsec (FWHM) fast NIM-level signal into 50 Ω. Occurs approximately at the trailing edge of the preset or start-stop gate output (including any gate extension due to input "OR"); ≤ 2.5 nsec risetime.

Presettable Gate Durations:

Continuous from < 100 nsec to > 11 sec. plus latched position; full-scale switch determines range. On single-width version, screwdriver-adjustment vernier permits fine adjustment from ≤ 10% to > 110% of full scale (screwdriver included). Front-panel test point gives DC voltage related to gate width (in % of range switch setting). Conversion chart included with module. On double-width version, front panel locking potentiometer replaces the screwdriver adjust pot and monitor point. Output width jitter, approx. 0.05% of setting.

GENERAL

Recovery Time:

None; unit may be retriggered immediately after gate output returns to its quiescent state.

Input-Output Delay:

14 nsec.

Manual:

Front-panel "Start" and "Stop" pushbuttons permit manual operation when full-scale switch set on "latch", and single-shot presettable operation when full-scale switch is in any other position.

Bin Gate Driver:

Each channel has one rear-panel Lemo-type connector which switch selectably drives external bins in either normal or inverted direction. Logic 1: < 1 volt at 200 mA; logic 0.5 volts into high impedance (2 kΩ).

Channel Select Switch:

Rear panel 3-position switch (A/B/OFF) determines which channel drives the bin in which the Model 222 is located.

Busy Indicator:

Front panel LED remains on when gate output is present, even if extended by "OR" input.

Packaging:

Model 222: NIM-standard single-width module; Lemo-type connectors.
Model 222N: NIM-standard double-width module; BNC connectors.
Model 222NL: NIM-standard double-width module; Lemo-type connectors.

Current Requirements:

+12 V at 95 mA +24 V at 45 mA + 6 V at 235 mA (drawn from +12 V if unavailable)
−12 V at 180 mA −24 V at 80 mA

*Blanking of the delayed output may be disabled by factory option.

3. ADDENDA TO SPECIFICATIONS

None.

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OPERATION

A. INPUT CHARACTERISTICS

1. START and STOP Inputs

The START and STOP inputs respond to either fast NIM* or TTL level inputs. Since the Model 222 input circuit automatically responds to either type of signal, no switch selection or internal change is necessary. A fast NIM input "sees" an impedance of 50 Ω, while a TTL input "sees" a high impedance. The TTL input requires 5 mA at +2.5 V, increasing slightly as the input voltage is increased (i.e., 5.75 mA at +3.5 V). Protection is provided for currents of up to ±5 A for 1 μsec by a 47 Ω series-terminating resistor, clamping at 0 volts for negative pulses and at +6 volts for positive pulses.

It is important to note that the STOP input (or STOP pushbutton) is only intended for use with the FULL SCALE WIDTH switch set in the LATCH mode. However, if a Stop is applied while an output is present with the FULL SCALE WIDTH switch set at a finite range, the output pulse will nevertheless be terminated, but only after a short delay.

2. BLANK Input

The BLANK input responds to fast NIM level* inputs. Input impedance is 50 Ω, and input protection extends to at least ±5 volts. The blanking input suppresses only the portion of the Model 222 output pulse occurring during the blanking interval. The delayed output pulse is also suppressed on the standard unit, but this may be disabled as a factory option upon special request.

3. OR Input

The OR input responds to fast NIM level* inputs, has a 50 Ω impedance, and is protected to at least ±5 volts. Its specific function is to enable the user to easily extend the preset output width on the basis of external criteria, (e.g., extending an input inhibit to scalers or other data acquisition modules while a computer readout is still in progress).

* Fast NIM Levels: $-12\ \text{mA} \leq \text{Logical 1} \leq -36\ \text{mA}$
TTL Levels: $+2.0\ \text{V} \leq \text{Logical 1} \leq +5.0\ \text{V}$

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B. OUTPUT CHARACTERISTICS

1. Gate Outputs

a. General

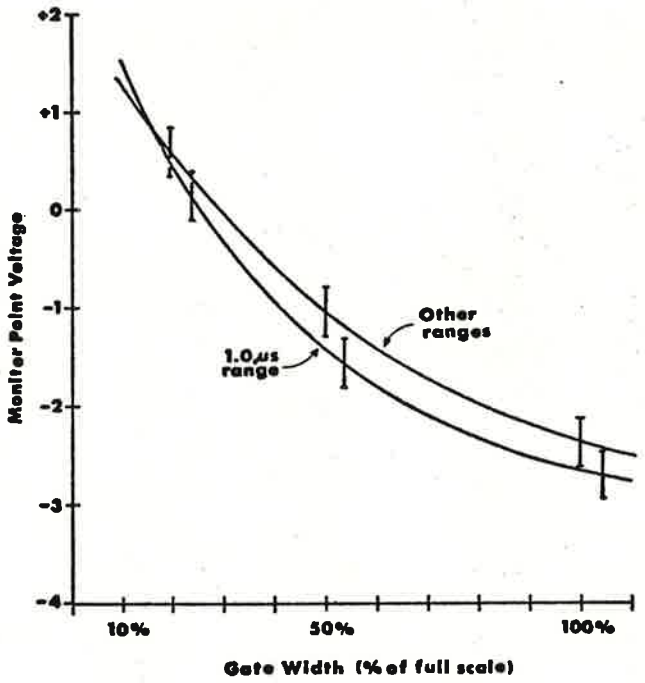
The Model 222 provides one standard fast NIM level output (quiescently 0 volts, -750 mV during pulse) of approximately 2 nsec risetime, one complementary fast NIM level output (quiescently -750 mV, 0 volts during pulse), and one TTL level output (quiescently 0 volts, >+2.5 volts into 50 Ω during pulse). The falltime of the fast NIM outputs is generally similar to the risetime, except at large output widths where the Model 222 timing stage causes a slight degradation of the falltime.

b. Gate Durations

Preset output durations extend from <100 nsec to >11 sec and are determined by a combination of the FULL SCALE WIDTH selector switch and the screwdriver-adjustable vernier. On the BNC version (Model 222N), a lock-in potentiometer replaces the switch and vernier, giving direct visual indication of output width setting. On the LEMO Model 222, a DC level available at the front-panel test point gives an indication of the output width setting as a percentage of the FULL SCALE WIDTH switch setting, from approximately 10% to 110%. The conversion chart representing this test point output is shown on the following page.

When the output width range selector switch is set in the LATCH position, the output width of the Model 222 is determined by either the START and STOP pushbuttons, or the START and STOP inputs. Once "started", the Model 222 output will stay on indefinitely until "stopped" or until power is turned off.

Model 222—Dual Gate Generator
CONVERSION CHART



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2. Delayed Output

The delayed output (DEL) delivers a 10 nsec FWHM (Full Width Half Maximum) fast NIM level signal into 50 Ω. The leading edge of this output occurs shortly before the trailing edge of the normal gate output pulse. In other words, its leading edge occurs a few nsec before the normal gate output is fully completed. This characteristic is necessitated by internal circuitry which actually creates the full gate output width from the addition of an internal pulse generated by the delayed output onto a slightly shorter-than-setting gate output. This technique enables the Model 222 to perform in a mode exhibiting no recovery time, which permits a second output to appear instantaneously after the first output ends.

The delayed output is normally suppressed by the BLANK input, but this feature may be disabled by factory option. This output is often useful for creating a "delay and gate generator" using two channels of the Model 222. In this case, either the delayed output or the complementary output of Channel 1 can be fed into the START input of Channel 2 of the Model 222 to create an output pulse of specified width occurring at a time determined by the output width setting of Channel 1. More standard applications involve using the delayed output to trigger a computer readout cycle, as a reset pulse, or as a "flag" pulse to indicate the completion of a data acquisition interval.

3. Bin Gate Driver Outputs

a. For Remote Bins

The Model 222 provides a rear-panel LEMO connector output which switch-selectably drives external bins in either the normal or inverted direction. For the normal direction, the Model 222 will clamp 200 mA for a Logical 1 (less than 1 volt). A Logical 0 is a high-impedance open-collector-type output. A 2 kΩ resistor provides pullup to +5.2 volts.

NOTE: The NORMAL position disables the driven bin for the duration of the Model 222 output. The INVERTED position enables a normally disabled bin during the gate output interval.

b. For Driving the Local Bin

Either Channel 1 or Channel 2 of the Model 222 can drive the bin from which the unit is powered. A rear-panel 3-position switch selects which channel, with the third position (OFF) available to disassociate the local bin from the influence of the Model 222. The NORMAL position serves to disable the driven bin for the duration of the Model 222 gate output.

C. GENERAL

1. Recovery Time

With the Model 222, it is possible to get a second gate output immediately after the first gate output. In this respect, no delay period (deadtime) is required before the Model 222 can be retriggered. This feature is made possible by the or-ing of two internal signals to create one output signal with a width corresponding to the front-panel rotary switch setting and vernier.

2. BUSY Indicator

The Model 222 provides a front-panel LED (light-emitting diode) indication of when a gate output is present. This LED lights whenever an output is present, even if extended by an OR input. Because no mechanism is provided to slow down the turning on and off of the LED for each gate output, at short output widths or high rates, the LED will appear to the eye as a steady "on" condition.

3. Packaging

The Model 222 is packaged in a standard NIM module conforming to the standards outlined in AEC-NIM Report TID 20893, Rev. 3. The LEMO connector version has a #1 front-panel width, while the BNC version utilizes a #2 width due to the size of the front-panel lock-in potentiometer and the BNC connectors.

4. Current Requirements

The Model 222 dissipates 7.5 watts of power and requires the following NIM voltages and currents:

-24 V at	80 mA
-12 V at	160 mA
+ 6 V at	235 mA*
+12 V at	95 mA*
+24 V at	45 mA

* It is important to note that the Model 222 will automatically draw current from the +12 volt supply if no +6 volt supply is available. For this reason, a +6 volt NIM bin is not necessary to power the Model 222. When only the +12 volt supply is available, the power dissipation increases by 470 mW.

FUNCTIONAL DESCRIPTION

A. GENERAL

The Model 222 is a two-channel NIM module. It can be divided into three major sections:

The Start-Stop, Latch and Or-ing stages
The Ramp and Ramp Level Detector stages
The Output and Blanking stages

Each of these will be discussed briefly. The reader should refer to the circuit schematic (located at the end of this manual), the functional block diagram (on page 2-5) and the timing waveform diagrams (on page 2-4).

B. START-STOP, LATCH AND OR-ING STAGES

The Start and Stop input stages are identical. Each is composed of a special input stage capable of accepting a low-impedance NIM input (-500 mV into 50 Ω) or a high-impedance TTL input (+2.5 V at 5 mA) using the same input connector. This is accomplished by requiring the input NPN transistor to provide a low-impedance path for negative signals, routing the input current of the negative input signal to the inverting input of the MC10115 receiver, causing it to go low. The same effect is accomplished with a positive input pulse, which turns off the input PNP transistor, enabling the 2kΩ resistor on the MC10115 to pull the input low. A third method of inputting a Start or Stop is via the respective pushbutton which, when depressed, causes circuit operation similar to that for the positive input.

When the inverting input of either the Start or Stop receivers (MC10115) is taken more negative than the non-inverting input, the output will go high. Even for slow or marginal inputs, the output is fast due to both AC and DC positive feedback to the non-inverting input.

From this point on, the Start differs from the Stop. The Start is first differentiated and the resulting "leading-edge" pulse is shaped by an emitter-coupled logic (ECL) receiver (which is inhibited if the Ramp section is already busy). The resulting pulse is then used to set the Latch, (composed of a heavily fed-back section of ECL receiver), by forcing the Latch output positive. (See "Presettable Width Mode" timing diagram). This pulse is present for the duration of the Latch and is fed to the Ramp section to start the ramp cycle as well as to provide a prompt input to the final Or stage which is used to drive the output stage.

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Once a ramp is generated (see next section), the Ramp Detector output is fed to the Or along with the Latch output to hold the output stage "on" and inhibit the Start input for the entire ramp duration. At the maximum amplitude of the ramp, the Stop-level Detector (in the Ramp section) will reset the Latch, but the output of the final Or will still be present until the ramp is totally recovered, at which point the Ramp Detector will return to its quiescent level, removing drive from the output stage.

The STOP input is intended primarily for use in the LATCH mode of operation. In this mode, the Ramp section is disabled, so the output stage follows the Latch output only. (See "Start-Stop Mode" timing diagram). A Stop input will reset the Latch previously set by the Start. Therefore, the output stage will be driven only for the time from Start to Stop. If a Stop input is generated when operating in any of the preset modes, it will reset the Latch before the end of the ramp, causing the ramp to be shortened, but because the output stage follows the total ramp duration, the output width will not be promptly terminated, but will be extended by the ramp recovery time (which depends on both the range setting and the amount of preset time which had already elapsed before the Stop was generated).

The input Or stage converts NIM levels to offset ECL levels required to drive directly the final Or stage, independent of the states of the Start-Stop stage, the Latch, the Ramp stage, etc. Thus it provides a final output width equal to the input OR width (or to the overlap of it and the Start-Stop Latch and/or the Ramp Detector).

C. RAMP AND RAMP DETECTOR STAGES

The Ramp stage is composed of a capacitor, (C1 through C8, as selected by the FULL SCALE WIDTH switch), resistor R1 (paralled by R2 on the 1.0 μsec range), and a 10 mA current source (transistor Q15). The current source is quiescently on, causing the ramp to be clamped at about +3 volts by the 1N702 zener diode and the base-emitter drop of Q2. When the Start-Stop Latch is set by a Start pulse, Q15 current source is disabled and the ramp begins to discharge toward -3 volts at a rate determined by R1 (15 kΩ, or 7.5 kΩ when paralled by R2 on 1.0 μsec range) and C(n), which is determined by the FULL SCALE WIDTH switch setting. (See "Presettable Width Mode" timing diagram).

As soon as the current source is turned off, the integrated circuit comparator used as the Ramp Detector is enabled because Q15 collector goes to zero. When the ramp reaches the voltage level set by the 2 kΩ front-panel vernier width potentiometer, the Stop-level Detector comparator I.C. resets the Start-Stop Latch. This enables the current source and the ramp is returned to its quiescent level at a rate determined primarily by the 10 mA of the current source and the value of C(n). When the ramp reaches the clamp level

determined by transistor Q2, the current is shunted to Q2 collector, the Ramp Detector turns off, the output drive to the ECL final Or and the inhibit to the Start stages are removed, and the unit can be retriggered.

D. OUTPUT AND BLANKING STAGES

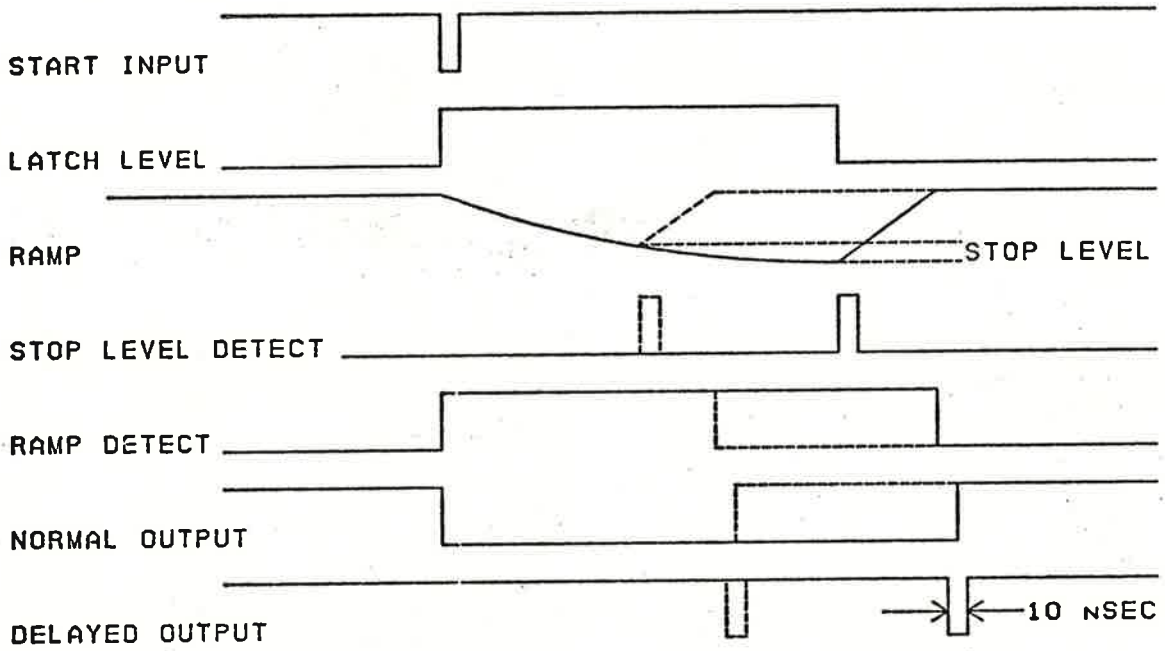
The NIM driver output stage is a 16 mA differential stage operating from the output Or (with a 5 nsec stretcher stage) via a 1N706 zener diode to provide level shifting. Both the normal and complementary outputs are made available and they are individually clamped at -1 volt if no output load is present.

The TTL and Bin Gate output stages and the BUSY LED driver are driven from a stage the same as above except that the collectors are referenced to positive voltages. The TTL stage uses a double emitter-follower to provide stiff drive for either logic level. The Bin Gate output uses one of two switch-selectable, stiff, clamp-to-ground inverting transistors. One provides a normal level to inhibit modules on the bin gate bus for the duration of the output. The other provides an inverted level to inhibit quiescently and to enable only during the output duration. The Busy driver holds the BUSY LED on for the duration of the output, stretching short pulses enough to provide a visual indication.

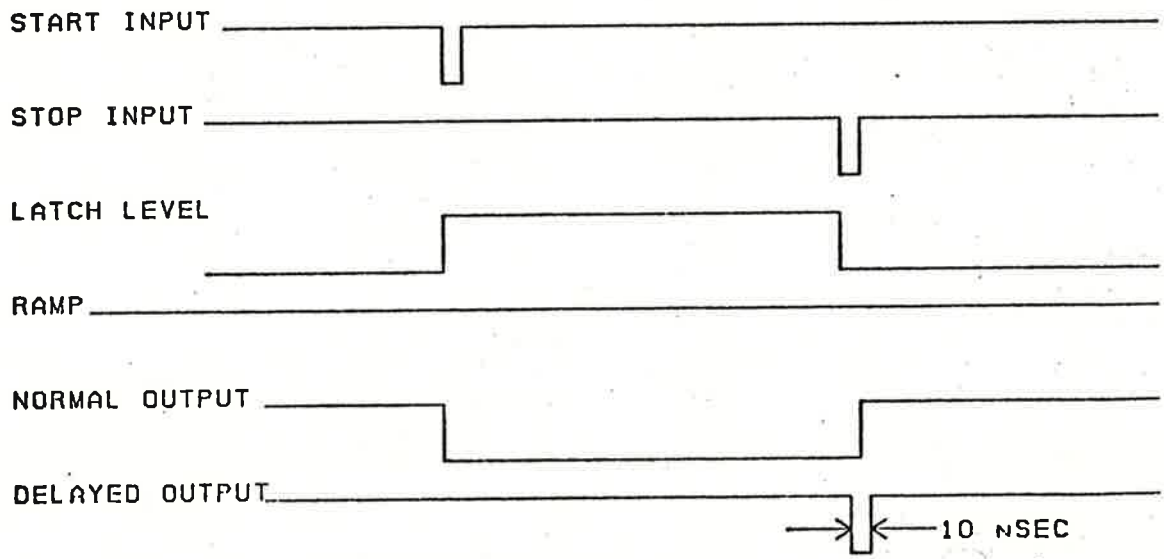
The Delayed Output stage is also similar to the NIM driver stage, except that only the normal output (quiescently zero, -16 mA during pulse) is available and the stage is driven from a trailing-edge differentiator-shaper stage to generate a 10 nsec wide pulse.

The Blanking input converts a NIM level input to a proper level to disable the three differential stages, and therefore all outputs and the BUSY LED, for the duration of the Blanking input.

MODEL 222 DUAL GATE GENERATOR
TIMING DIAGRAMS



PRESETTABLE WIDTH MODE



START-STOP MODE

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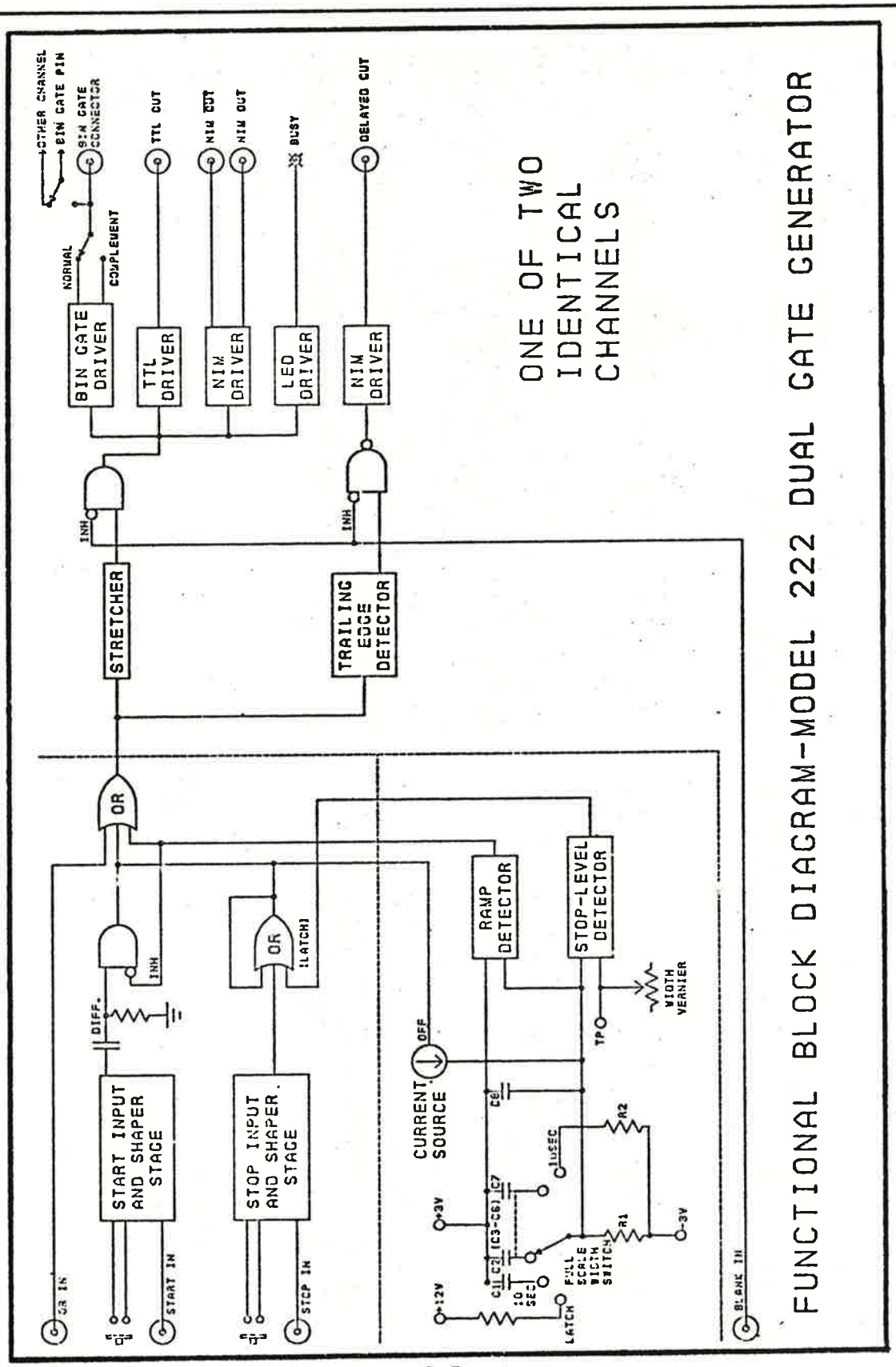

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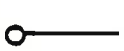
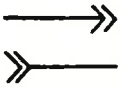
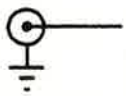
STANDARD DRAFTING SYMBOLS, ELECTRONIC

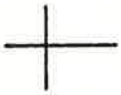

Connection to any given voltage.

Line ending at the edge of the sheet indicates continuance on another sheet.


Male pin or card edge contact.


Female pin, socket or card edge connector.


Coaxial connector.


No connection.

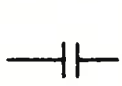

Connection.


Resistor, 1/4 W, ±5%, value in ohms (unless specified otherwise).

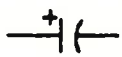
Resistor, 1/4W, ±1%, value in ohms (unless specified otherwise).

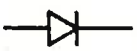

Resistor, variable, any type.


Resistor, variable, any type.


Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).


Capacitor, variable. Values in Picofarads (unless specified otherwise).


Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).

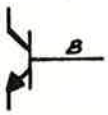

Diode, signal or rectifier.


Diode, zener.

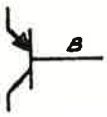

Diode, tunnel.


Diode, snap.

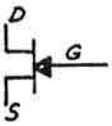

Light emitting diode (LED).



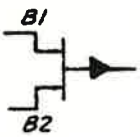
NPN Transistor.



PNP Transistor.



Field effect transistor, P Channel.



Field effect transistor, N.


Air choke.


Ferrite bead.


Ferrite core choke, Z 500 ohms when f ≥ 60 MHz (unless otherwise indicated).


Ferrite core choke, 40 uH, (unless otherwise indicated).

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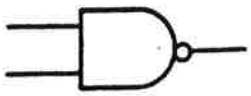
LeCroy Research Systems Corp.
West Nyack, New York

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL).

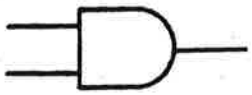
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

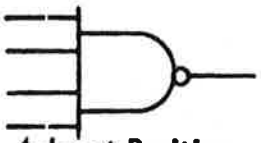
Supply voltages of IC's are shown in a table on each schematic.



2-Input Positive NAND Gate

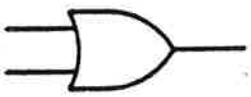


2-Input Positive AND Gate

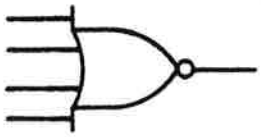


4-Input Positive NAND Gate

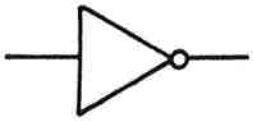
2- Input Positive NOR Gate



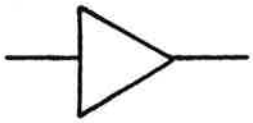
2-Input Positive OR Gate



4-Input Positive NOR Gate



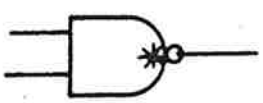
Inverter or Inverting Buffer



Non-Inverting Buffer

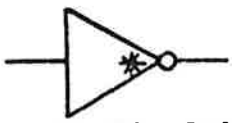
Exclusive OR Gate

Open collector outputs are identified by an asterisk (*) on the output connection.



2-Input Positive NAND Gate W/Open Collector

2-Input Positive OR Gate W/Open Collector



Non Inverting Buffer W/Open Collector

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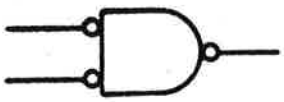
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS
EMITTER - COUPLED LOGIC (ECL)

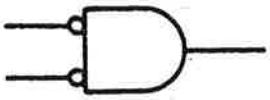
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

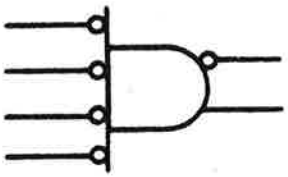
Supply voltages of IC's are shown in a table on each schematic.



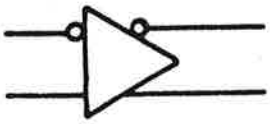
2 - Input Gate.
Negative AND (Positive OR) Gate.



2 - Input Gate.
Negative NAND (Positive NOR) Gate.

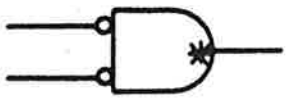


4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.

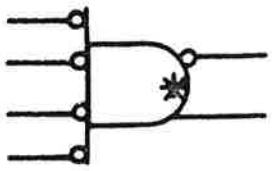


Differential
Amplifier.

Open emitter outputs are identified by an asterisk (*) on the output connection.



2 - Input Negative NAND Gate.
With Open Emitter.



A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.

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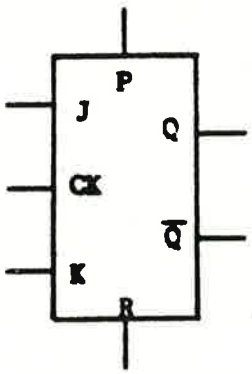
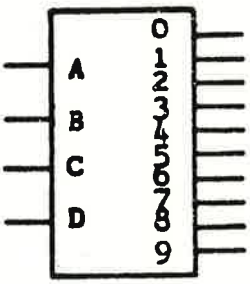
West Nyack, New York

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL) OR EMITTER COUPLED LOGIC (ECL).

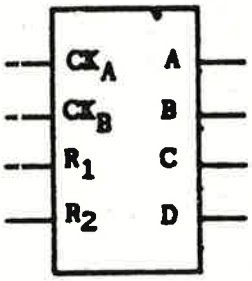
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave Flip-Flop

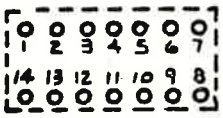


BCD-To-Decimal Decoder-Driver



Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.



Bottom View

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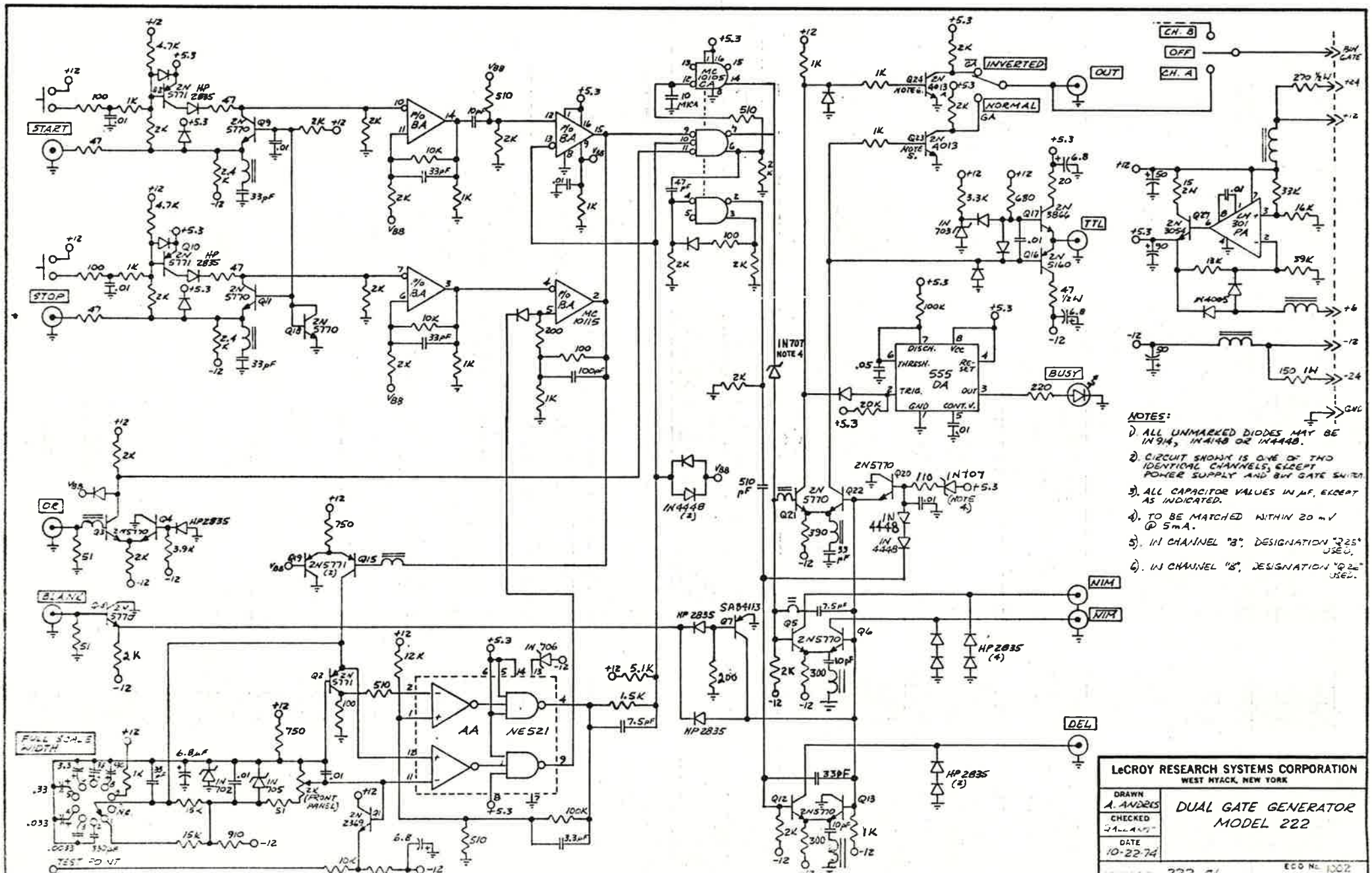

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN A. ANDRES	DUAL GATE GENERATOR MODEL 222
CHECKED GALLANT	
DATE 10-22-74	

ECO No. 1002

ECO NO.	DATE	DESCRIPTION
798	12-18-74	33 pF CAP REMOVED FROM Q5 & Q6 EMITTERS (WITH BEAD)/7.5 pF CAPACITORS ADDED: Q5B TO Q6B AND Q12B TO Q13B/CHANGED: 33pF CAPACITOR WITH BEAD AT Q12 & Q13 EMITTERS CHG. TO 10pF WITHOUT BEAD. / Q1 CHANGED FROM 2N5770 TO 2N2369A/ PIN #1 OF TIME RANGE SWITCH: 10 K CHANGED TO 15K/ 2K RESISTOR ADDED PIN 2 OF IC "CA" TO GROUND (SCHEMATIC ONLY.)
868	June 12 1975	BIN GATE DRIVER TRANSISTORS CH. FROM 2N3866 TO 2N 2369A, HP2835 DIODES REMOVED AT SAME.
893	7-18-75	PARTS LIST CORRECTION ONLY: 1N703 ADDED/
910	8-19-75	TWO HP2835s CHANGED TO 1N4448 (AT PIN 10 OF MC 10105)/PARTS LIST ONLY: 12 OHMS CORRECTED TO 12K (TWO).
927	10-7-75	CHANGE TO NEW WRAPAROUND: PARTS LIST. TAPING /E to /F.
966	10-29-75	ALL REMAINING .05 CAPACITORS CHANGED TO .01, 25V.
019	12-29-75	PARTS LIST CORRECTION ONLY: 1N4001 DIODES CORRECTED FROM 4 TO 1.
060	2-25-76	AT PIN 6 OF 555: .01 uF CAPACITOR REPLACED WITH .05 (ASSEMBLY ONLY).
086	3-19-76	ALL 18 MBD 101 DIODES CHANGED TO HP2835/ HARDWARE CORRECTION (PARTS LIST ONLY)
179	6-16-76	Q24, Q25, Q26 AND Q23 CHANGED TO 2N4013.
226	9-8-76	5.1 K RESISTOR FROM PIN 2 OF IC "DA" CHANGED TO A 1N4448 DIODE.
309	1-12-77	222N ONLY: PARTS LIST CORRECTION.
314	1-18-77	CHANGED MATCHED 1N706's TO MATCHED 1N707. CHANGED 5.1K RESISTOR AT Q4E TO 2K. CHANGED 75 OHM AT Q20B TO 110 OHM. CHANGED HPA-2835 AT Q20B TO 1N4448. CHANGED Q7(2N5771) TO SAB-4113. CHANGED 680 OHM AT Q7B TO 200 OHM. LEFT OUT 7.5pF CAPACITOR FROM Q7B TO Q7C. ADDED 1/2 BEAD TO 7.5pF CAPACITOR BETWEEN Q5B AND Q6B. ADDED 10pF CERAMIC CAPACITOR WITH FULL BEAD TO Q5 AND Q6E TO GROUND. CHANGED 7.5pF CERAMIC CAPACIOTR TO 33pF CERAMIC AT Q12 & Q13B. CHANGED 2K AT Q13B TO 1K, AND ADDED FULL BEAD TO 10pF CAP. AT Q12 AND Q13B.
374	4-22-77	CHANGED 510 OHM RESISTOR AT Q5 AND Q6E TO 300 OHM; CHANGED 510 OHM RES. AT Q12 AND Q13E TO 300 OHM; ADDED 1 FULL BEAD AT Q21B.

REMARKS

PAGE ONE OF TWO

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN
CHECKED
DATE

ENGINEERING CHANGE ORDERS

MODEL 222

DRAWING No.

ECO NO.	DATE	DESCRIPTION
414	6-24-77	REVERSED FIVE POLARIZED CAPACITORS ON FRONT PANEL SWITCH - 330 uF, 33 uF, 3.3 uF, .33 uF, .033 uF BOTH CHANNELS.
468	9-19-77	REVERSED CHANGES DONE ON LAST ECO (414) - REVERSED POLARITY ON 5 CAPS ON FRONT PANEL SWITCHES.
1001	2-2-78	CHANED 1N4001 DIODE TO 1N4005.
1002	5-3-78	CORRECTED SCHEMATIC. (SHEET 1 OF SCHEMATIC AFFECTED)
1003	6-28-78	MADE 222N AN "ADDER" PARTS LIST.
1004	8-9-78	PARTS LIST UPDATED ONLY.
1005	8-28-78	PARTS LIST CORRECTED ONLY.

REMARKS

PAGE TWO

LeCROY RESEARCH SYSTEMS CORPORATION

DRAWN

CHECKED

DATE

ENGINEERING CHANGE ORDERS

MODEL 222/222N

DRAWING No.

ECO NO.	DATE	DESCRIPTION
1000	8-15-78	GENERATED PARTS LIST.

REMARKS

LeCROY RESEARCH SYSTEMS CORPORATION

DRAWN	ENGINEERING CHANGE ORDERS
CHECKED	MODEL 222NL
DATE	