technical information manual

NIM Model 127FL

Dual Bipolar Linear Fan-In

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
West Nyack, New York

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique,reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refine and improve the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Spring Valley, NY, telephone 914-425-2000, or from your local distributor in countries other than the U.S.A.

LeCROY RESEARCH SYSTEMS

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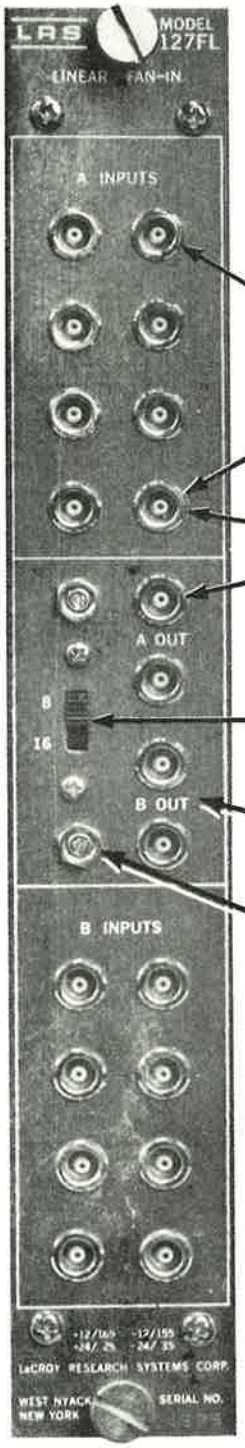
technical
information
manual

NIM Model 127FL

Dual Bipolar Linear Fan-In



Channel A inputs (50Ω impedance; linear for inputs between ±1 V; unused inputs need not be terminated; protected to ± 100 V for transients.

Input→Output delay: 4 nsec.
Gain: 1.0, non inverting.

Output mixing switch - selects 2 independent 8 channel fan-ins or single 16 fold fan-in.

Bridged current source outputs provide full output into one 50 Ω load, half amplitude into two loads.

DC offset adjust, channel B

Power consumption: +24 @25 mA, +12 @ 180 mA, -12 @ 150 mA, -24 @ 35 mA.

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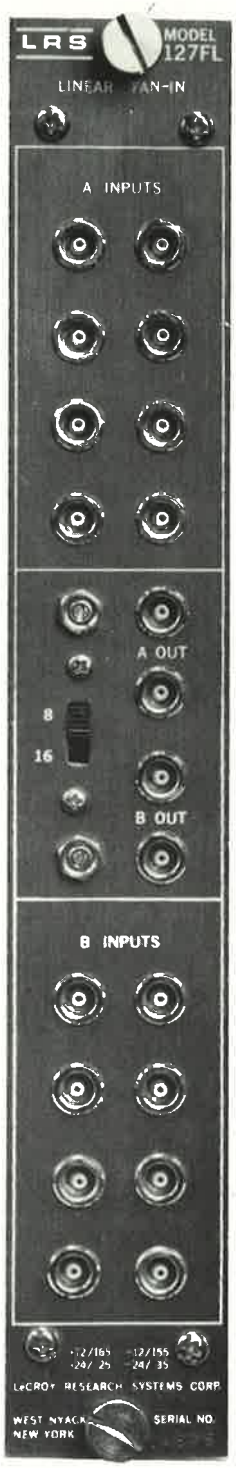
West Nyack, New York

TECHNICAL DATA

LeCroy



NIM Model 127FL

Dual Bipolar Linear Fan-In

The LRS Model 127FL is a fast, versatile bipolar linear fan-in featuring unity gain, non-inverting operation, direct-coupled circuit design and freedom from duty cycle limitations and rate effects. The Model 127FL operates as either a dual 8-fold linear fan-in or as a single 16-fold linear fan-in. With rise and fall times of $\leq$ 2.5 ns and an absolute delay of less than 4 ns, the Model 127FL may be used to combine nanosecond pulses from as many as sixteen different sources. All inputs are terminated in 50 Ω. Pulses may be applied separately or simultaneously to one or both channels; channel inputs and outputs at ground potential allow compatible interconnection between units. The current source output stage permits paralleling, by external cables, a large number of similar high-output impedance channels. The front-panel MIXED switch connects Channel A output to Channel B output. The output amplitude of each channel is the algebraic sum of the input amplitudes. Negligible stretching on overload allows use as a logic fan-in of NIM level inputs.

Offering integral linearity of better than 1% over a range from 0 to $\pm$1 volt, the 127FL features two bridged outputs per channel, eliminating the need for an external fan-out when driving both ADC and discriminator inputs. The maximum output amplitude characteristic of the 127FL is +2.4 volts and −1.6 volts into 50 Ω. When both connectors of the bridged outputs are terminated into 50 Ω, each delivers a half amplitude signal into its load.

July 1976

Innovators In Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION · SPRING VALLEY, N.Y. 10977 · TELEPHONE: (914) 425-2000

SPECIFICATIONS
NIM Model 127FL
DUAL BIPOLAR LINEAR FAN-IN

INPUT CHARACTERISTICS

Number of Channels:	Two.
Inputs:	8 per channel; direct coupled. (Unused inputs need not be terminated.)
Impedance:	50 Ω.
Polarity:	Positive or negative.
Reflection Coefficient:	Less than 7% for inputs of 2 ns risetime.
Input Protection:	Inputs protected against 10 μs transient overloads, up to ± 100 volts. DC overload characteristics are determined by the 500 mW dissipation limit of the 50 Ω terminating resistors.

OUTPUT CHARACTERISTICS (All characteristics for Dual Eight operation with single 50Ω load except as specified).

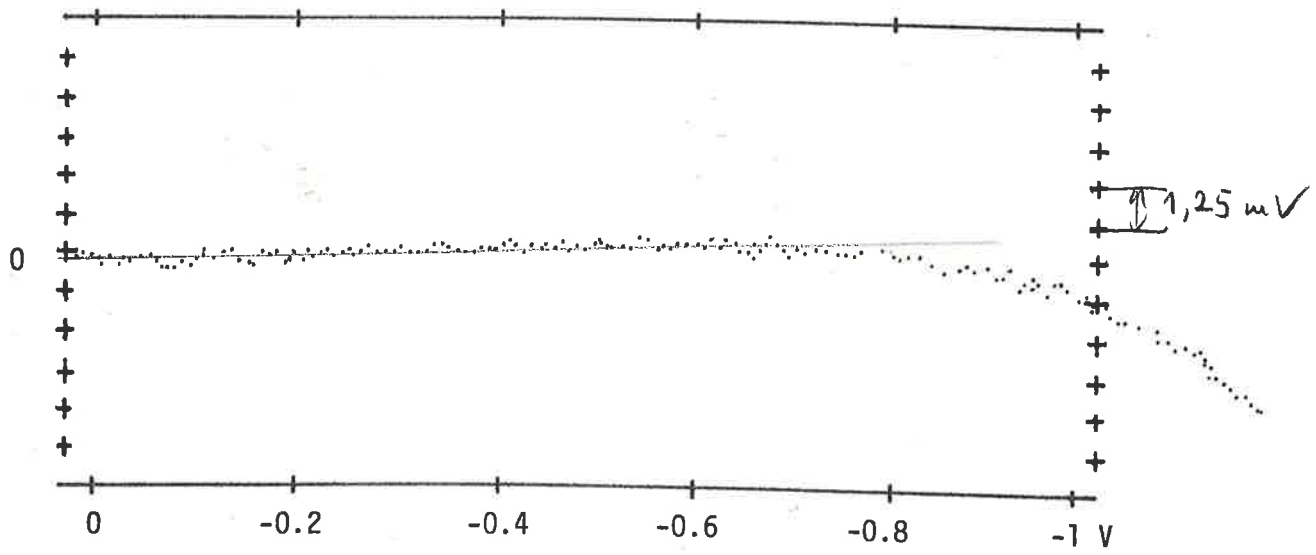
Outputs:	Two per channel, bridged: full amplitude output is delivered into 50Ω; if both connectors used, half amplutude is delivered into each 50Ω load. Direct-coupled; current source.
Maximum Amplitude:	Linear region, ± 20 mA (± 1.0 volts into 50Ω). Limits at +48 mA (+2.4 volts into 50Ω) and −32 mA (−1.6 volts into 50Ω).
Risetimes and Falltimes:	2.5 ns typical, 3.0 ns maximum, 10% to 90%, with one output per channel terminated in 50Ω (slightly faster with both terminated). Single sixteen mode increases times by approximately 20%.
Overshoot:	≤ 7% for 1 ns risetime, ± 800 mV input pulses into 50Ω, larger into 25Ω.
Current Gain:	1 ± 2% into 50Ω for ≤ 20 mA; 3 dB point at 150 MHz.
Duty Cycle Limitations:	None.
Noise:	≤ 750 microvolts RMS.
D.C. Offset:	Adjustable with front-panel potentiometer.
D.C. Offset Stability:	Better than 0.25 mV/°C and <4 mV/% of variation of any power supply (with 50Ω load).
Stage Delay:	4 ns.
Overload Recovery:	Approximately 1 ns with eight simultaneous NIM level (−800 mV) inputs.
Non-Linearity:	Less than 1% over operating range of 0 to ± 1.0 volts; (<5% to ± 1.5 volts).

GENERAL

Output Mixing:	A front panel switch combines the outputs of the two 8-input channels to provide one 16-input channel.
Packaging:	RF shielded AEC/NIM #1 module; dimensions 1.375 x 8.75 x 10 inches deep. LEMO-type connectors.
Current Requirements:	+ 24 volts at 25 mA, + 12 volts at 180 mA, −12 volts at 150 mA, and −24 volts at 35 mA.

OPERATION

1. Linearity: A typical integral linearity plot for the Model 127FL is shown below. The output of the unit under investigation was uniformly sampled over the range indicated. Eight identical inputs were used. The data collected of input voltage vs output voltage were fit to the best straight line using a least-squares fitting procedure. The integral linearity plots show the difference between the output voltage and the best fit plotted against input voltage. As is evident from the data presented, the linearity of the Model 127FL is excellent to 1 V output into 50 Ω. The scatter in the data points is indicative of the RMS circuit noise.



VERTICAL SCALE = 1.25 mV/DIV DEVIATION FROM BEST STRAIGHT LINE

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2. Output Limiting: The output of the Model 127FL limits at +48 and -32 mA per channel. This corresponds to a maximum amplitude of +2.4 V and -1.6 V into 50 Ω. When used as a single 16 fold fan-in, the output current from both channels is added at the output, but the output will begin to saturate at greater than ±2.5 V. The maximum linear output per channel in both modes is the same.

3. Output Zero Adjust: Care must be taken in adjusting the output DC levels of the unit. For best results, adjustment should be made under the final termination conditions. The channels should be separately adjusted in the dual 8-fold mode before switching to the single 16-fold mode. If not, it would be possible to, say, adjust one channel +50 mV and the other to -50 mV, thus cancelling the offset in the 16-fold mode. If the unit were then set to the dual 8-fold mode, a large DC level would exist on both channels which could cause problems in the subsequent electronics.

4. Gain: Although the current gain of the Model 127FL is unity, the voltage gain is dependent upon the load (see specification section). This fact is particularly important if unused outputs are terminated or if more than one 50 Ω cable is driven by the output of the 127FL.

5. Termination: The overshoot of the Model 127FL is load dependent. The specification quoted (7%) was measured with only one 50Ω load. Somewhat better overshoot and rise and fall times are obtained at the expense of voltage gain if unused outputs are terminated with 50 Ω. For example, in the dual 8 fold mode, both connectors should be terminated in 50Ω ; in the single 16 fold mode, one connector of each bridged pair should be terminated in 50 Ω.

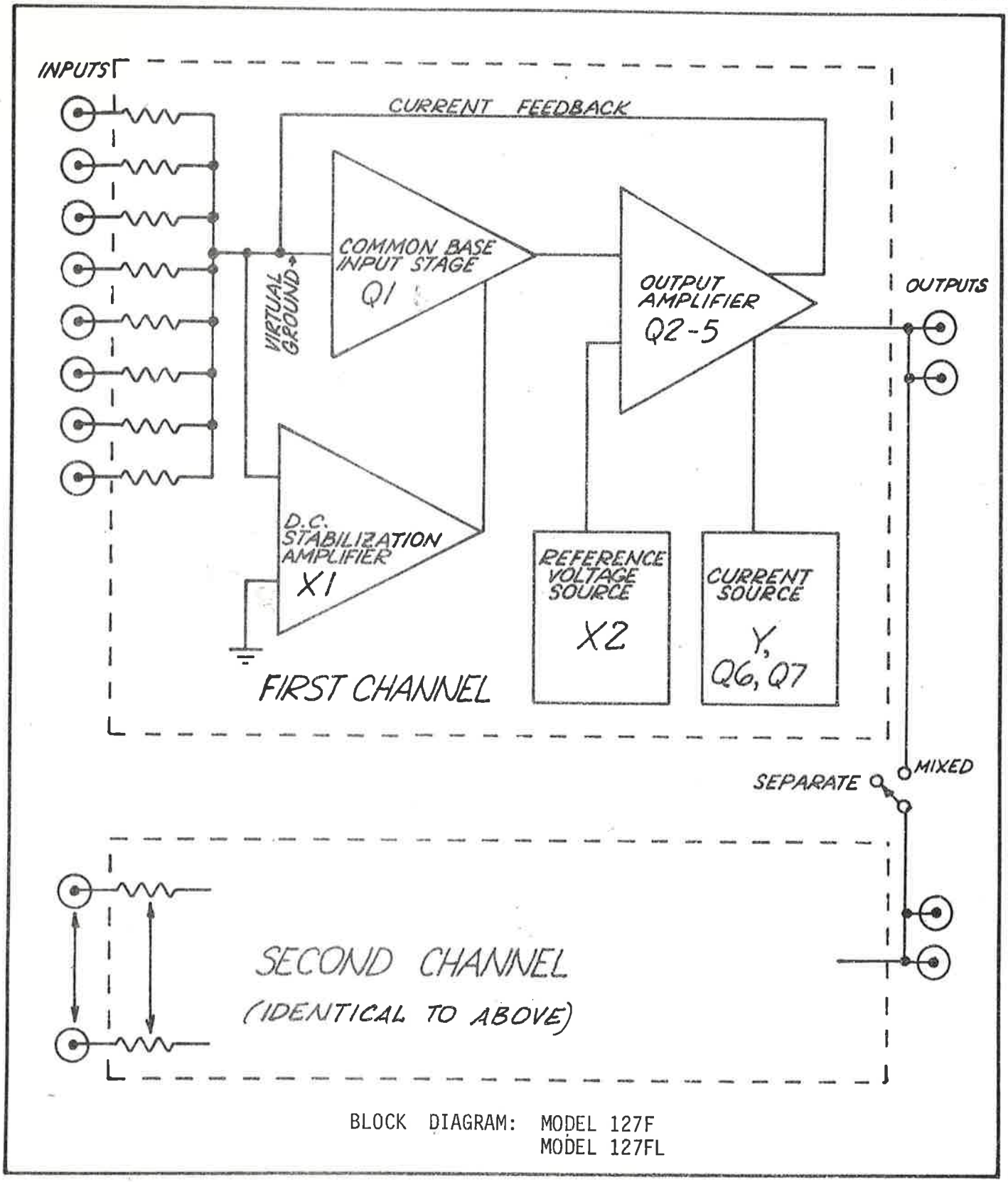
6. Output Mixing: The Model 127FL may be used as either a dual 8 fold fan-in or a single 16 fold fan-in. Selection of this mode is made via a front panel switch. Care should be taken to recheck terminations and the D.C. offset whenever the mode is switched from one condition to the other.

7. Bridged Outputs: Each channel drives two output connectors which are wired in parallel. This facility allows convenient fan-out to two subsequent circuits (e.g. ADC and discriminator) or the cascading of several 127FL outputs. Note that cascading outputs also adds output dc levels and noise.

Each channel of the Model 127FL consists of a direct-coupled, very high speed operational amplifier operated in a current-summing mode. Inputs are applied through eight 100 Ω precision input resistors to a common point which is maintained as a virtual ground by the operation of the amplifier feedback. Each input has an additional 100 Ω resistor to ground to provide proper 50 Ω input termination. The input currents are therefore halved, summed, and injected into the virtual ground. The amplifier then provides a gain of 2 to supply an output current equal to the total sum of the inputs.

Q1 functions as a common base amplifier. Signal current injected into its emitter from the input resistors appears at its collector and drives the input bases of a double differential stage consisting of Q2, Q3, Q4, and Q5. Approximately one half of the current is taken from the paralleled collectors of Q2 and Q3 and returned as feedback to the emitter of Q1. This feedback current is opposite in polarity to the signal current remaining (after being halved by the input resistors) and operates to cancel the current at the emitter of Q1. A current equal and opposite to the current which was halved for feedback, and therefore identical to the actual input signal current, appears at the collectors of Q4 and Q5. This is the output current of the fan-in which is delivered to the output connector. Resistors R10 and R11 are not exactly equal in order to provide compensation for beta losses in Q1, and for finite loop gain to make the fan-in output amplitude exactly equal to the input amplitude.

Diodes D1 and D2 are normally non-conducting. Input signals beyond the linear range of the fan-in cause one or the other of these diodes to conduct on overload, thus providing protection for the subsequent circuitry and maintaining an approximate input match. Amplifier X1 stabilizes the emitter voltage of Q1 against long-term drift. Amplifier Y, in conjuction with Q6 and Q7, forms a precision, high-stability current source whose current is equal and opposite to that quiescently standing in Q4 and Q5. The output of the fan-in is thus quiescently at approximately ground potential. It may be adjusted to zero by means of the front panel pot R33 which adjusts the magnitude of the current supplied by the current source. Note that the magnitude of the output offset voltage is proportional to the resistance to ground at the output and should normally be measured with a 50 Ω load in place. The output impedance of the circuit is very high, permitting cascading many channels of fan-in on a single cable without interaction or loading. Amplifier X2 provides a constant voltage reference for the bases of transistors Q4 and Q5. Diode D3 and transistors Q8 and Q9 provide anti-saturation control when the amplifier is overloaded and the output runs out of current.



BLOCK DIAGRAM: MODEL 127F
MODEL 127FL

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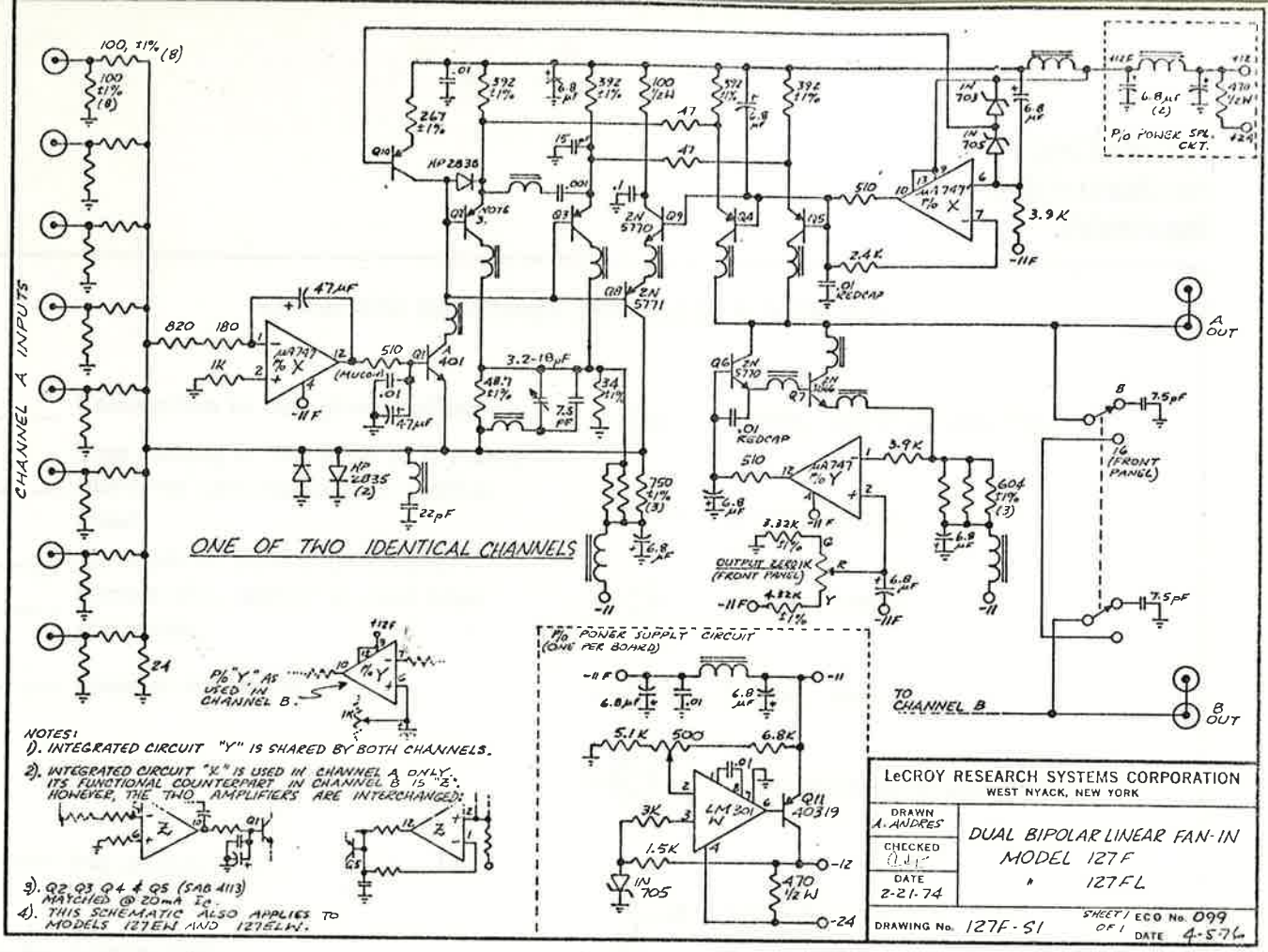

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WEST NYACK, NEW YORK

DRAWN A. ANDRES	DUAL BIPOLAR LINEAR FAN-IN
CHECKED	MODEL 127F & 127FL
DATE 2-21-74	

DRAWING No. 127F-S1 SHEET 1 OF 1 ECO No. 099 DATE 4-5-76

ECO NO.	DATE	DESCRIPTION
918	9-11-75	MECHANICAL ONLY: BOARD TAPING CHANGED TO FIT NEW WRAPAROUND.
967	11-3-75	OP AMP COMPENSATION CAP CHANGED FROM .05 TO .01, 25V.
003	12-22-75	ALL A492 (A430) CHANGED TO FLRS 003 (FMT 1190). PARTS LIST ONLY.
066	3-12-76	FOUR 47uF CAPACITORS ADDED. PARTS LIST ONLY: HARDWARE CORRECTED.
074	3-16-76	ALL MBD 101 DIODES (6PLACES) CHANGED TO HP 2835/ AT BASE OF Q6 - ADD .01 MONOL. CAPACITOR TO EMITT. BUSS FROM Q1 Emitter AND 7.5 pF CAP IS CUT AND FERRITE BEAD INSTALLED BETWEEN TRIMMER & 7.5pF AND THE REST OF THE BUSS/
099	3-29-76	TWO TRANSISTORS CHANGED FROM LRD 003 TO A 401.
~~136~~	~~4-5-76~~	~~TWO 3.2 - 18 VARIABLE CAPACITORS CHANGED TO 6 - 35 pF.~~ CANCEL.

REMARKS

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DRAWN	ENGINEERING CHANGE ORDERS
CHECKED	MODEL 127 F
DATE	

DRAWING No.

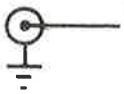
STANDARD DRAFTING SYMBOLS, ELECTRONIC


Connection to any given voltage.

Line ending at the edge of the sheet indicates continuance on another sheet.


Male pin or card edge contact.


Female pin, socket or card edge connector.

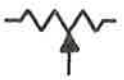

Coaxial connector.


No connection.

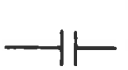

Connection.


Resistor, 1/4 W, ±5%, value in ohms (unless specified otherwise).

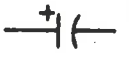
Resistor, 1/4W, ±1%, value in ohms (unless specified otherwise).


Resistor, variable, any type.


Resistor, variable, any type.


Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).


Capacitor, variable. Values in Picofarads (unless specified otherwise).


Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).


Diode, signal or rectifier.


Diode, zener.

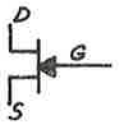

Diode, tunnel.


Diode, snap.

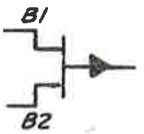

Light emitting diode (LED).

NPN Transistor.

PNP Transistor.



Field effect transistor, P Channel.



Field effect transistor, N.


Air choke.


Ferrite bead.


Ferrite core choke, Z 500 ohms when f ≥ 60 MHz (unless otherwise indicated).


Ferrite core choke, 40 uH, (unless otherwise indicated).

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STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL).

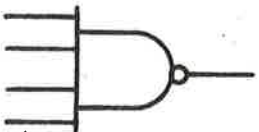
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

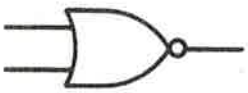
Supply voltages of IC's are shown in a table on each schematic.

2-Input Positive NAND Gate

2-Input Positive AND Gate

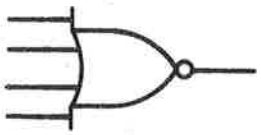


4-Input Positive NAND Gate

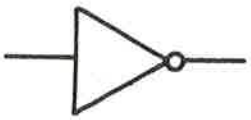


2- Input Positive NOR Gate

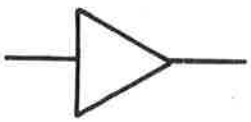
2 -Input Positive OR Gate



4-Input Positive NOR Gate



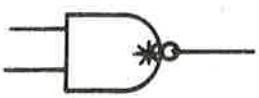
Inverter or Inverting Buffer



Non-Inverting Buffer

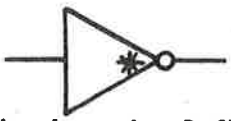
Exclusive OR Gate

Open collector outputs are identified by an asterisk (*) on the output connection.



2-Input Positive NAND Gate W/Open Collector

2-Input Positive OR Gate W/Open Collector



Non Inverting Buffer W/Open Collector

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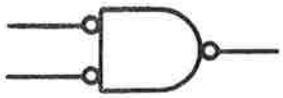
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS
EMITTER - COUPLED LOGIC (ECL)

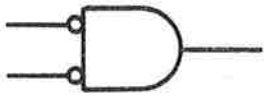
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

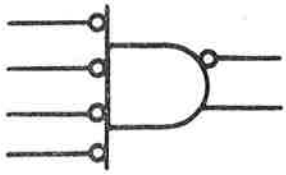
Supply voltages of IC's are shown in a table on each schematic.



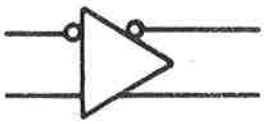
2 - Input Gate.
Negative AND (Positive OR) Gate.



2 - Input Gate.
Negative NAND (Positive NOR) Gate.

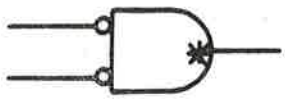


4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.

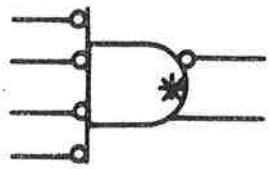


Differential
Amplifier.

Open emitter outputs are identified by an asterisk (*) on the output connection.



2 - Input Negative NAND Gate.
With Open Emitter.



A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.

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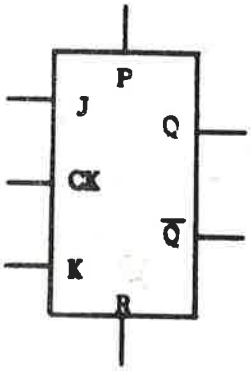
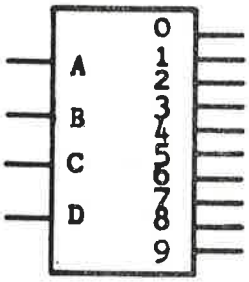
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL) OR EMITTER COUPLED LOGIC (ECL).

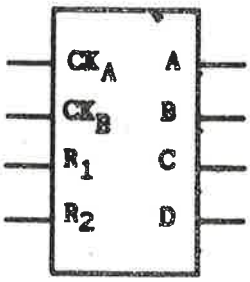
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave Flip-Flop



BCD-To-Decimal Decoder-Driver



Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.

Bottom View