IPNL

NOTICE POUR

COMPTEURS D'IMPULSIONS L 1020

MULTI-SCALER

JPV
LAUSANNE, le
11 fevrier 82

C O M P T E U R D ' I M P U L S I O N S L 1020

(M U L T I - S C A L E R)

Brève description: 3 compteurs 120 MHz et 1 compteur à présélection 5 MHz, avec affichages individuels et base de temps, dans un boîtier NIM.

Spécifications:

- Entrées/sorties: niveaux NIM rapides et connecteurs LEMO.
- Compteurs (3 compteurs de 9 décades chacun):

  vitesse de comptage $\geqslant$ 100 MHz;

  durée des impulsions d'attaque (garantie) $\geqslant$ 5 ns;

  dépassement de capacité indiqué par l'allumage d'un point lumineux à gauche de l'affichage du compteur correspondant et l'allumage des zéros non significatifs.

- Compteur à présélection (7 décades):

  vitesse de comptage $\begin{cases} \geqslant 10 \text{ MHz} & \underline{\text{sans}} \text{ présélection;} \\ \geqslant 5 \text{ MHz} & \underline{\text{avec}} \text{ présélection;} \end{cases}$

  durée des impulsions d'attaque (garantie) en mode COUNT $\geqslant$ 5 ns;

  utilisable avec base de temps interne 10 Hz (mode TIME);

  présélection en temps ($1/10$ seconde) ou en impulsions, de la forme $n \cdot 10^r$ (n=0 à 9, r=1 à 6), notée nEr (de 1E1 à 9E6);

  alarme acoustique en fin de comptage (interruptible par commutateur DT ou supprimable par interrupteur interne).

- Affichages:

  1 affichage par compteur, numérique, décimal; diodes électro-luminescentes rouges, 7 segments, hauteur des chiffres 3,8 mm;

  normalement, extinction des zéros non significatifs.

- Contrôle Arrêt/Marche/RAZ (START/STOP/SET-RESET):

  manuel en mode MASTER;

  compteurs utilisables en batterie en mode SLAVE commandés par 1 MASTER.

- Entrée PORTE (GATE) à haute impédance (HI-Z) agissant sur les entrées des 4 compteurs; normalement ouverte.
- Test des affichages (8 partout) et des compteurs sur base de temps interne (ne s'applique qu'aux compteurs 1, 2 et 3).
- Mécanique: boîtier NIM 3/12
- Alimentations: +6V/1,2A; -6V/o,4A;+12V/60mA;-12V/10mA;-24V/1mA; total 11W.

JFL 30.IX.81

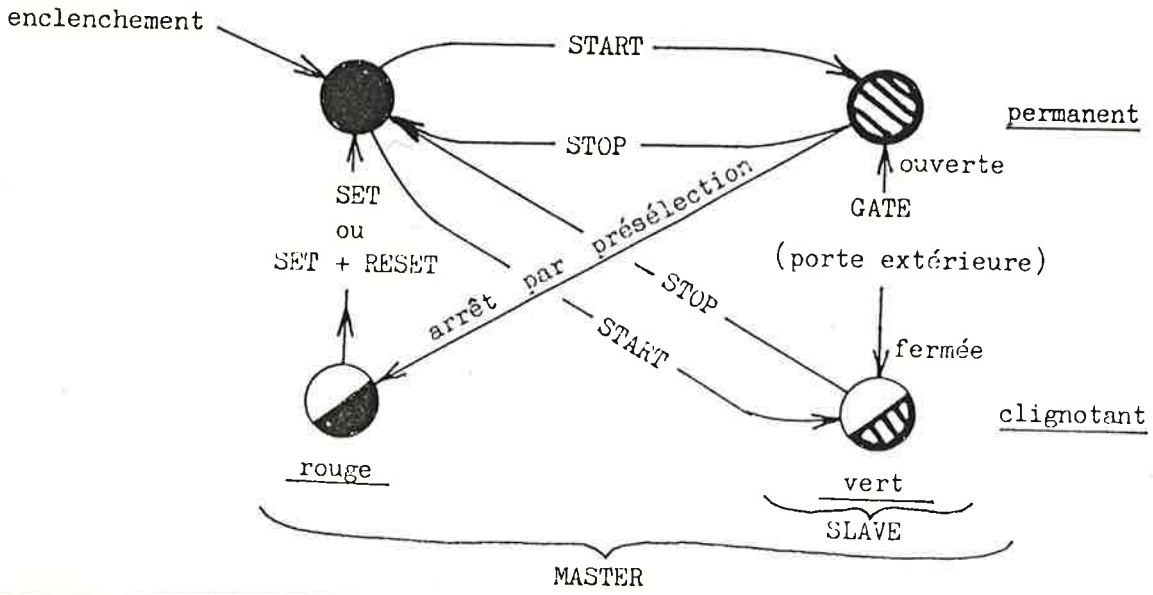
Utilisation:

- Entrées COUNTER, RESET: impédance 50Ω; admettent des impulsions négatives d'amplitude supérieure à 0,6 V.
- Entrée GATE: 2 connecteurs en parallèle pour permettre le chaînage; impédance 10 kΩ vers -5V; sans connexion extérieure, porte ouverte; une terminaison de 50Ω sur une des 2 entrées bloque la porte; en cas d'utilisation, chaîner les entrées et terminer la chaîne sur 50Ω ; un niveau NIM rapide (-0,6 V ou plus bas) est alors nécessaire pour ouvrir la porte.
- Sorties GATE, RESET, 1 MHz, 10 Hz: niveaux NIM rapides (16 mA correspondant à -0,8 V dans une terminaison de 50Ω).
- Remise à zéro et présélection automatiques à l'enclenchement (mise sous tension).
- Commutateur TIME/COUNT (2 positions avec blocage): commute l'entrée du compteur à présélection soit sur la base de temps interne 10 Hz (mode TIME) soit sur l'entrée extérieure Pr (mode COUNT).
- Commutateur SLAVE/SET (2 positions fixes et 1 position inférieure temporaire) et commutateur DT/RESET (2 positions temporaires et 1 position médiane fixe):

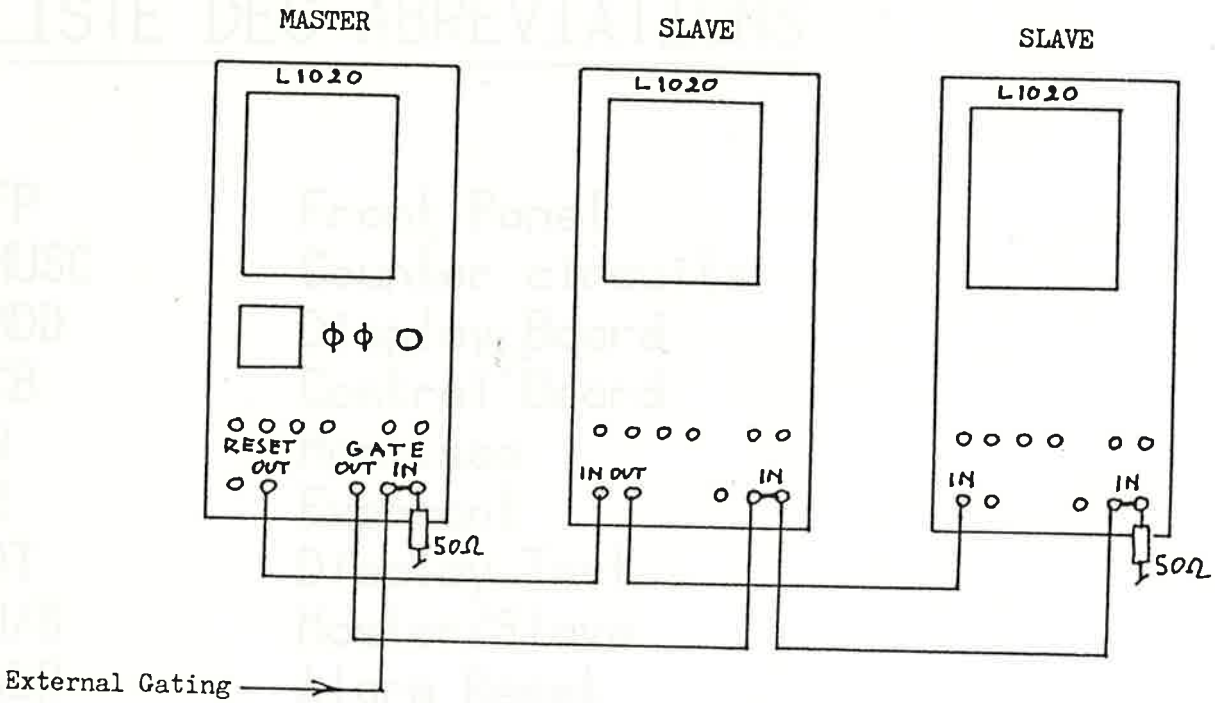
  position SLAVE: poussoir START/STOP inactif;
  SET et RESET manuels impossibles;
  présélection inactive;
  test des affichages (DT) possible;
  fonctionnement dépendant d'un tiroir MASTER par l'intermédiaire des entrées GATE et RESET;
  voyant du poussoir START/STOP alternant entre le vert permanent et le vert clignotant.

  position MASTER: poussoir START/STOP actif;
  nombre présélectionné chargé par SET simultanément ou non avec la mise à zéro par RESET des compteurs 1 à 3; SET et RESET sont retardés d'environ 1 seconde et sont inactivés pendant le comptage (voyant START/STOP à l'état vert);
  DT teste l'affichage sans perturber le contenu des compteurs et sert aussi à arrêter l'alarme acoustique de fin de comptage (présélection atteinte).

- Poussoir START/STOP (temporaire, avec voyant):
  inactif en mode SLAVE;
  en mode MASTER, détermine le début et la fin du comptage, tant que la présélection n'est pas atteinte.
- Voyant du poussoir START/STOP:



Câblage d'une batterie de compteurs:



START/STOP

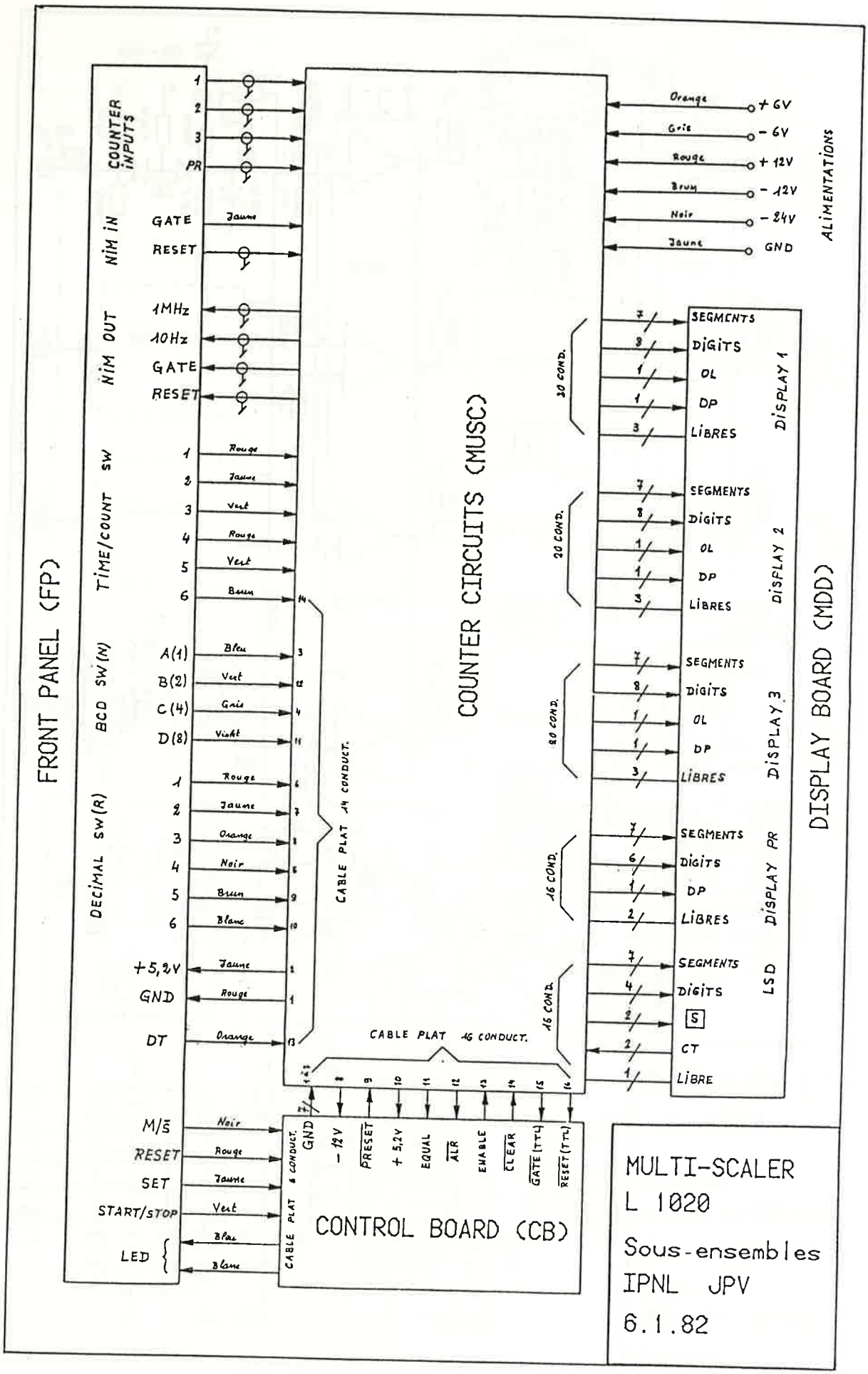
SET/RESET

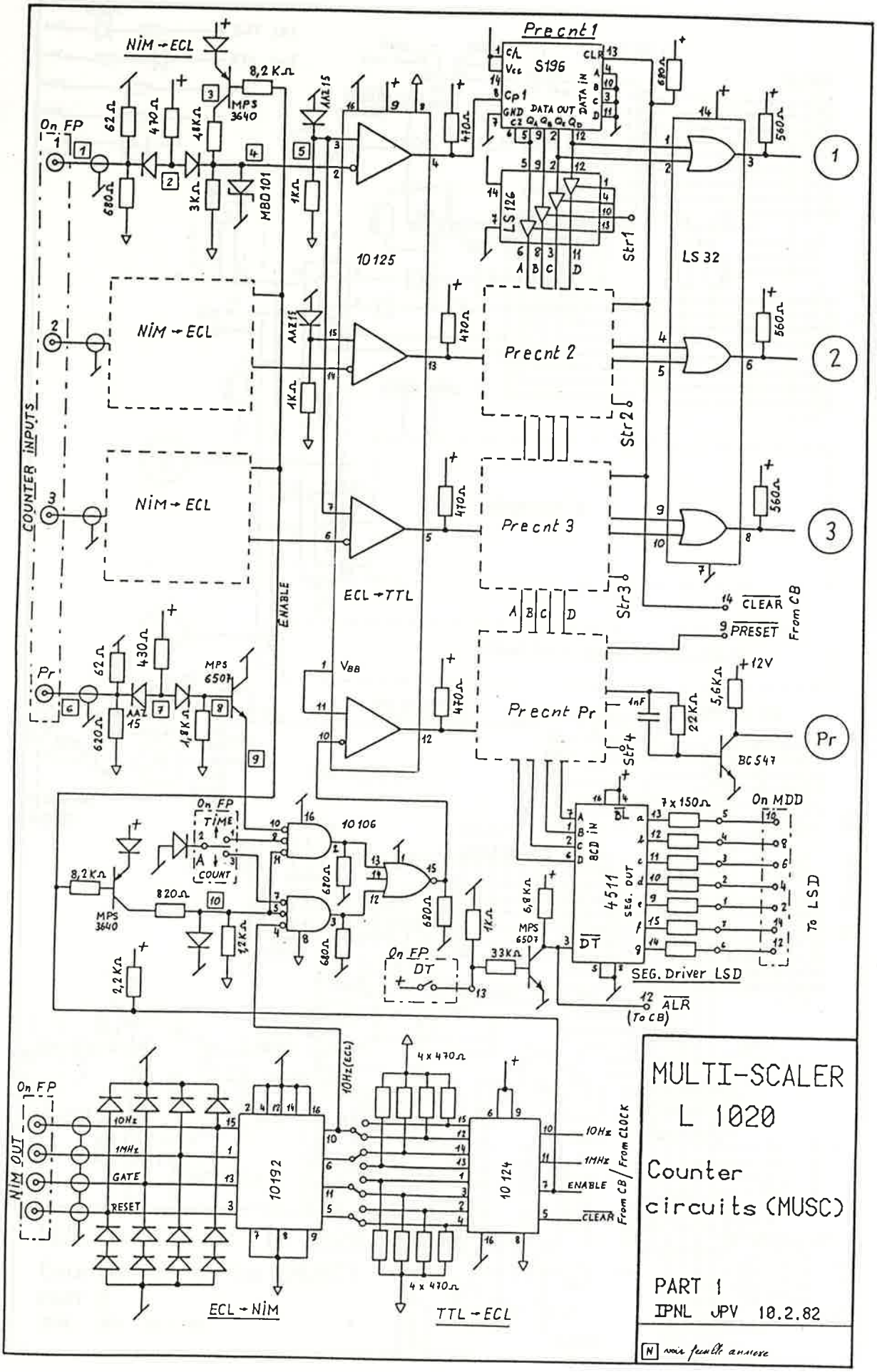
Présélection

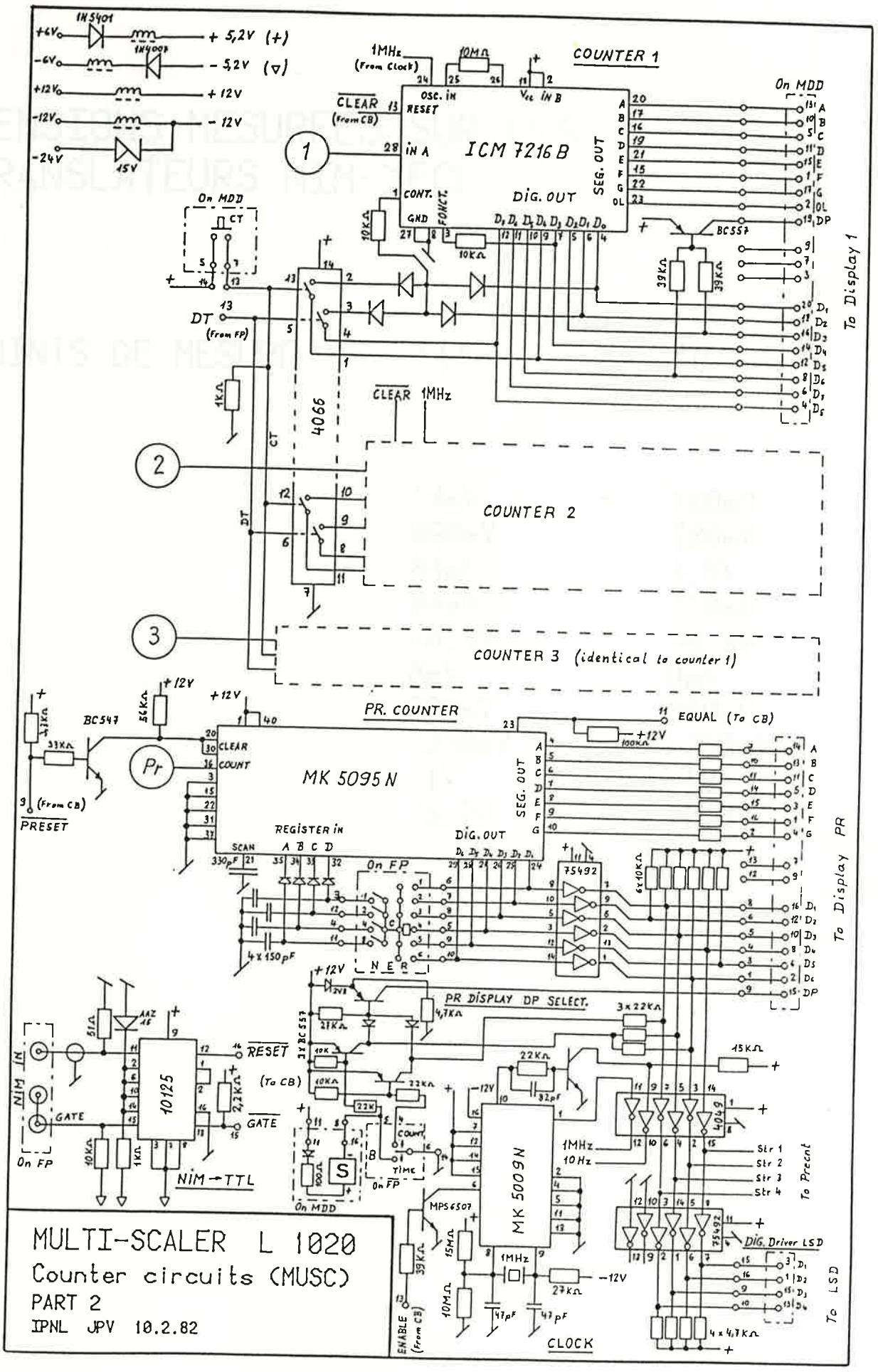
Alarme acoustique

LISTE DES ABREVIATIONS

FP	Front Panel
MUSC	Counter circuits
MDD	Display Board
CB	Control Board
N	Mantisse
R	Exposant
DT	Display Test
M/S	Master/Slave
ALR	Alarm Reset
OL	Over Load (over flow)
DP	Decimal Point
CT	Counter Test
LSD	Least Significant Digit
Precnt	Pre-Counter (S196+LS126)

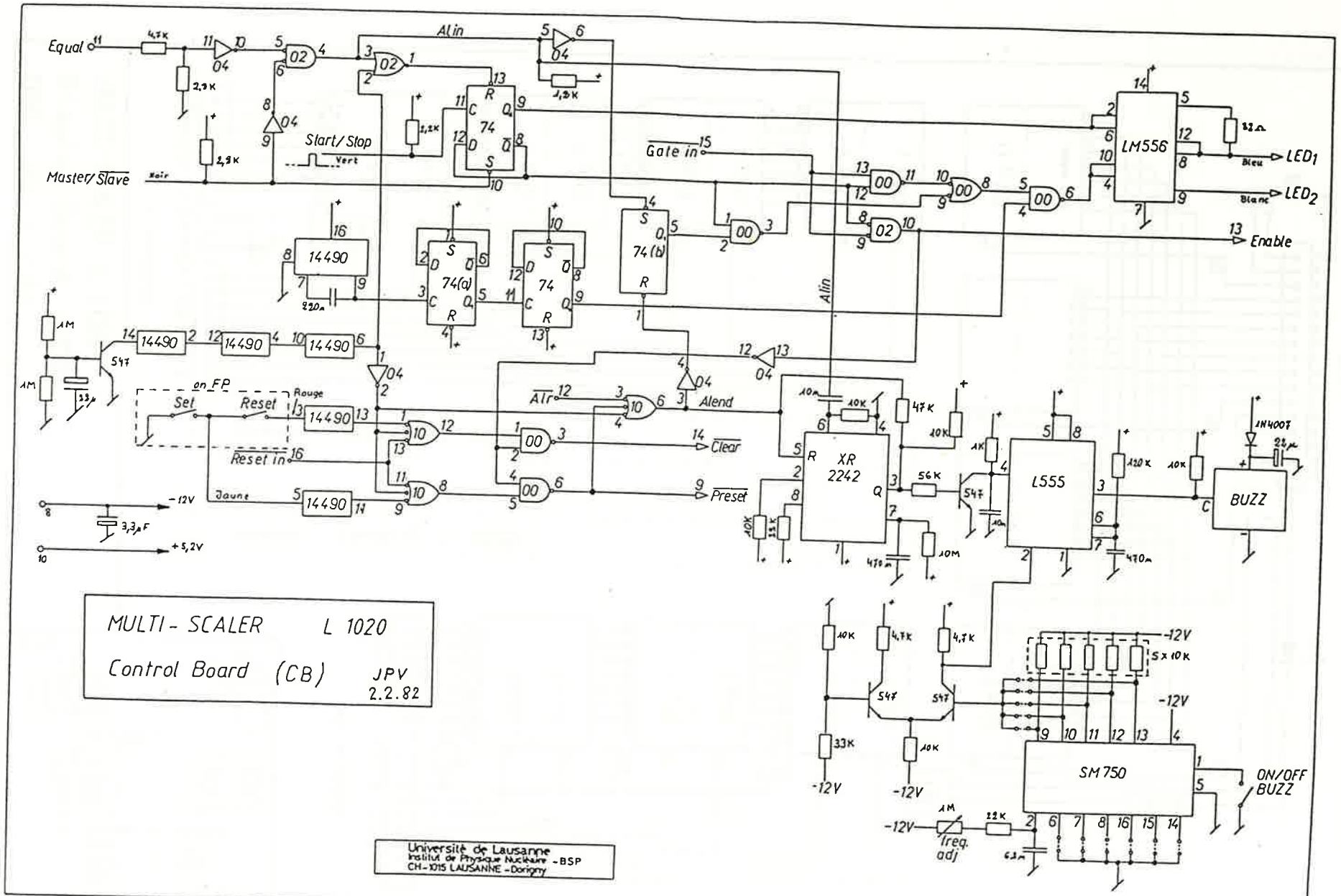

FRONT PANEL (FP)
COUNTER INPUTS
NIM IN
NIM OUT
TIME/COUNT SW
BCD SW(N)
DECIMAL SW(R)
1
2
3
PR
GATE
RESET
1MHz
10Hz
GATE
RESET
A(1)
B(2)
C(4)
D(8)
+5,2V
GND
DT
M/S
RESET
SET
START/STOP
LED
Jaune
Rouge
Vert
Bleu
Gris
Violet
Noir
Brun
Blanc
Orange
CABLE PLAT 14 CONDUCT.
CABLE PLAT 16 CONDUCT.
CABLE PLAT 6 CONDUCT.
COUNTER CIRCUITS (MUSC)
CONTROL BOARD (CB)
GND
-12V
PRESET
+5,2V
EQUAL
ALR
ENABLE
CLEAR
GATE (TTL)
RESET (TTL)
ALIMENTATIONS
Orange
+6V
Gris
-6V
Rouge
+12V
Brun
-12V
Noir
-24V
Jaune
GND
10 COND.
20 COND.
20 COND.
16 COND.
16 COND.
SEGMENTS
DIGITS
OL
DP
LIBRES
DISPLAY 1
DISPLAY 2
DISPLAY 3
DISPLAY PR
LSD
S
CT
LIBRE
DISPLAY BOARD (MDD)
MULTI-SCALER
L 1020
Sous-ensembles
IPNL JPV
6.1.82


NIM → ECL
8,2 KΩ
MPS 3640
On FP
62 Ω
470 Ω
48 KΩ
3 KΩ
MBD 101
680 Ω
AAZ 15
1 KΩ
10125
Precnt 1
S196
LS 126
Str1
LS 32
Precnt 2
Str2
Precnt 3
Str3
Precnt Pr
Str4
ECL → TTL
ENABLE
COUNTER INPUTS
CLEAR
PRESET
From CB
+12V
5,6 KΩ
22 KΩ
1nF
BC 547
Pr
On MDD
7 x 150 Ω
4511
BCD IN
SEG. OUT
SEG. Driver LSD
To LSD
ALR
(To CB)
On FP
TIME
COUNT
10106
820 Ω
1,2 KΩ
2,2 KΩ
6,8 KΩ
33 KΩ
DT
10Hz(ECL)
4 x 470 Ω
NIM OUT
10Hz
1MHz
GATE
RESET
10192
10124
ENABLE
CLEAR
From CB / From CLOCK
ECL → NIM
TTL → ECL
MULTI-SCALER
L 1020
Counter
circuits (MUSC)
PART 1
IPNL JPV 18.2.82
N voir feuille annexe

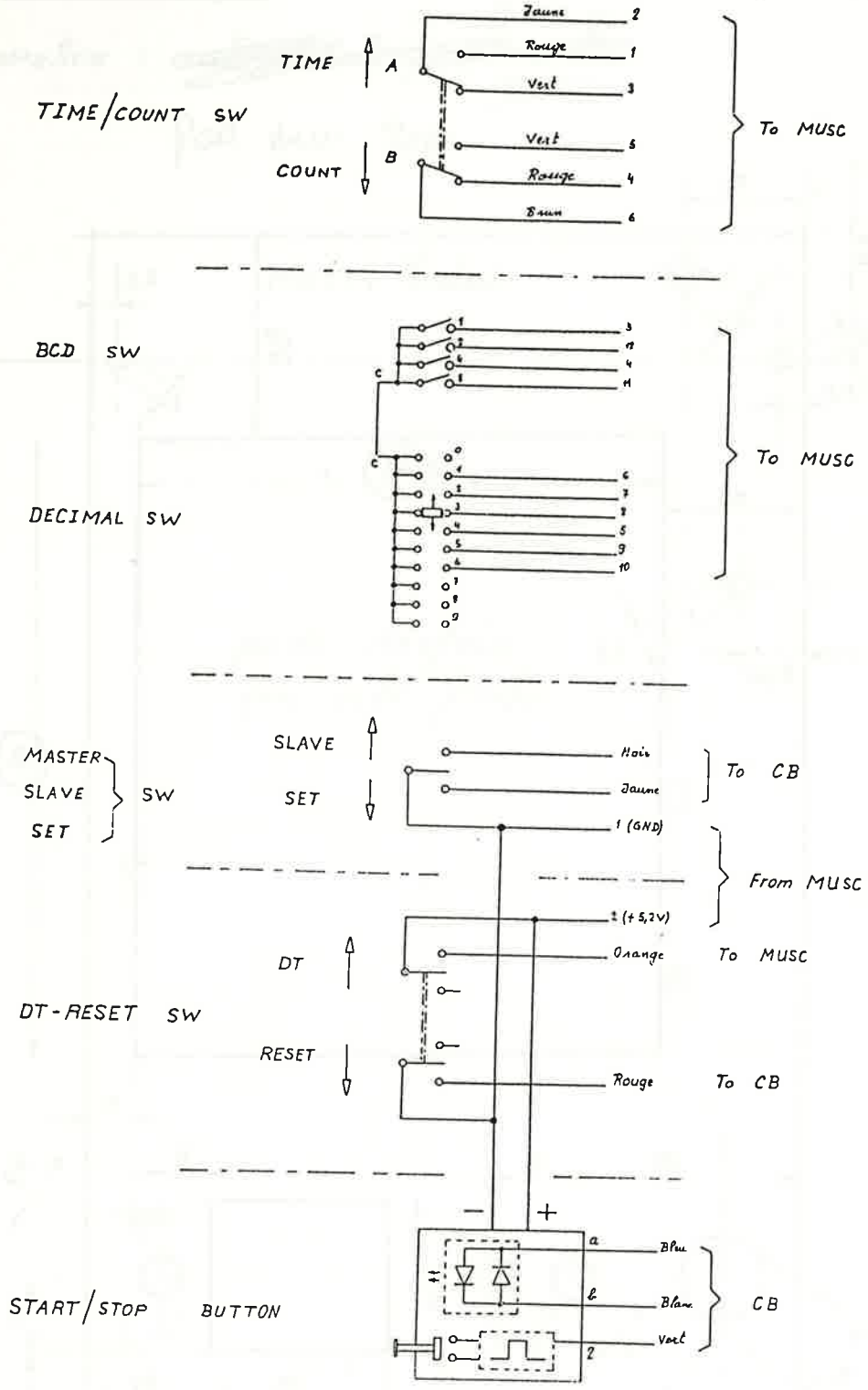

+ 5,2V (+)
- 5,2V (▽)
+ 12V
- 12V
1N5401
1N4002
15V
COUNTER 1
ICM 7216 B
OSC. in
RESET
IN A
IN B
CONT.
FONCT.
GND
SEG. OUT
DIG. OUT
On MDD
BC557
4066
CLEAR 1MHz
COUNTER 2
COUNTER 3 (identical to counter 1)
To Display 1
PR. COUNTER
MK 5095 N
EQUAL (To CB)
PRESET
REGISTER in
SCAN
On FP
75492
To Display PR
PR DISPLAY DP SELECT.
10125
NIM → TTL
RESET
GATE
MK 5009 N
MPS6507
1MHz
10Hz
To Precnt
Str 1
Str 2
Str 3
Str 4
Dig. Driver LSD
To LSD
ENABLE
CLOCK
MULTI-SCALER L 1020
Counter circuits (MUSC)
PART 2
IPNL JPV 10.2.82

TENSIONS MESUREES SUR LES TRANSLATEURS NIM->ECL

POINTS DE MESURE	ENABLE = "1"	"0"
1	14mV	100mV
2	690mV	780mV
3	84mV	4,5V
4	84mV	310mV
5	-0,3V	-0,3V
6	8mV	8mV
7	360mV	360mV
8	-250mV	-250mV
9	-1V	-1V
10	-5,2V	-0,3V


Equal
Alin
Start/Stop
Master/Slave
Gate in
LM556
LED1
LED2
Enable
14490
74(a)
74(b)
74
Alin
Alend
Clear
Preset
Set
Reset
Reset in
on FP
Rouge
Jaune
Bleu
Blanc
Noir
Vert
XR 2242
L555
BUZZ
1N4007
SM 750
ON/OFF BUZZ
Freq. adj
5 x 10K
-12V
+5,2V
MULTI - SCALER L 1020
Control Board (CB) JPV 2.2.82
Université de Lausanne
Institut de Physique Nucléaire - BSP
CH-1015 LAUSANNE - Dorigny

MULTI-SCALER L 1020
Display Board (MDD)
IPNL JPV 1.2.82



MULTI-SCALER L 1020

Front Panel (FP)

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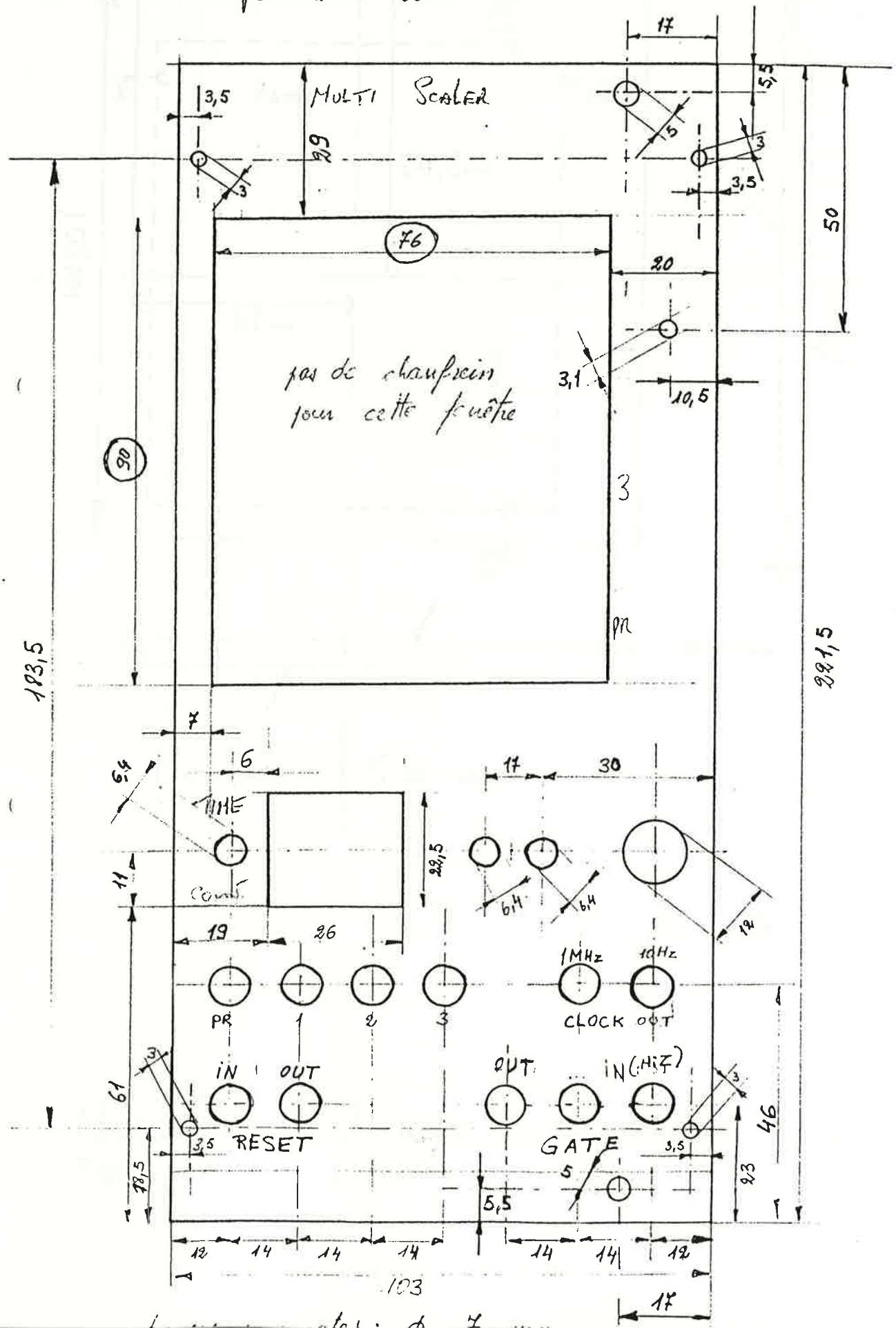
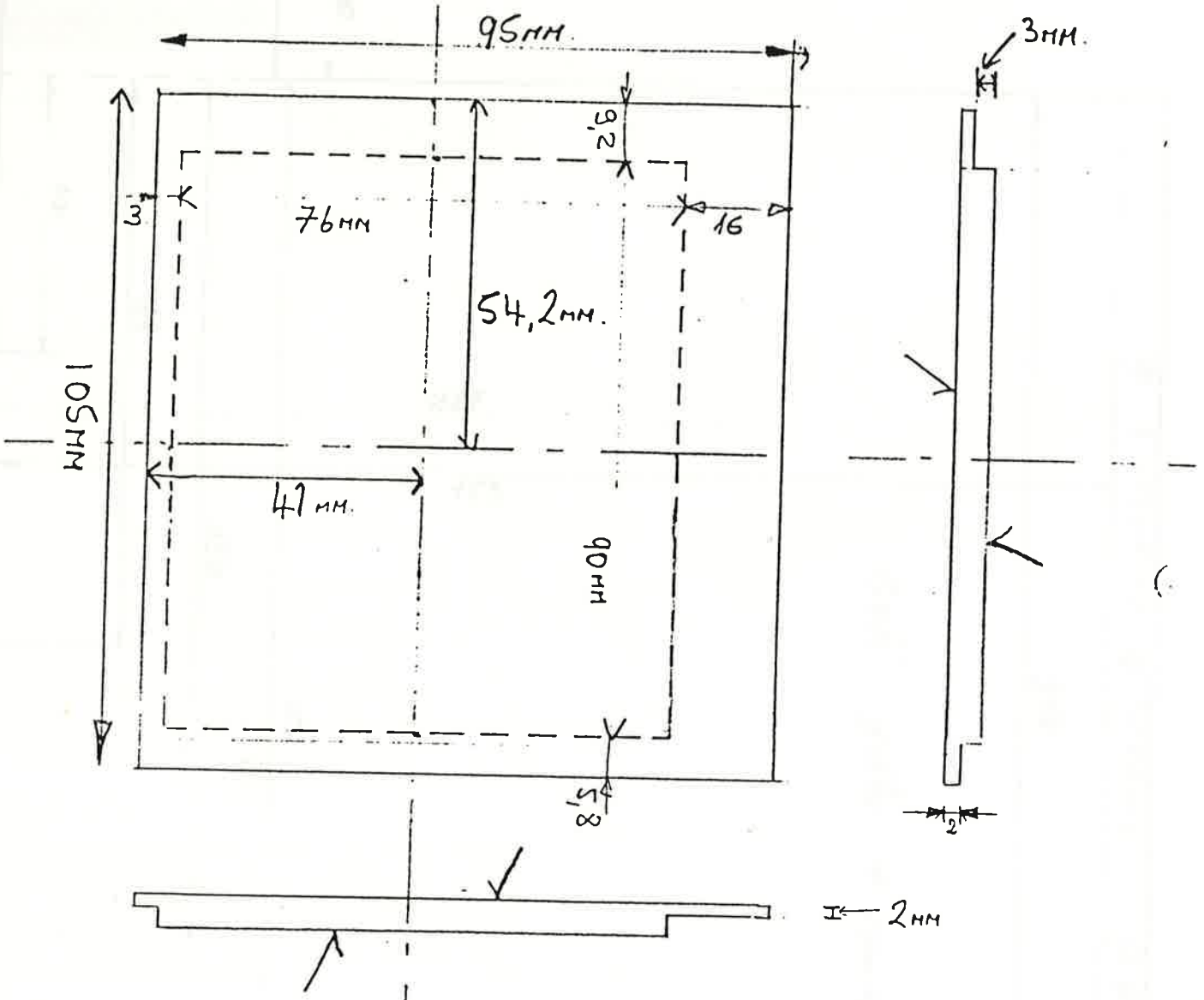
épaisseur : 3 mm

matière : ~~aluminium~~ ? ~~Tôle~~

Pour MLU 300





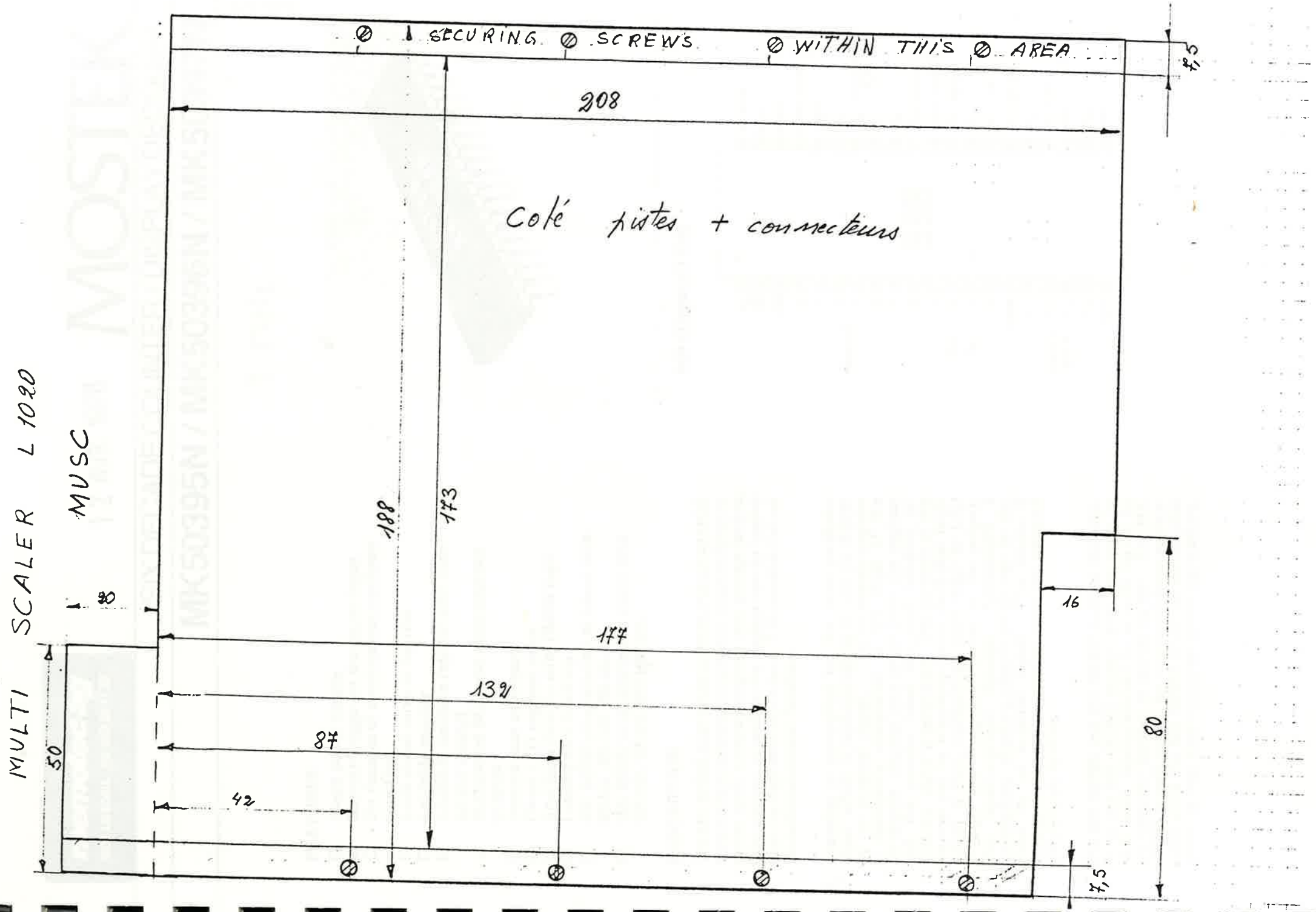
PLEXIGLASS. | 5 MM THICK

✓ = face jolie

MULTI SCALER | L 1020 | 17-10-80

SAM.

ouverture de la fenêtre : 76 x 90


SECURING SCREWS WITHIN THIS AREA
7,5
208
Coté pistes + connecteurs
188
173
30
177
139
87
42
50
16
80
7,5
MULTI SCALER L 1020
MUSC

MOSTEK

SIX DECADE COUNTER / DISPLAY DECODER

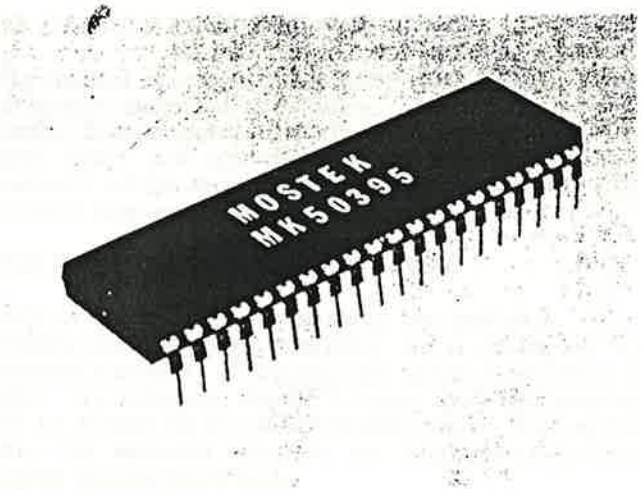
MK50395N / MK50396N / MK50397N

June 1976

1 MHz

FEATURES

- Single power supply
- Schmitt-Trigger on the count-input
- Six decades of synchronous up/down counting
- Look-ahead carry or borrow
- Loadable counter
- Loadable compare-register with comparator output
- Multiplexed BCD and seven-segment outputs
- Internal scan oscillator
- Direct LED segment drive
- Interfaces directly with CMOS logic
- Leading zero blanking
- MK 50396 programmed to count time: 99 hrs. 59 min. 59 sec.
- MK 50397 programmed to count time: 59 min. 59 sec. 99/100 sec.



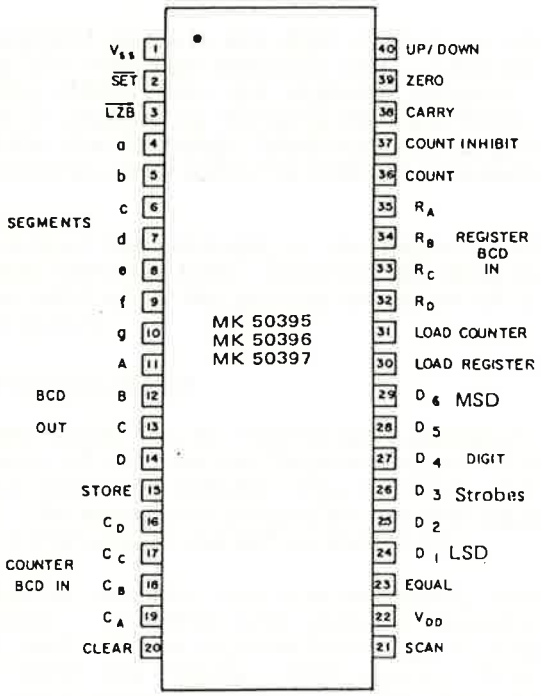
DESCRIPTION

The MK 50395 is an ion-implanted, P-channel MOS six-decade synchronous up/down-counter/display driver with compare-register and storage-latches. The counter as well as the register can be loaded digit-by-digit with BCD data. The counter has an asynchronous-clear function.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be driven by an external signal. The six-decade register is constantly compared to the state of the six-decade counter and when both the register and the counter have the same content, an EQUAL signal is generated. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD and 7-segment format to the output. The seven-segment decoder incorporates a leading-zero blanking circuit which can be disabled by an external signal. This device is intended to interface directly with the standard CMOS logic families.

The MK 50396 and MK 50397 operate identically to the MK 50395 except that two digits in each were reprogrammed to provide divide by six circuitry instead of divide by ten. The MK 50396 is well suited for industrial timer applications while the MK 50397 is best suited for stop watch or real time computer clock applications.

PIN CONNECTION



OPERATIONS:

SIX DECADE COUNTER, LATCH

The six decade counter is synchronously incremented or decremented on the positive edge of the count input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the count input.

The count inhibit can be changed in coincidence with the positive transition of the count input; the count input is inhibited when the count inhibit is high.

The counter will increment when up/down input is high (V_{SS}) and will decrement when up/down input is low. The up/down input can be changed .75 μs prior to the positive transition of the count input.

The clear input is asynchronous and will reset all decades to zero when brought high but does not affect the six digit latch or the scan counter.

As long as store input is low, data is continuously transferred from the counter to the display. Data in the counter will be latched and displayed when store input is high. Store can be changed in coincidence with the positive transition of the count input.

The counter is loaded digit by digit corresponding to the digit strobe outputs. BCD thumb wheel switches with four diodes per decade connected between the digit strobe outputs and the BCD inputs is one method to supply BCD data for loading the counter decades.

The load counter pulse must be at V_{SS} 2 microseconds prior to the positive transition of the digit strobe of the digit to be loaded. The load counter pulse may be removed after the positive transition of the digit strobe since the chip internally latches this signal. The BCD data to be loaded must be valid through the negative transition of the digit strobe.

INPUTS, OUTPUTS

The seven segment outputs are open drain capable of sourcing 10mA average current per segment over one digit cycle. Segments are on when at V_{SS}. The Carry, Equal, Zero, BCD and digit strobe outputs are push pull and are on when at V_{SS}. All inputs except Counter BCD, Register BCD, and SCAN inputs are high impedance CMOS compatible.

Three basic outputs originate from the counter: zero output, equal output, and carry output. Each output goes high on the positive (V_{SS}) going edge of the count input under the following conditions:

Zero output goes high for one count period when all decades contain zero. During a load counter operation the zero output is inhibited.

Equal output goes high for one count period when the contents of the counter and compare register are equal. The equal output is inhibited by a load counter or load register operation, which lasts until the next interdigit blanking period following a negative transition of Load Counter or Load Register.

*Carry occurs at 99 59 59 for the MK 50396 and 59 59 99 for the MK 50397

The carry output goes high with the leading edge of the count input at the count of 000000 when counting up or at 999999* when counting down and goes low with the negative going edge of the same count input.

A count frequency of 1 MHz can be achieved if the equal output, zero output and carry output are not used. These outputs do not respond at this frequency due to their output delay illustrated on the timing diagram.

SIX DECADE COMPARE REGISTER

The register is loaded identically to the load counter paragraph described previously. The register may be loaded independently of the counter, however, the clear input will not remove the register contents. Contents of the register are not displayed by the BCD or seven segment outputs.

BCD & SEVEN SEGMENT OUTPUTS

BCD or seven segment outputs are available. Digit strobes are decoded internally by a divide by six Johnson counter. This counter scans from MSD to LSD. By bringing the $\overline{SET}$ input low, this counter will be forced to the MSD decade count. During this time the segment outputs are blanked to protect against display burn out.

BCD outputs are valid for MSD when $\overline{SET}$ is low. Applying V_{SS} to $\overline{SET}$ allows normal scan to resume. Digit 6 output is active (V_{SS}) until the next scan clock pulse bring up digit 5 output.

The segment outputs and digit strobes are blanked during the interdigit blanking time. Leading zero blanking affects only the segment outputs. This option is disabled by bringing the $\overline{LZB}$ input high. Typically the interdigit blanking time is 5 to 25 microseconds when using the internal scan oscillator.

BCD output data changes at the beginning of interdigit blanking time. Therefore the BCD output data is valid when the positive transition of a digit output occurs.

SCAN OSCILLATOR

The MK 50395 has an internal scan oscillator. The frequency of the scan oscillator is determined by an external capacitor between V_{SS} or V_{DD} and scan input. The wave form present on the scan oscillator input is triangular in the self oscillate mode.

An external oscillator may also be used to drive the scan input. In either case, external capacitors of 150pF each will be required from V_{SS} to Counter BCD inputs and register BCD inputs. This will allow asynchronous loading of the BCD inputs.

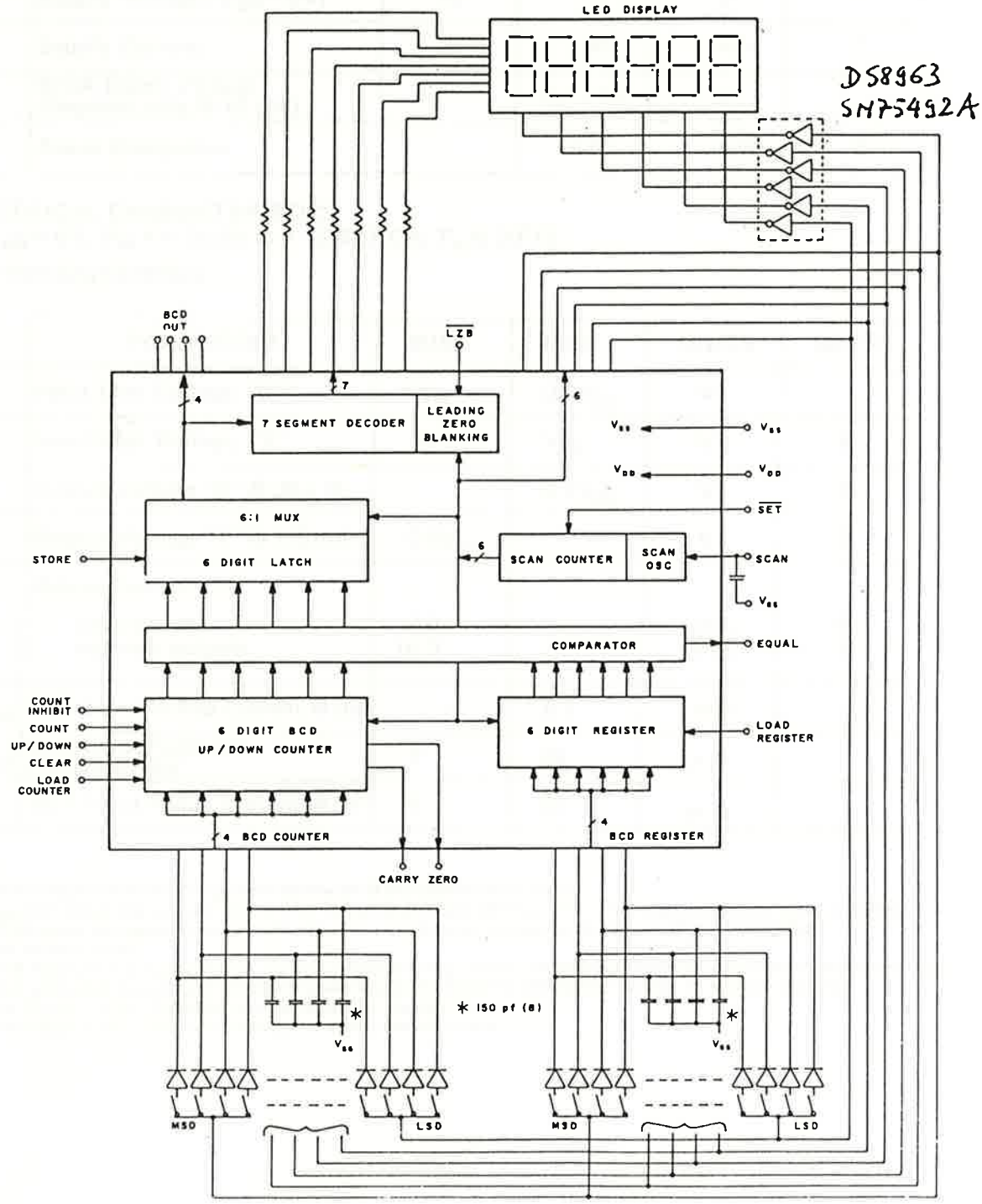
In the internal drive mode the interdigit blanking time will be the sum of the negative dwell period of the external oscillator and the normal self oscillate blanking time. (5 → 25 μsec). Display brightness can be controlled by the duty cycle of the external scan oscillator.

If external capacitors on the BCD inputs are undesirable, it will be necessary to synchronize the negative going edge of the load register and/or load counter command to coincide with the positive going edge of the scan input signal. Also the V_{SS} range should be limited from 10.8 to 13.2 volts.

Typically, the scan oscillator will oscillate at the following frequencies with these nominal capacitor valves from V_{SS} to scan input.

	Min	Max
820pF	1.4KHz	4.8 KHz
470pF	2.0KHz	6.8KHz
120pF	7.0KHz	20KHz

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} . . . . . +0.3V to −20V
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Storage Temperature Range (Ambient) . . . . . -40°C to +100°C

MAXIMUM OPERATING CONDITIONS

	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Operating Temperature	0	70	C	
V_{SS}	Supply Voltage (V_{DD} = 0V)	10	15	V	1
I_{SS}	Supply Current		30	mA	2
B_V	Break Down Voltage (Segment only @ 10 μA)		V_{SS} − 26	V	
P_D	Power Dissipation		670	mW	3

ELECTRICAL CHARACTERISTICS
(V_{DD} = 0V, V_{SS} = + 10.0V to + 15.0, 0°C ≤ T_A ≤ 70°C)

Static Operating Conditions

	PARAMETER	MIN	MAX	UNITS	NOTES
V_{IL}	Input Low Voltage, "0"	V_{DD}	$0.2V_{SS}$	V	
V_{IH}	Input High Voltage, "1"	V_{SS}−1	V_{SS}	V	4
V_{OL}	Output Voltage "0" @ 30μ A		$0.2V_{SS}$	V	5
V_{OH}	Output Voltage "1" @ 1.5 mA	$0.8V_{SS}$		V	5
I_{OH}	Output Current "1" digit strobes segment outputs	 3.0 10.0		 mA mA	 6 7
I_{SCAN}	Scan Input Pullup Current @ 0V		5.5	mA	
I_{SCAN}	Scan Input Pulldown Current @ 15V	2	40	μ A	
$I_{\overline{SET}}$	$\overline{SET}$ Input Pullup Current @ 0V	5	60	μ A	

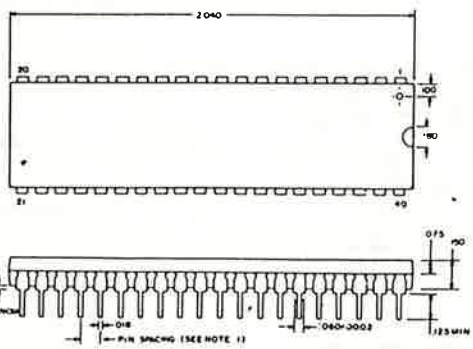
NOTES:
1. With 150 pF capacitor to V_{SS} from counter BCD and register BCD inputs.
2. I_{SS} with inputs and outputs open at 0°C. 28mA at 25°C and 25mA at 70°C. This does not include segment current. Total power per segment must be limited not to exceed power dissipation of package. (Θ_{JA} = 100 C/Watt)
3. All outputs loaded
4. MIN V_{IH} from R_A R_B R_C R_D C_A C_B C_C C_D inputs is V_{SS} −2.5V. Those inputs have internal pulldown reisitors to V_{DD}.
5. This applied to the push pull CMOS compatible outputs. Does not include digit strobes on segment outputs.
6. For V_{OUT} = V_{SS} −2.0 volts. Average value over one digit cycle.
7. For V_{OUT} = V_{SS} −3.0 volts. Average value over one digit cycle.

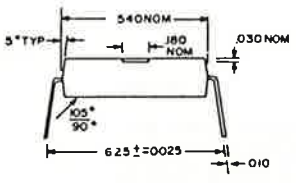
Dynamic Operating Conditions

	PARAMETER	MIN	MAX	UNITS	NOTES
f_{CI}	Count Input Frequency	0	1.00	MHz	8,9
f_{SI}	Scan Input Frequency	0	20	KHz	
t_{CPW}	Count Pulse Width	400		ns	10
t_{SPW}	Store Pulse Width	2.0		μs	
t_{SS}	Store Setup Time	0		μs	11
t_{CIS}	Count Inhibit Setup Time	0		μs	11
t_{UDS}	Up/Down Setup Time	-.75		μs	11
t_{CPW}	Clear Pulse Width	2.0		μs	11
t_{CS}	Clear Setup Time	- 0.5		μs	11
t_{OA}	Zero Access Time		3.0	μs	11
t_{OH}	Zero Hold Time		1.5	μs	11
t_{CA}	Carry Access Time		1.5	μs	11
t_{CH}	Carry Hold Time		0.9	μs	12
t_{EA}	Equal Access Time		2.0	μs	11
t_{EH}	Equal Hold Time		1.5	μs	11
t_L	Load Time	1/6 f_{SI}			

NOTES:
8. Measured at 50% duty cycle.
9. If carry, equal, or zero outputs are used, the count frequency will be limited by their respective output times.
10. The count pulse width must be greater than the carry access; time when using the carry output.
11. The positive edge of the count input is the t = 0 reference.
12. Measured from negative edge of count input.

PACKAGE DESCRIPTION 40-pin Dual In-Line Plastic

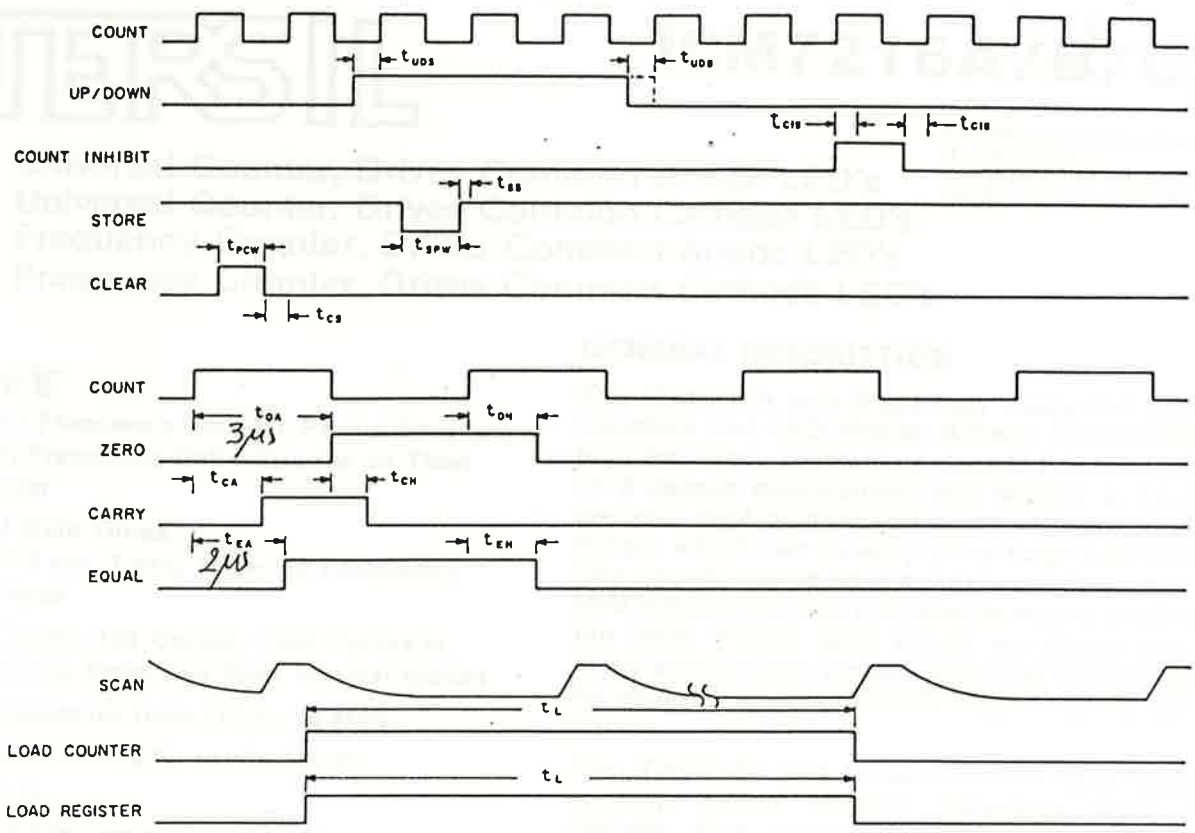




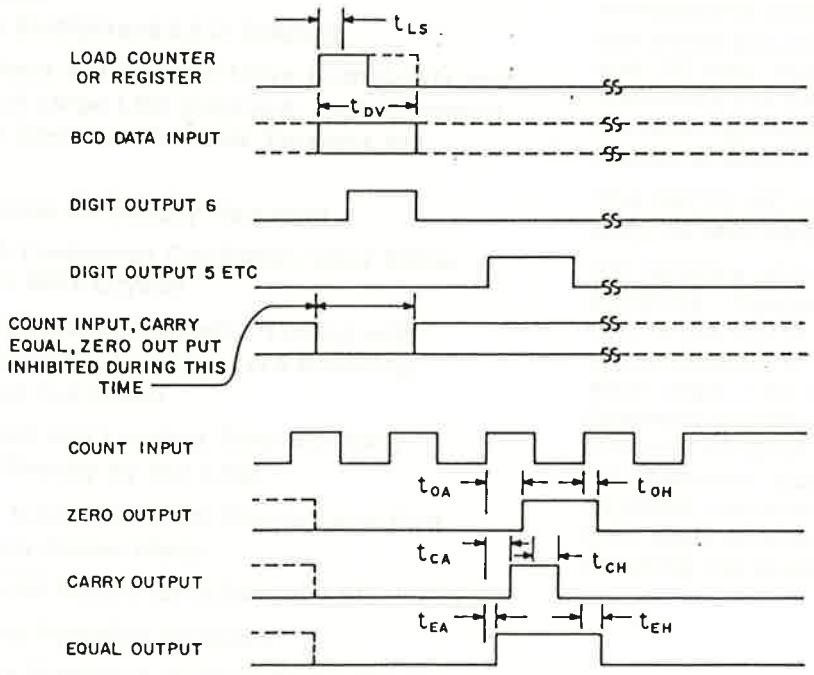
NOTE:

1. The true position pin spacing is 0.100 between center lines. Each pin centerline is located within± 0100 of its true longitudinal position relative to pins 1 and 40.

TIMING



LOADING COUNTER, REGISTER (1 DIGIT)



t_{LS} 2.0 μsec min NOTE: REF TO POSITIVE TRANSISTION OF DIGIT OUTPUT

t_{DV} 2.0 μsec min NOTE: REF TO NEGATIVE EDGE OF DIGIT OUTPUT

NOTE:

The inhibit function of the zero or equal outputs does not end when the Load Counter input goes to a "0" unless that transition occurs during interdigit blanking period at least 2.0 μsec prior to a positive transition of a digit output. This same timing restriction hold for Equal and Low Register.

MOSTEK

EUROPEAN MARKETING OFFICES

GERMANY

MOSTEK GMBH
TALSTRASSE 172
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TELEX 07 255 792

FRANCE

MOSTEK FRANCE S.A.R.L.
1, PLACE DES ETATS-UNIS
SILIC 217
F 94518 RUNGIS-CEDEX
01/686-0153
TELEX 204049

UNITED KINGDOM

MOSTEK UK LIMITED
MASONS HOUSE
1-3 VALLEY DRIVE
KINGSBURY ROAD
LONDON NW 9
TELEPHONE: 01-204 9322
TELEX: 25 940

ITALY

MOSTEK ITALIA S.P.A.
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TELEX 25 601

- 1 Dec. 1978

INTERSIL

ICM7216A/B/C/D

LASER- & Electronic-Equipment
A. Schürmann
Eierbrechtstr. 47, 8053 Zürich
Tel. 01 55 33 30, Telex 52124

ICM7216A Universal Counter, Drives Common Anode LED's
ICM7216B Universal Counter, Drives Common Cathode LED's
ICM7216C Frequency Counter, Drives Common Anode LED's
ICM7216D Frequency Counter, Drives Common Cathode LED's

FEATURES

ICM7216A AND B

- Functions as a Frequency Counter, Period Counter, Unit Counter, Frequency Ratio Counter or Time Interval Counter
- Four Internal Gate Times:
  0.01 sec, 0.1 sec, 1 sec, 10 sec in Frequency Counter Mode
- 1 Cycle, 10 Cycles, 100 Cycles, 1000 Cycles in Period, Frequency Ratio and Time Interval Modes
- Measures Frequencies from DC to 10 MHz
- Measures Period from 0.5μ sec to 10 sec

ICM7216C AND D

- Functions as a Frequency Counter. Measures Frequencies from DC to 10 MHz
- Decimal Point and Leading Zero Blanking May be Externally Selected

ALL VERSIONS:

- Eight Digit Multiplexed LED Outputs
- Output Drivers will Directly Drive Both Digits and Segments of Large LED Displays. Both Common Anode and Common Cathode Versions are Available
- Single Nominal 5V Supply Required
- Stable High Frequency Oscillator, Uses Either MHz or 10 MHz Crystal
- Internally Generated Multiplex Timing with Interdigit Blanking, Leading Zero Blanking and Overflow Indication
- Decimal Point and Leading Zero Blanking Controlled Directly by the Chip
- Display Off Mode Turns Off Display and Puts Chip into Low Power Mode
- Hold and $\overline{\text{Reset}}$ Inputs for Additional Flexibility
- Test Speedup Function Included
- All Terminals Protected Against Static Discharge

GENERAL DESCRIPTION

The ICM7216A and B are fully integrated Universal Counters and LED display drivers. They combine a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexers and 8 segment and 8 digit drivers which can directly drive large LED displays. The counter inputs have a maximum frequency of 10 MHz in frequency and unit counter modes and 2 MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7216A and B can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10 MHz or 1 MHz quartz crystal timebase. An external timebase input is also provided. For period and time interval, the 10MHz timebase gives a 0.1 μsec resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation time of 0.01 sec, 0.1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to an accuracy of 0.1 Hz in the least significant digit. There is 0.2 seconds between measurements in all ranges.

The IMC7216C and D function as frequency counters only, as described above.

All versions of the ICM7216 incorporate leading zero blanking. Frequency is displayed in KHz. In the ICM7216A and B, time is displayed in μsec. The display is multiplexed at 500Hz with a 12.5% duty cycle for each digit. The ICM7216A and C are designed for common anode display with typical peak segment currents of 25mA. The ICM7216B and D are designed for common cathode displays with typical peak segment currents of 12mA. In the display off mode, both digit drivers and segment drivers are turned off enabling the display to be used for other functions.

Preliminary ICM7216A/B/C/D Low Power CMOS

ORDERING INFORMATION

Universal Counter for use with Common Anode LED Display:	ICM 7216 A	IJI
Universal Counter for use with Common Cathode LED Display:	ICM 7216 B	IPI
Frequency Counter for use with Common Anode LED Display:	ICM 7216 C	IJI
Frequency Counter for use with Common Cathode LED Display:	ICM 7216 D	IPI

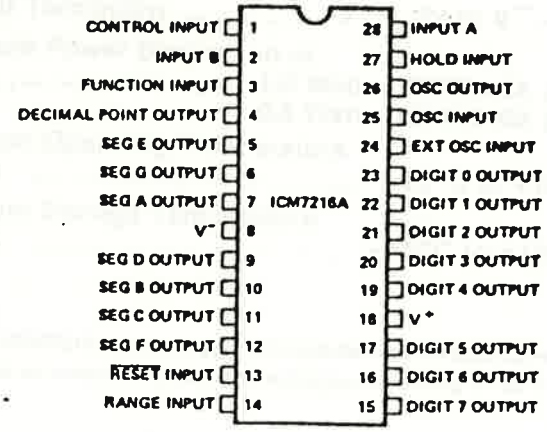
Type — Package (See Outline Drawing) — Temperature Range -20°C to +70°C

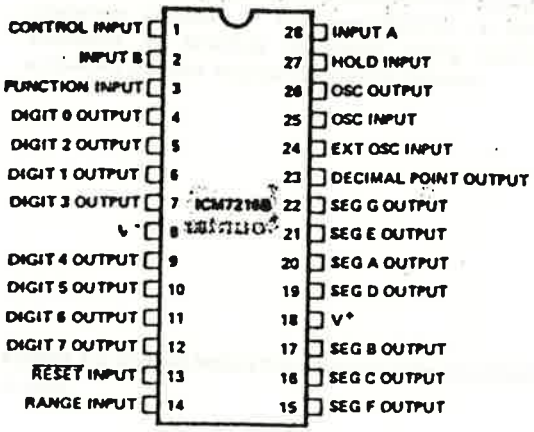
Evaluation Kit:
ICM7226 EV/Kit

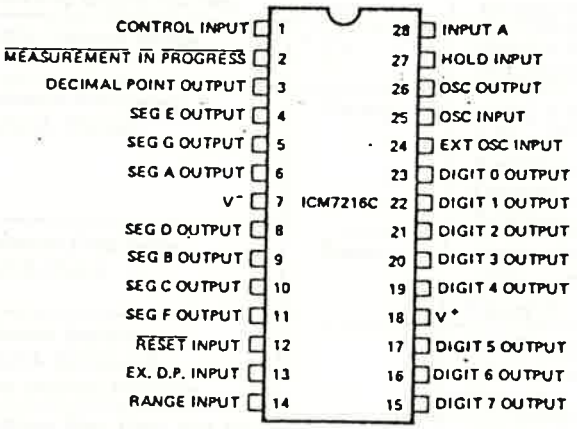
INTERSIL, INC., 10710 N. TANTAU AVE., CUPERTINO, CA 95014
(408) 996-5000 TWX: 910-338-0171

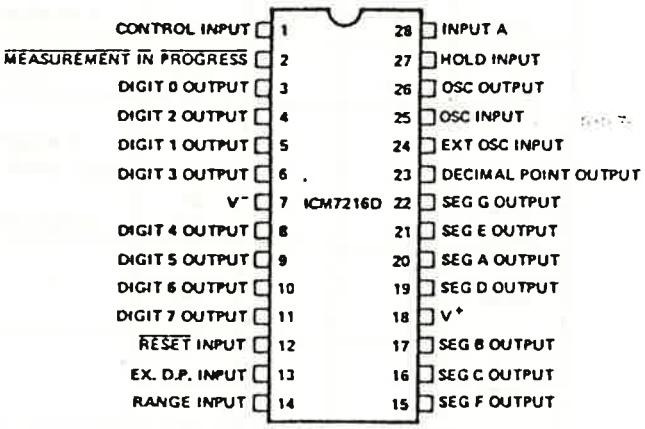
ICM7216

PIN CONFIGURATIONS









EVALUATION KIT

The ICM7226 Universal Counter System has all of the features of the ICM7216 plus a number of additional features. The ICM7226 Evaluation Kit consists of the ICM7226AIDL (Common Anode LED Display), a 10 MHz quartz crystal, 8 each 7 segment .3" LED's, P.C. board, resistors, capacitors, diodes, switches, socket: everything needed to quickly assemble a functioning ICM7226 Universal Counter System.

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage ($V^+ - V^-$) ..... 6.5 Volts
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
Voltage On Any Input or
Output Terminal[1] ..... $V^+ + .3V$ to $V^- - .3V$
Maximum Power Dissipation at
70°C ..... 1.0 Watts (ICM7216A & C)
0.5 Watts (ICM7216B & D)
Maximum Operating Temperature
Range ..... −20°C to +70°C
Maximum Storage Temperature
Range ..... −55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

Notes:
1. The ICM7216 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V^+ to V^- by more than 0.3 volts.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ - V^- = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
ICM7216A/B						
Operating Supply Current	I_{DD}	Display Off, Unused Inputs to V^-		2	5	mA
Supply Voltage Range		-20°C < T_A < +70°C, Input A, Input B Frequency at F_{MAX}	4.75		6.0	Volts
Maximum Frequency Input A, Pin 28	$F_{A\,MAX}$	-20°C < T_A < +70°C 4.75 < $V^+ - V^-$ < 6.0V, Figure 1, Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	10 2.5			MHz MHz
Maximum Frequency Input B, Pin 2	F_{BMAX}	-20°C < T_A < +70°C 4.75V < V^+ ≤ 6.0V Figure 2	2.5			MHz
Minimum Separation Input A to Input B Time Interval Function		-20°C < T_A < 70°C 4.75V < V_T < 6.0V Figure 3	250			nsec
Maximum Osc. Freq. and Ext. Osc. Frequency		-20°C < T_A < +70°C 4.75 < $V^+ - V^-$ < 6.0V	10			MHz
Minimum Ext. Osc. Freq.					100	KHz
Oscillator Transconductance	gm	$V^+ - V^- = 4.75V$, $T_A = +70°C$	400			μs
Multiplex Frequency	f_{mux}	f_{osc} = 10MHz		500		Hz
Time Between Measurements		f_{osc} = 10MHz		200		msec
Input Voltages: Pins 2,13,25,27,28 Input Low Voltage Input High Voltage	 V_{IL} V_{IH}	-20°C < T_A < +70°C	 3.5		1.0	 Volts Volts
Input Resistance to V^+ Pins 13,24	R		100K	400K		ohms
Input Leakage Pin 27	I_L				10	μA

INTERSIL

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
ICM7216A						
Digit Driver:						
Pins 15,16,17,19,20,21,22,23						
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.0V$	-170	-200		mA
Low Output Current	I_{OL}	$V_{OUT} = 1.0V$		-0.3		mA
Segment Driver:						
Pins 4,5,6,7,9,10,11,12						
Low Output Current	I_{OL}	$V_{OUT} = V^- + 1.5V$	25	35		mA
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.5V$		100		μA
Multiplex Inputs:						
Pins 1,3,14						
Input Low Voltage	V_{IL}				0.8	Volts
Input High Voltage	V_{IH}		$V^- + 2.0$			Volts
Input Resistance to V^-	R	$V_{IN} = V^- + 1.0V$	100	200		KΩ
ICM7216B						
Digit Driver:						
Pins 4,5,6,7,9,10,11,12						
Low Output Current	I_{OL}	$V_{OUT} = V^- + 1.0V$	50	75		mA
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.5V$		100		μA
Segment Driver:						
Pins 15,16,17,19,20,21,22,23						
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.0V$	10			mA
Leakage Current	I_L	$V_{OUT} = V^+ - 2.5V$			10	μA
Multiplex Inputs:						
Pins 1,3,14						
Input Low Voltage	V_{IL}				$V^+ - 2.0$	Volts
Input High Voltage	V_{IH}		$V^+ - 0.8$			Volts
Input Resistance to V^+	R	$V^+ - 1.0V$	200	360		KΩ

TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $V^+ - V^- = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
ICM7216C/D						
Operating Supply Current	I_{DD}	Display Off, Unused Inputs to V^-		2	5	mA
Supply Voltage Range		$-20°C < T_A < +70°C$, Input A Frequency at F_{MAX}	4.75		6.0	Volts
Maximum Frequency Input A, Pin 28	F_{MAX}	$-20°C < T_A < +70°C$ $4.75 < V^+ - V^- < 6.0V$, Figure 1	10			MHz
Maximum Osc. Freq and Ext. Osc. Frequency		$-20°C < T_A < +70°C$ $4.75 < V^+ - V^- < 6.0V$	10			MHz
Minimum Ext. Osc. Freq.					100	KHz
Oscillator Transconductance	gm	$V^+ - V^- = 4.75V$, $T_A = +70°C$	400			μmhos
Multiplex Frequency	f_{mux}	$f_{osc} = 10MHz$		500		Hz
ne Between Measurements		$f_{osc} = 10MHz$		200		msec
Input Voltages:						
Pins 12,27,28						
Input Low Voltage	V_{IL}	$-20°C < T_A < +70°C$	3.5			Volts
Input High Voltage	V_{IH}				1.0	Volts
Input Resistance to V^+ Pins 12,24	R		100	400		KΩ
Input Leakage Pin 27	I_L				10	μA
Input Current Pin 2	I_{OL}	$V_{OL} = V^- + .4V$	0.36			mA
	I_{OH}	$V_{OH} = V^+ - .8V$	265			μA

TYPICAL OPERATING CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
ICM7216C						
Digit Driver: Pins 15,16,17,19,20,21,22,23						
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.0V$	-170	200		mA
Low Output Current	I_{OL}	$V_{OUT} = 1.0V$		-0.3		mA
Segment Driver: Pins 3,4,5,6,8,9,10,11						
Low Output Current	I_{OL}	$V_{OUT} = V^- + 1.5V$	25	30		mA
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.5V$		100		μA
Multiplex Inputs: Pins 1,13,14						
Input Low Voltage	V_{IL}				0.8	Volts
Input High Voltage	V_{IH}		$V^- + 2.0$			Volts
Input Resistance to V^-	R	$V_{IN} = V^- + 1.0V$	100	200		KΩ
ICM7216D						
Digit Driver: Pins 3,4,5,6,8,9,10,11						
Low Output Current	I_{OL}	$V_{OUT} = V^- + 2.0V$	50	75		mA
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.5V$		100		μA
Segment Driver: Pins 15,16,17,19,20,21,22,23						
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.0V$	10	15		μA
Leakage Current	I_L	$V_{OUT} = V^+ - 2.5V$			10	μA
Multiplex Inputs: Pins 1,13,14						
Input Low Voltage	V_{IL}				$V^+ - 2.0$	Volts
Input High Voltage	V_{IH}		$V^+ - 0.8$			Volts
Input Resistance to V^+		$V_m = V^+ - 1.0V$	200	360		kΩ

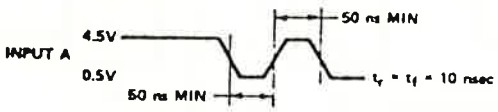


FIGURE 1. Waveform for Guaranteed Minimum FAMAX Function = Frequency, Frequency Ratio, Unit Counter.

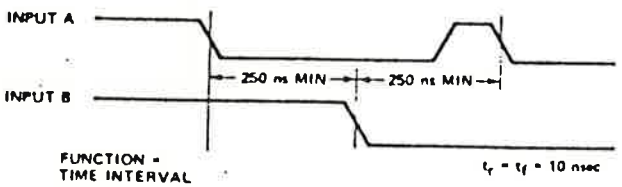


FIGURE 3. Waveform for Minimum Time Between Transitions of Input A and Input B.

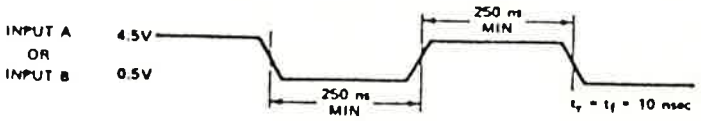
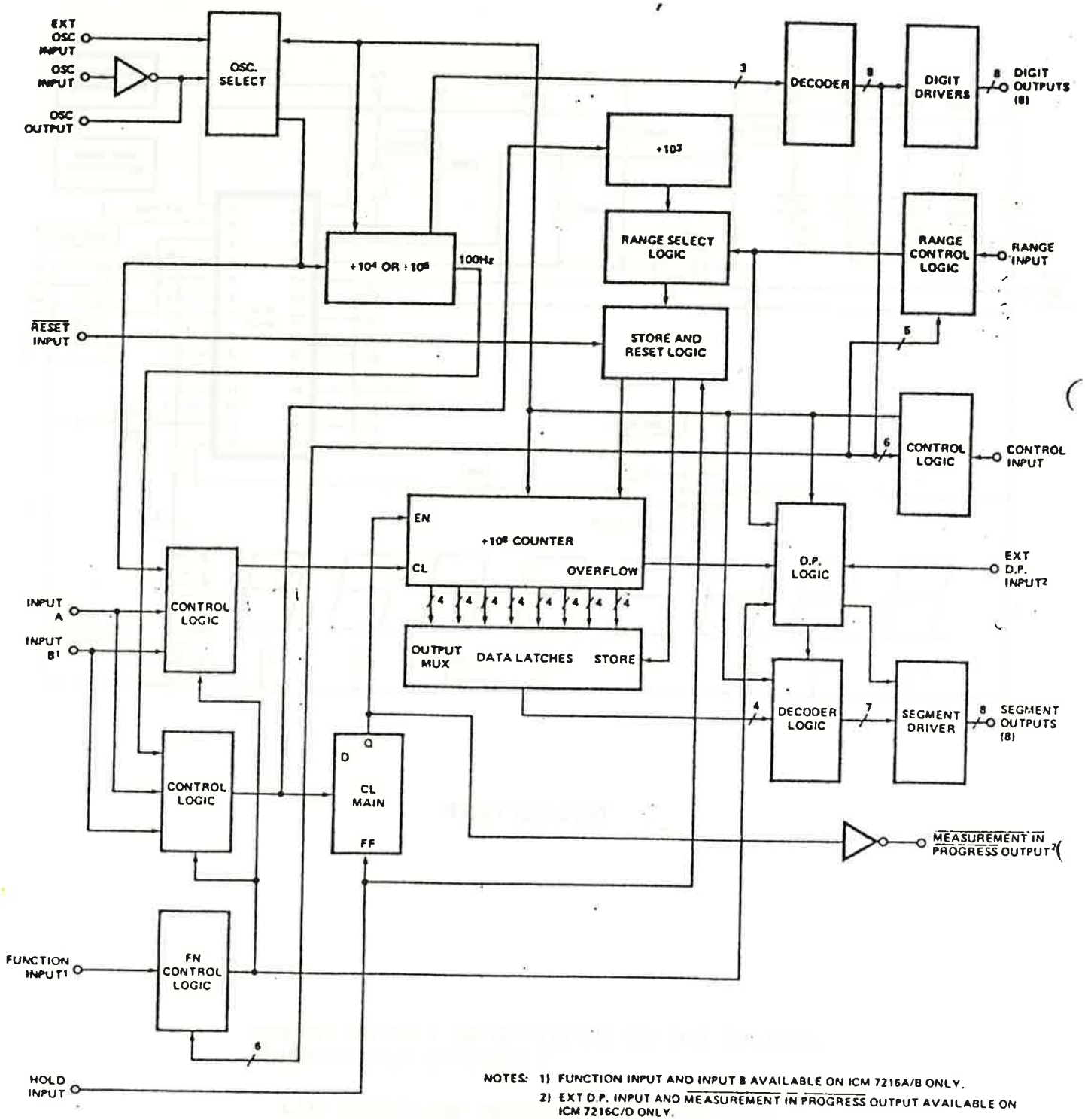


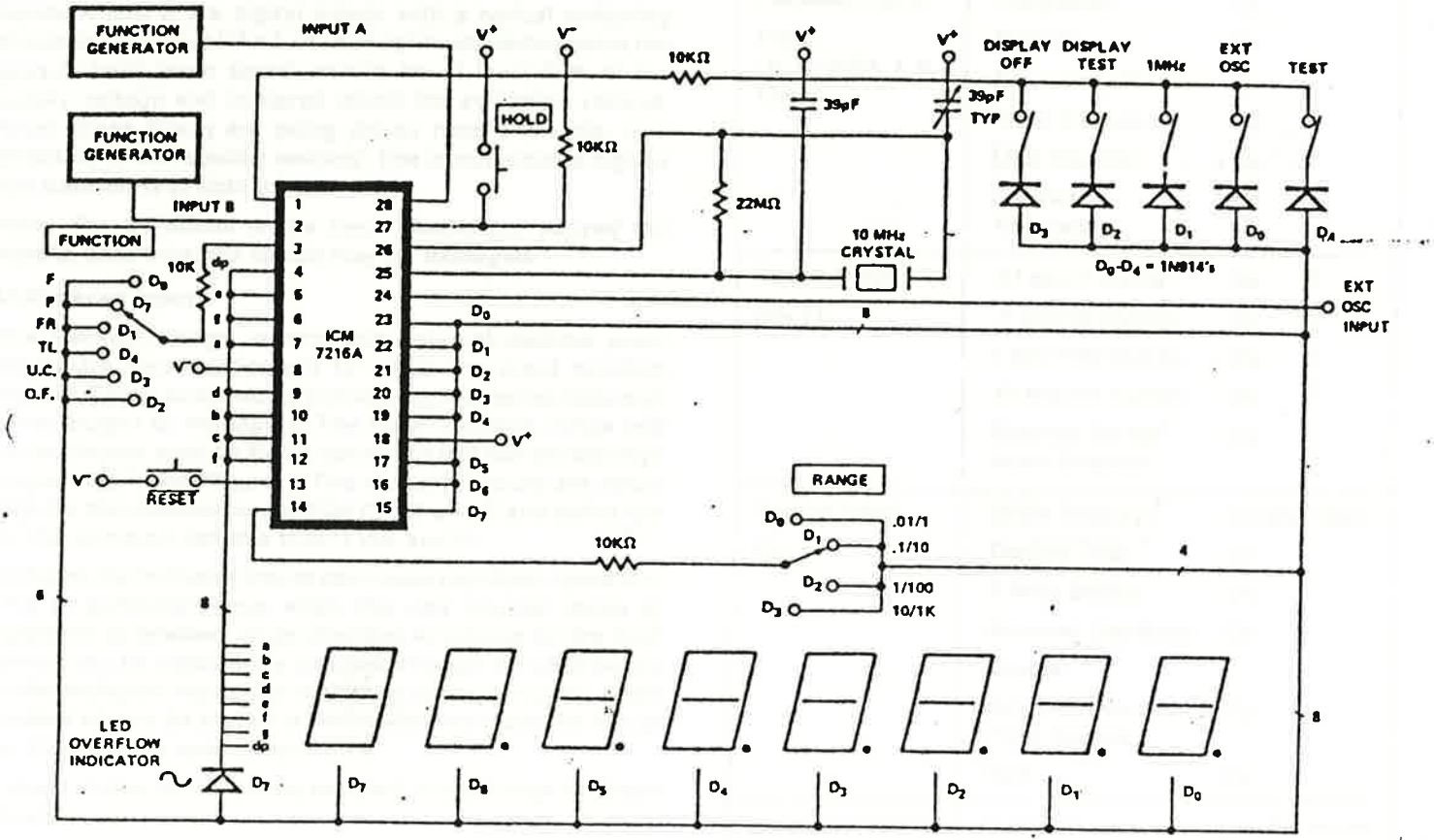
FIGURE 2. Waveform for Guaranteed Minimum FBMAX and FAMAX for Function = Period and Time Interval.

Channel A going negative starts the time interval counter. Channel B stops the counter. Channel A must then go negative after B goes negative to complete the measurement cycle. On repetitious signals, this occurs automatically. On "one-shot" time interval measurements, external provisions must be made to accommodate the above described procedure.



NOTES: 1) FUNCTION INPUT AND INPUT B AVAILABLE ON ICM 7216A/B ONLY.
2) EXT D.P. INPUT AND MEASUREMENT IN PROGRESS OUTPUT AVAILABLE ON ICM 7216C/D ONLY.

BLOCK DIAGRAM



TEST CIRCUIT

OVERFLOW WILL BE INDICATED ON THE DECIMAL POINT OUTPUT OF DIGIT 7.

LED OVERFLOW INDICATOR CONNECTIONS

	CATHODE	ANODE
ICM 7216A	DEC. PT.	D_7
ICM 7216B	D_7	DEC. PT.
ICM 7216C	DEC. PT.	D_7
ICM 7216D	D_7	DEC. PT.

APPLICATIONS NOTES

GENERAL

Inputs A and B

Inputs A and B are digital inputs with a typical switching threshold of 2.0V at $V^+ = 5.0V$. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from T²L logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

Multiplexed Inputs

The function, range, control and external decimal point inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125μsec). The multiplex inputs are active high for the common anode ICM7216A and C and active low for the common cathode ICM7216B and D.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the unit counter mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10K resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

Control Input Functions

a. Display Test — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Display Off is selected at the same time.

b. Display Off — To enable the Display Off mode it is necessary to input D_3 to the control input and have the HOLD input at V^+. The chip will remain in the Display Off mode until HOLD is switched back to V^-. While in the Display Off mode, the segment and digit driver outputs are open. During Display Off the oscillator continues to run with a typical supply current of 1.5mA with a 10 MHz crystal and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to V^-.

c. 1 MHz Select — The 1 MHz select mode allows use of a 1 MHz crystal with the same digit multiplex rate and time between measurements as with a 10 MHz crystal. The decimal point is also shifted one digit to the right in Period and Time Interval, since the least significant digit will be in μsecond increments rather than 0.1 μsec increments.

d. External Oscillator Enable — In this mode the external oscillator input is used instead of the on-chip oscillator for Timebase input and Main Counter input in Period and Time interval modes. The on-chip oscillator will continue to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100 KHz or the chip will reset itself to enable the on-chip oscillator.

TABLE 1

	FUNCTION	DIGIT
Function Input Pin 3 (ICM7216A & B Only)	Frequency	D_0
	Period	D_7
	Frequency Ratio	D_1
	Time Interval	D_4
	Unit Counter	D_3
	Oscillator Frequency	D_2
Range Input Pin 14	.01 sec/1 Cycle	D_0
	.1 sec/10 Cycles	D_1
	1 sec/100 Cycles	D_2
	10 sec/1K Cycles	D_3
	External Range Input Enabled	D_4
Control Input Pin 1	Blank Display	D_3 and Hold
	Display Test	D_7
	1 MHz Select	D_1
	External Oscillator Enable	D_0
	External Decimal Point Enable	D_2
	Test	D_4
External Decimal Point Input Pin 13, ICM7216C & D Only	Decimal point is output for same digit that is connected to this input	

e. External Decimal Point Enable — When external decimal point is enabled a decimal point will be displayed whenever the digit driver connected to the external decimal point is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

f. Test Mode — In the test mode the main counter is split into groups of two digits each and the groups are clocked in parallel. The reference counter is split such that the clock into the reference count goes directly to the clock of the third decade counter (10 sec/1K cycle range). The count in the main counter is continuously output.

Range Input — The range input selects whether the measurement is made for 1, 10 , 100, 1000 counts of the reference counter. In all functional modes except Unit Counter a change in the range input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the Range Input is changed.

Function Input — The six functions that can be selected are: Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency. This Input is available on the ICM7216A and B only.

These functions select which signal is counted into the Main Counter and which signal is counted by the reference counter as shown in Table 2. In Time Interval a flip flop is toggled first by a 1-0 transition of Input A and then by a 1-0 transition of Input B. The oscillator is gated into the Main Counter from the time Input A toggles the flip flop until Input B gates the flip flop. A change in the function input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the Function Input is changed.

TABLE 2

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (F_A)	Input A	100 Hz (Oscillator ÷ 10^5 or 10^4)
Pe[illegible]d (T_A)	Oscillator	Input A
Ratio (F_A/F_B)	Input A	Input B
Time Interval (A − B)	Osc•(Time Interval FF)	Time Interval FF
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (F_{OSC})	Oscillator	100 Hz (Oscillator ÷ 10^5 or 10^4)

External Decimal Point Input — When the external decimal point is selected this input is active. Any of the digits, except D_7, can be connected to this point. D_7 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point. This input is available on the ICM7216C and D only.

Hold Input — When the Hold Input is at V^+, any measurement in progress is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updated so the last complete measurement is displayed. When Hold is changed to V^-, a new measurement is initiated.

$\overline{\text{Reset}}$ Input — The $\overline{\text{Reset}}$ Input is the same as a Hold Input, except the latches for the Main Counter are enabled, resulting in an output of all zeros.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500 Hz rate with a digit time of 244 μsec. An interdigit blanking time of 6 μsec is used to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays. Any zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled in the Main Counter overflows.

The ICM7216A and C are designed to drive common anode LED displays at peak current of 25mA/segment, using displays with V_F = 1.8 V at 25mA. The average DC current will be over 3mA under these conditions. The ICM7216B and D are designed to drive common cathode displays at peak current of 15mA/segment using displays with V_F = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. Figures 4,5,6 and 7 show the digit and segment currents as a function of output voltage.

To get additional brightness out of the displays, V^+ may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

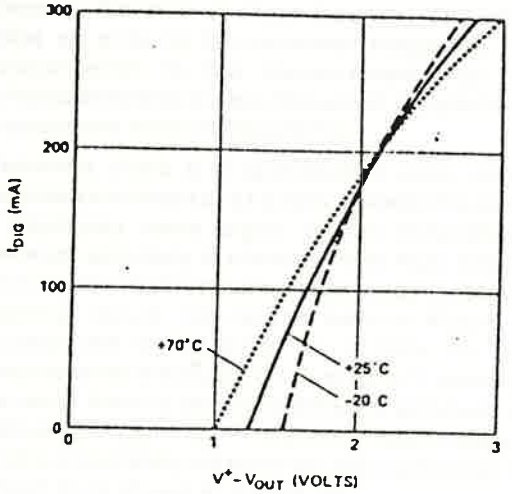
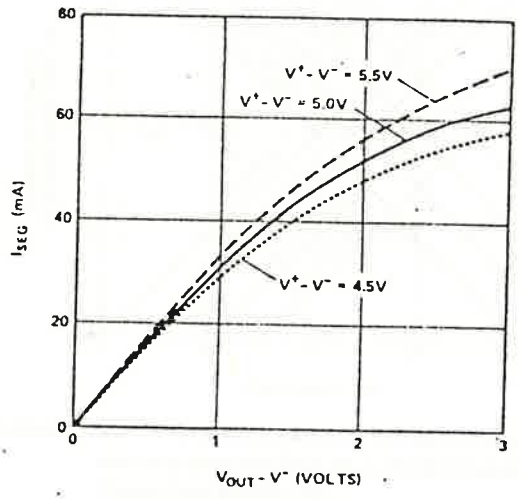


FIGURE 4. ICM7216A & C Typical I_{DIG} vs. $V^+ - V_{OUT}$, $4.5V \leq V^+ - V^- \leq 6.0V$



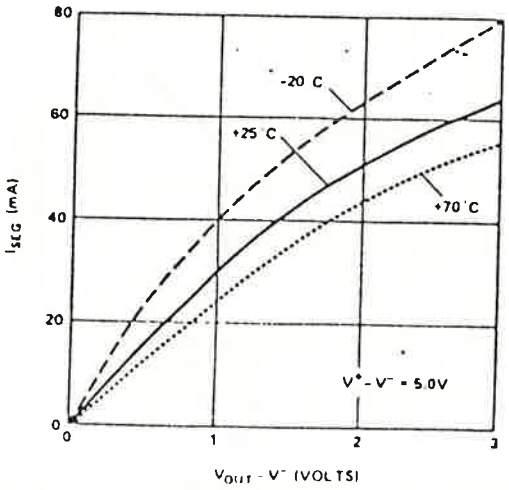
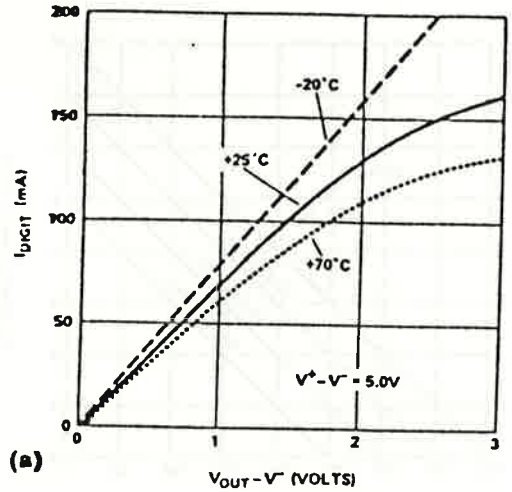
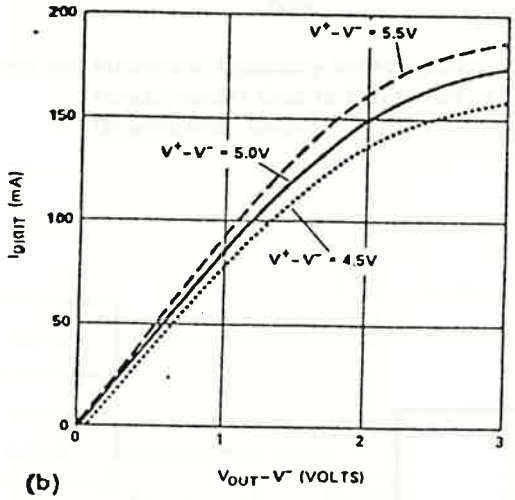


FIGURE 5. ICM7216A & C Typical I_{SEG} vs. $V_{OUT} - V^-$



(a)



(b)

FIGURE 6. ICM7216B & D Typical I_{DIGIT} vs. $V_{OUT} - V^-$

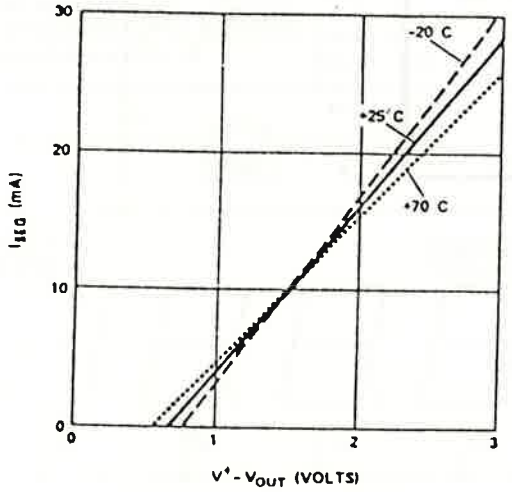
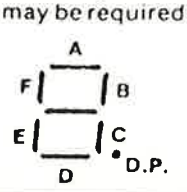


FIGURE 7. ICM7216B & D Typical I_{SEG} vs. $V^+ - V_{OUT}$, $4.5V \leq V^+ - V^- \leq 6.0V$

The segment and digit outputs in ICM7216's are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

Segment Identification:



ACCURACY

In a Universal Counter crystal drift and quantization errors cause errors. In Frequency, Period and Time Interval modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppM/°C will cause a measurement error of 20ppM/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the Frequency mode the maximum accuracy is obtained with high frequency inputs and in Period mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 8, the least accuracy will be obtained at 10 KHz. In Time Interval measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 9. In Frequency Ratio measurement can be more accurately obtained by averaging over more cycles of Input B as shown in Figure 10.

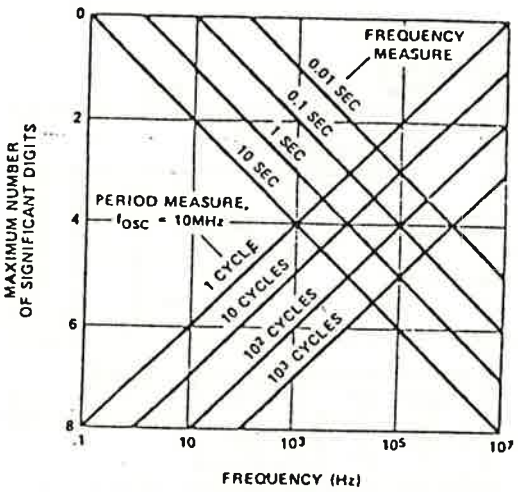


FIGURE 8. Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors

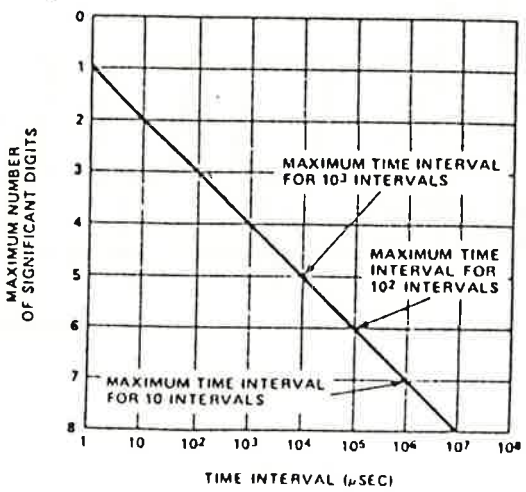


FIGURE 9. Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors

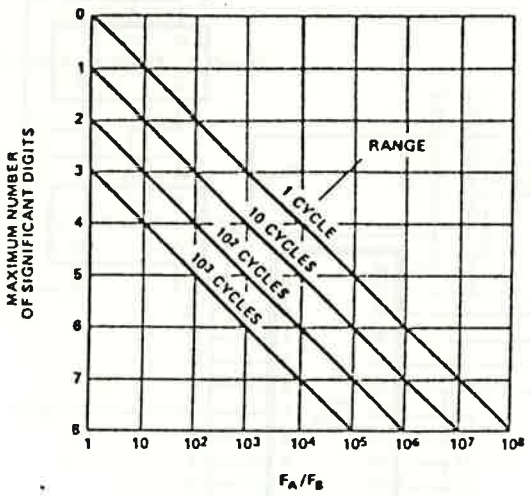


FIGURE 10. Maximum Accuracy for Frequency Ratio Measurement Due to Limitation of Quantization Errors

CIRCUIT APPLICATIONS

The ICM7216 has been designed for use in a wide range of Universal and Frequency counters. In many cases, prescalers will be required to reduce the input frequencies to under 10 MHz. Because Input A and Input B are digital inputs, additional circuitry often will be required for input buffering, amplification, hysterisis, and level shifting to obtain a good digital signal. The cost and complexity for doing this can vary widely depending on the sensitivity and maximum frequency required.

The ICM7216A or B can be used as a minimum component complete Universal Counter as shown in Figure 11. This circuit can use input frequencies up to 10 MHz at Input A and 2 MHz at Input B.

For input frequencies up to 40 MHz the circuit shown in Figure 12 can be used to implement a frequency counter. To obtain the correct measured value, it is necessary to divide the oscillator frequency by four as well as the input frequency. In doing this the time between measurements is also lengthened to 800 msec and the display multiplex rate is decreased to 125 Hz.

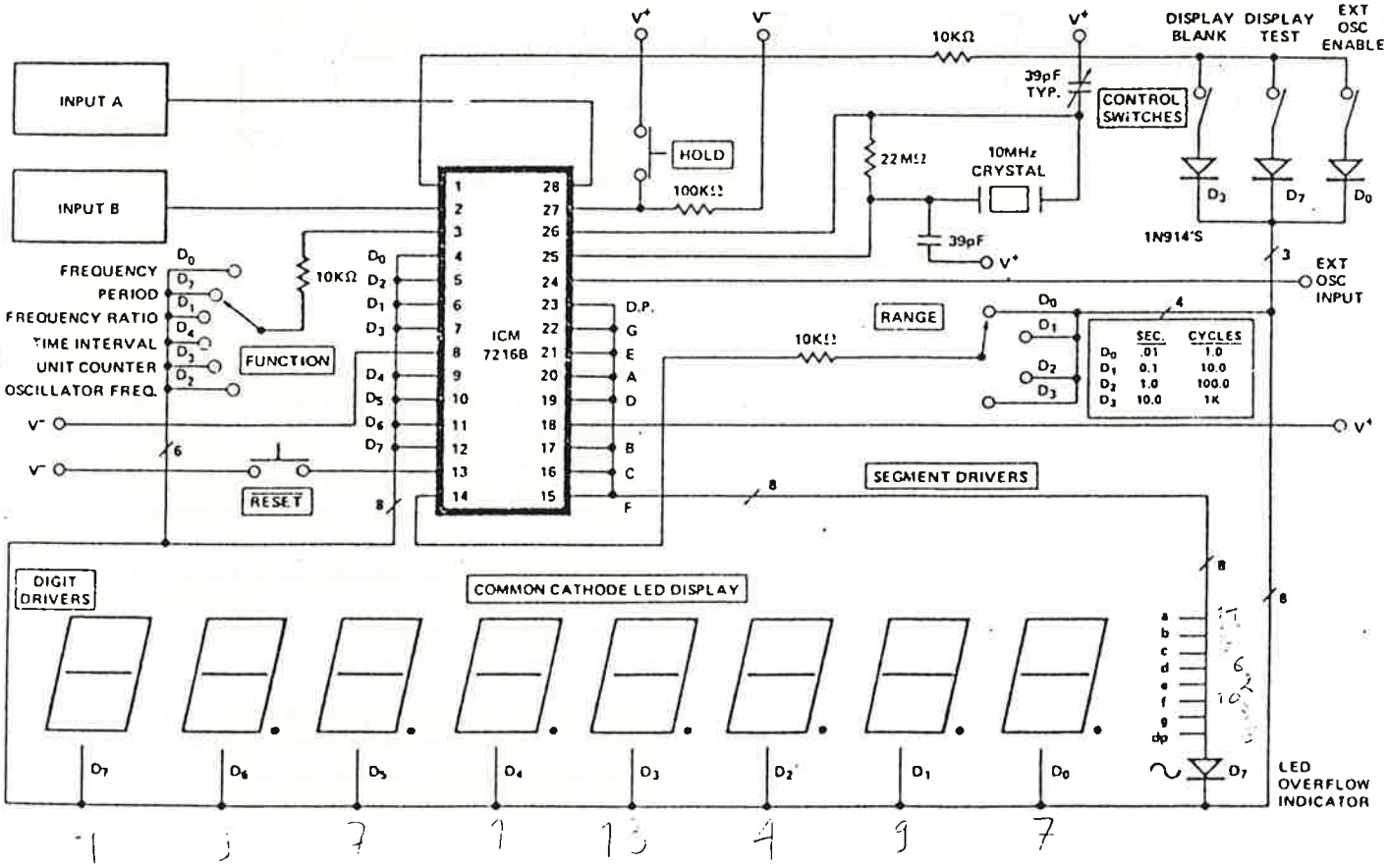


FIGURE 11. 10MHz Universal Counter

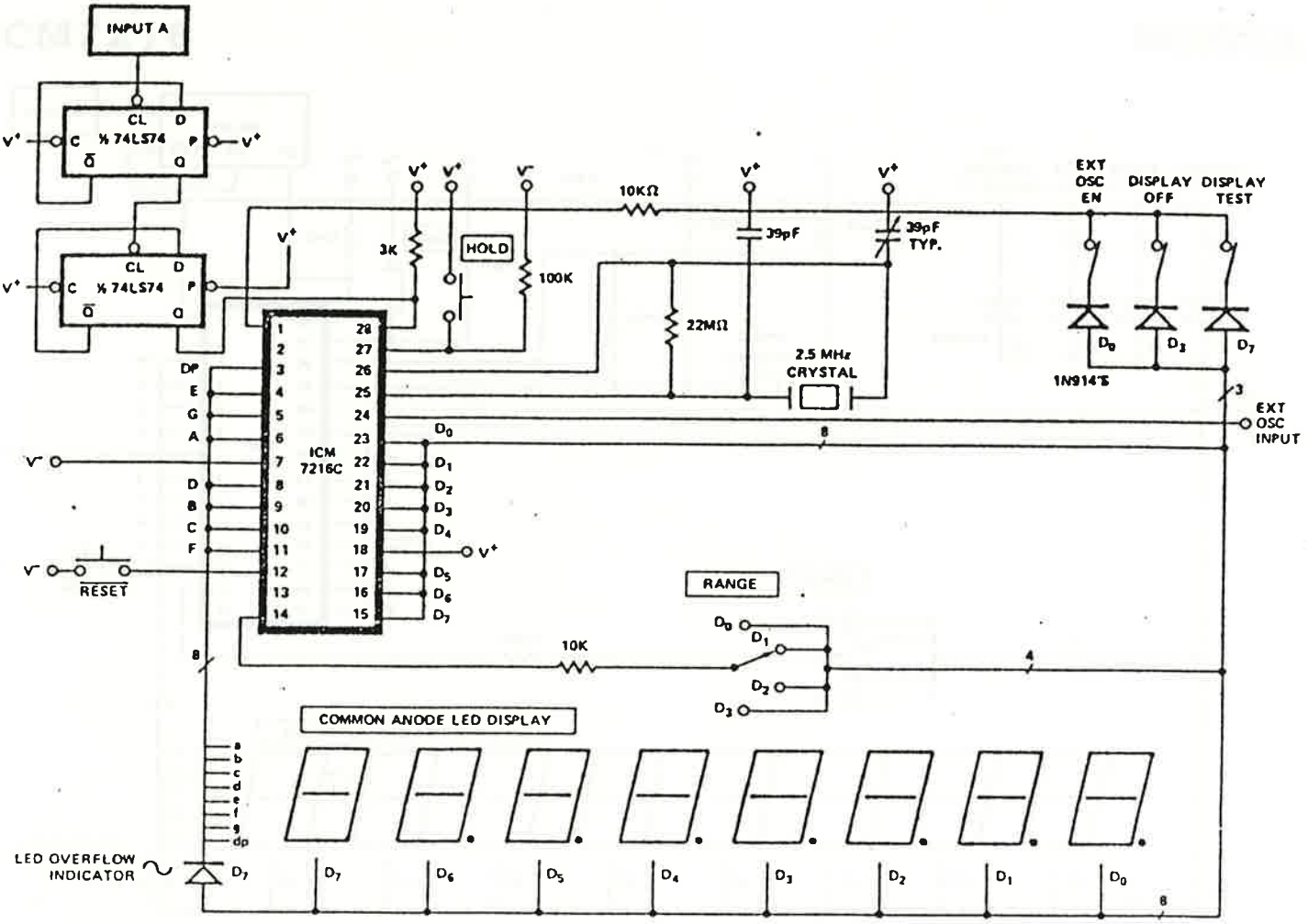


FIGURE 12. 40MHz Frequency Counter

If the input frequency is prescaled by ten, then the oscillator can remain at 10 or 1 GHz, but the decimal point must be moved one digit to the right. Figure 13 shows a frequency counter implemented with a ÷10 prescaler and an ICM7216C. Since there is no external decimal point with the ICM7216A or B, the decimal point must be implemented with additional drivers as shown in Figure 14. Note that there can be one zero to the left of the decimal point since the internal leading zero blanking cannot be changed. In Figure 15 additional logic has been added to count the input directly in mode for maximum accuracy. On both Figures 13 and 14, Input A comes from Q_C of the prescaler rather than Q_A to obtain an input duty cycle of 40%. If the signal at Input A has a very low duty cycle then it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse width to guarantee 50 nsec minimum pulse width.

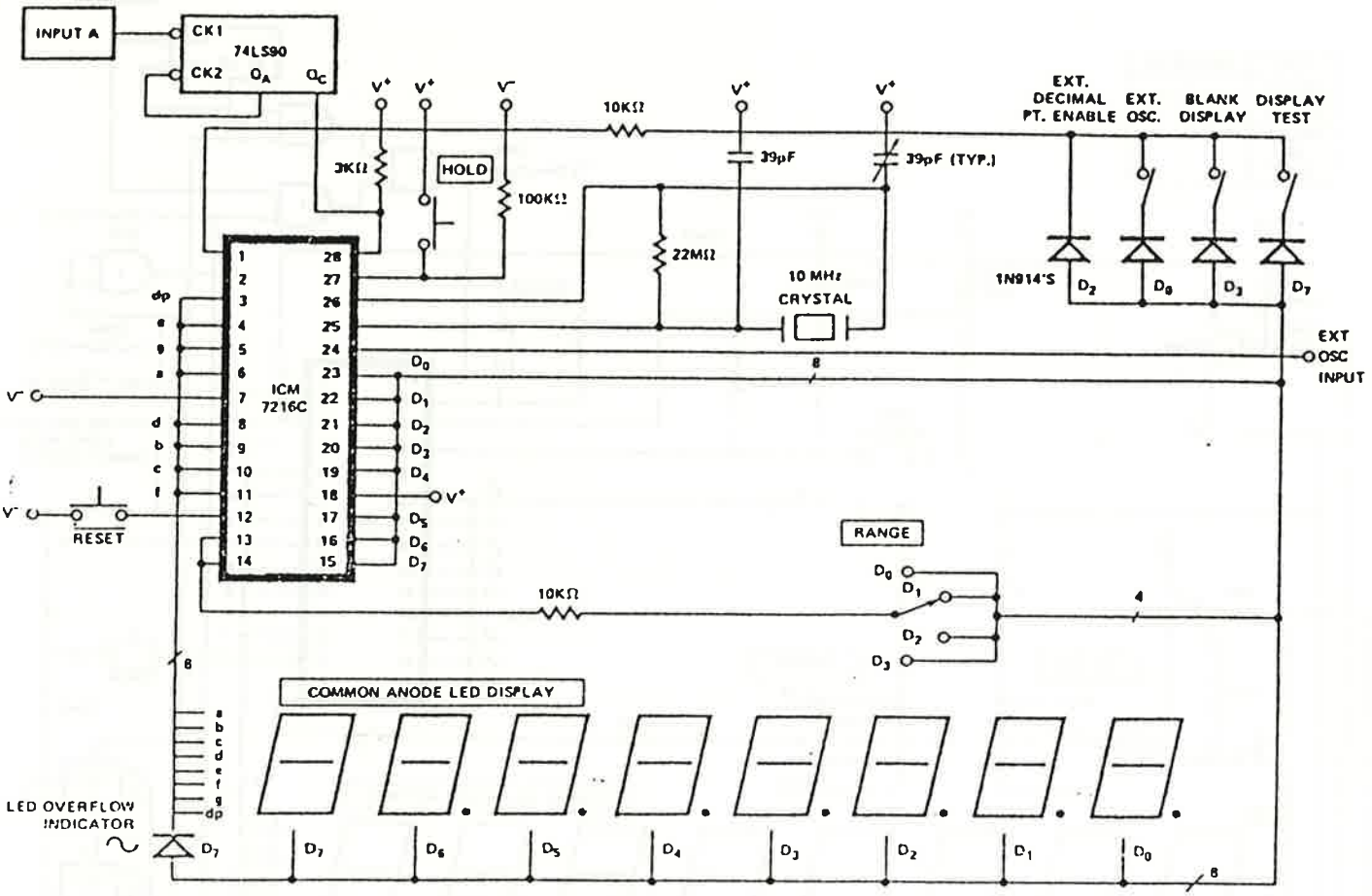
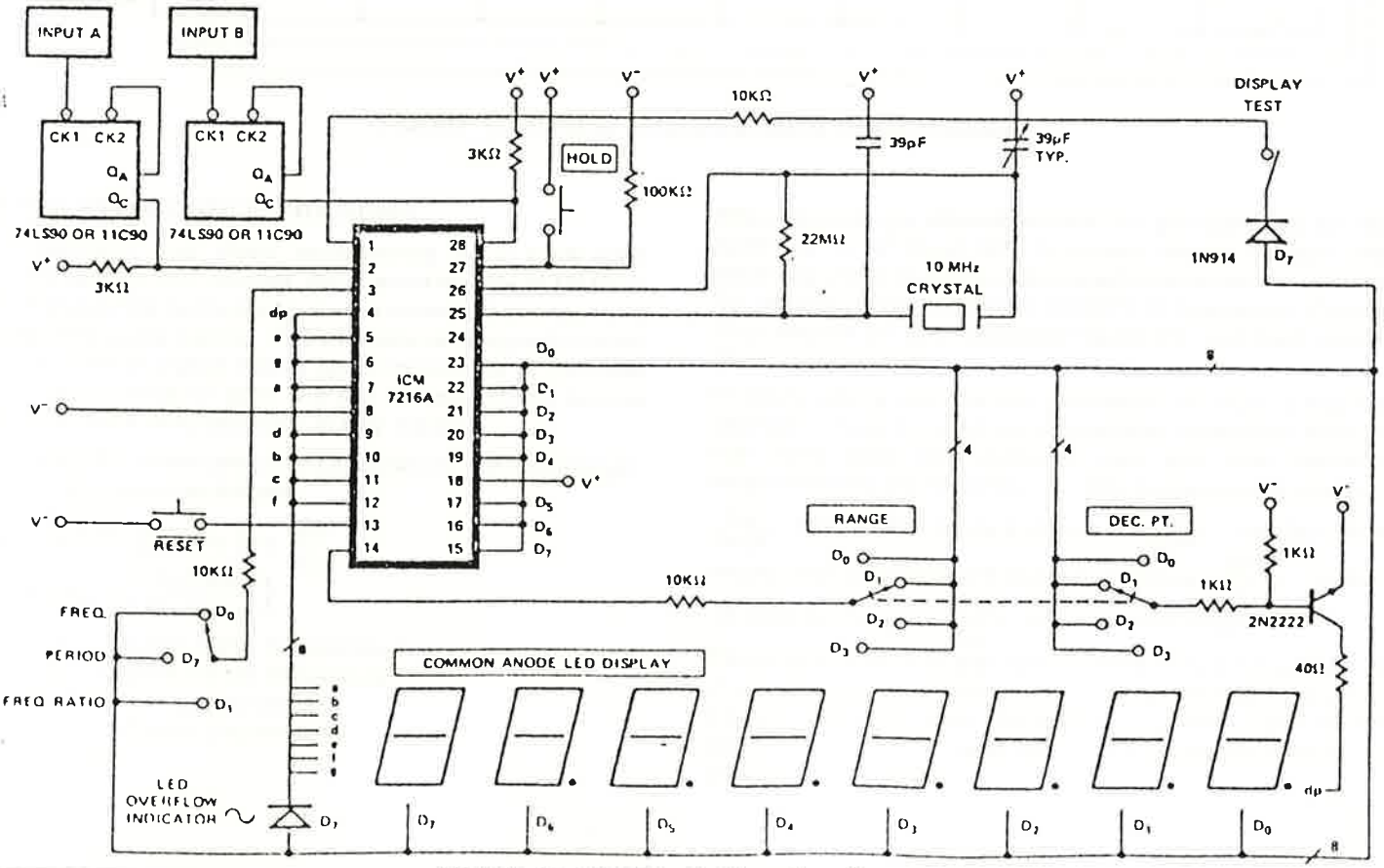


FIGURE 13. 100MHz Frequency Counter



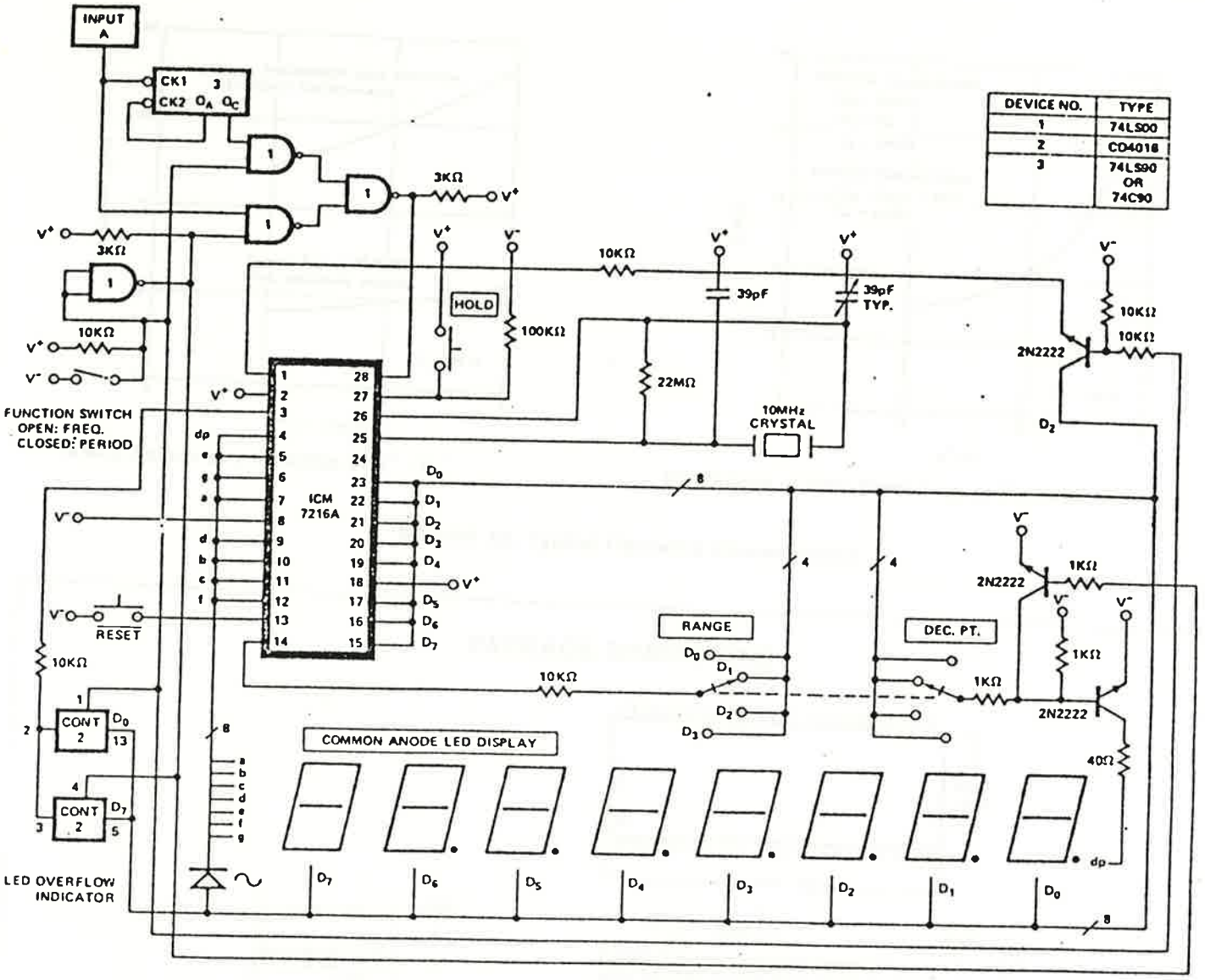


FIGURE 15. 100MHz Frequency, 2MHz Period Counter

OSCILLATOR CONSIDERATIONS

The oscillator has been implemented as a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a 10 MHz crystal with a series resistance of 35Ω and static capacitance of 22pF. As can be seem in the typical characteristics, this oscillator is very stable.

For a specific crystal and load capacitance, the required gm may be calculated as follows:

$$gm = \omega^2 C_{in} C_{out} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

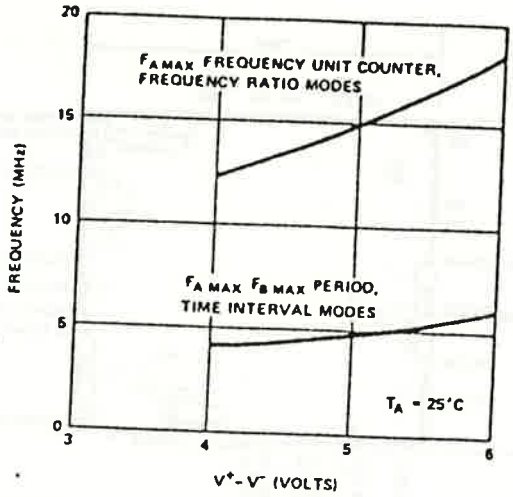
where $C_L = \left(\frac{C_{in}C_{out}}{C_{in}+C_{out}}\right)$

C_O = Crystal Static Capacitance
R_S = Crystal Series Resistance
C_{in} = Input Capacitance
C_{out} = Output Capacitance
$\omega = 2\pi f$

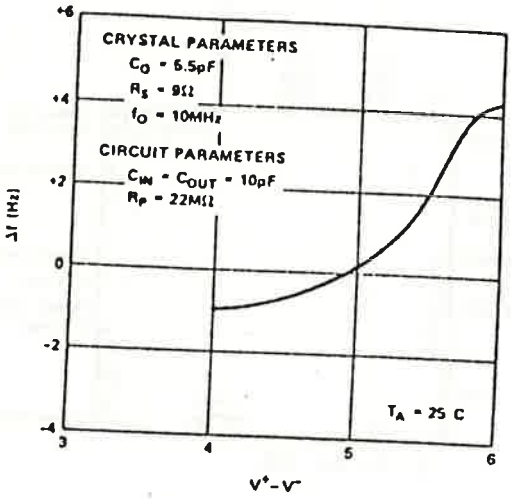
The required gm should exceed the gm specified for the ICM7216 by at least 50% to insure reliable startup. The oscillator input and output pins each contribute about 5pf to C_{in} and C_{out}. For maximum stability of frequency, C_{in} and C_{out} should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10 MHz or 1 MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate is $f_{max} = \frac{f_{osc}}{2\times10^4}$ for 10 MHz mode and $f_{max} = \frac{f_{osc}}{2\times10^3}$ for the 1 MHz mode. The time between measurements is $\frac{2\times10^6}{f_{osc}}$ in the 10 MHz mode and $\frac{2\times10^5}{f_{osc}}$ in the 1 MHz mode.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the External oscillator input to the oscillator output or input can cause undesirable shifts in oscillator frequency.



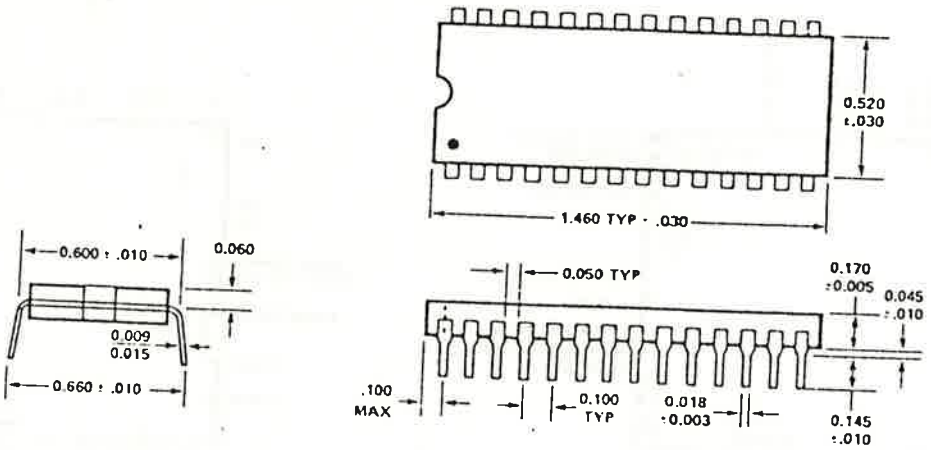
a) $F_{A\,MAX}$, $F_{B\,MAX}$ as a Function of $V^+ - V^-$



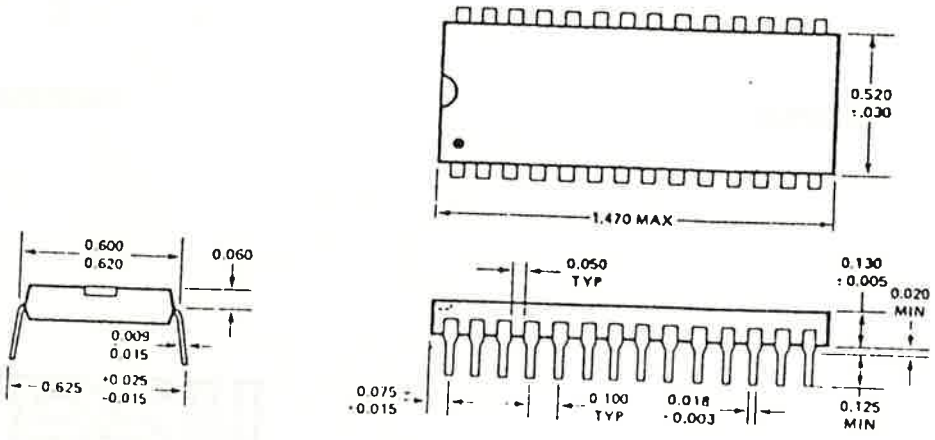
b) Change of Osc. Frequency as Function of $V^+ - V^-$

FIGURE 16. Typical Operating Characteristics

PACKAGE DIMENSIONS



28 PIN CERDIP DUAL IN LINE PACKAGE

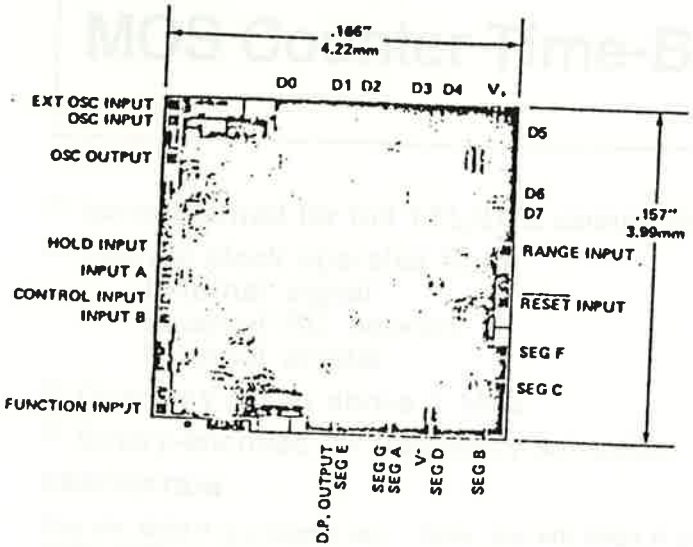


28 PIN PLASTIC DUAL IN LINE PACKAGE

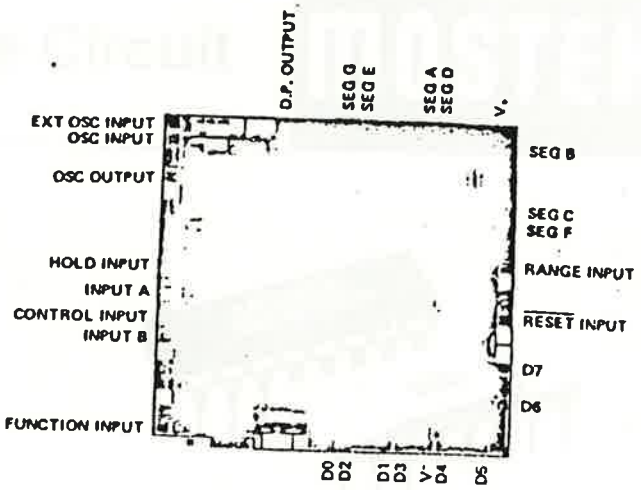
ICM7216

CHIP TOPOGRAPHY

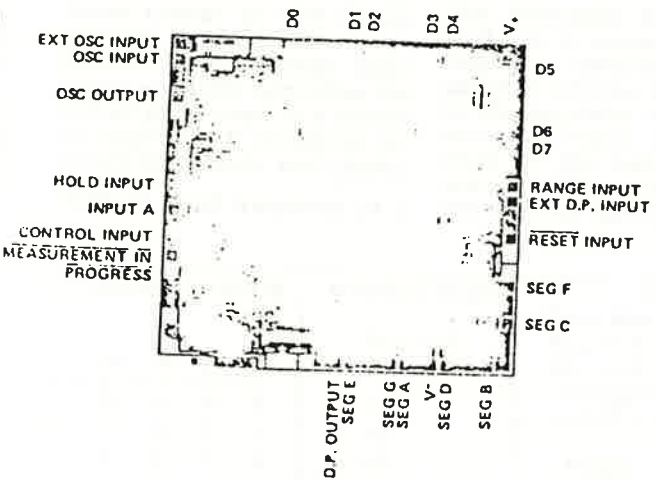
INTERSIL



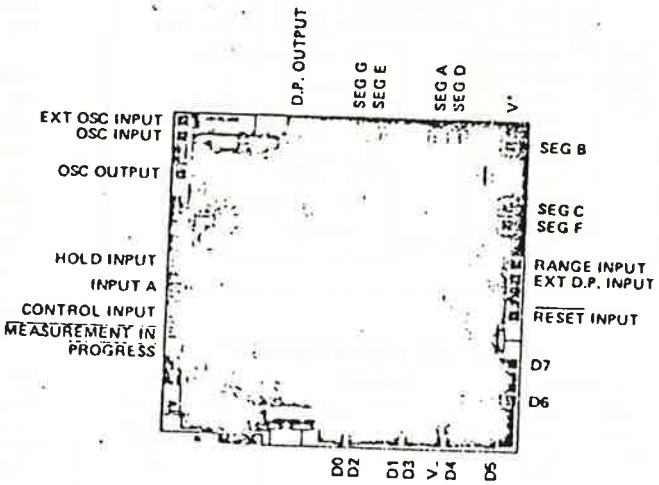
ICM7216A



ICM7216B



ICM7216C



ICM7216D

INTERSIL

10710 N. Tantau Ave., Cupertino, CA 95014 (408) 996-5000 TWX: 910-338-0228

MK 5009 P
MK 5009 N

MOS Counter Time-Base Circuit

MOSTEK

- Ion-implanted for full TTL/DTL compatibility
- Internal clock operates from:
  - External signal
  - External RC network
  - External crystal
- Operates DC to above 1 MHz
- Binary-encoded for frequency selection

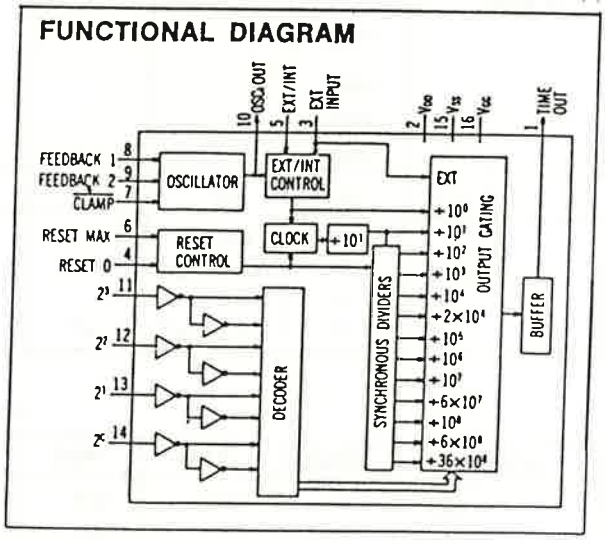
DESCRIPTION

The MK 5009 P is a highly versatile MOS oscillator and divider chain manufactured by Mostek using its depletion-load, ion-implantation process and P.-channel technology. The 16-pin DIP package provides frequency division ranges from 1 to 36×10^8. The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination; the internal oscillator with an external crystal; or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instruments, timers, and clocks.

With an input frequency of 1 MHz, the MK 5009 P provides the basic time periods necessary for most frequency measuring instruments, i.e., 1 μs through 100 seconds. One-minute, ten-minute, and one-hour periods are also available using a 1 MHz input. Using a 1/1.2 MHz input, the MK 5009 P can also provide a 50/60 Hz output for accurate generation of line frequencies in portable instruments or clocks.

The time-base output (TIME OUT) is a square wave, its frequency determined by the selected counter division, and by the oscillator frequency or external input. The falling edge of the output square wave should be used to control external gating circuitry.

FUNCTIONAL DIAGRAM



TIME OUT

ADDRESS INPUTS 2^3	2^2	2^1	2^0	WITHOUT RESET $R_{MAX}=0$ $R_O=0$	RESET Reset Max. $R_{MAX}=1$ $R_O=0$	RESET Reset Min. $R_{MAX}=0$ $R_O=1$	BYPASS MODES (see page 3) Mode 1 $R_{MAX}=V_{GG}$ $R_O=0$	Mode 2 $R_{MAX}=0$ $R_O=V_{GG}$	Mode 3 $R_{MAX}=V_{GG}$ $R_O=V_{GG}$
0	0	0	0	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$
0	0	0	1	$\div 10^1$			$\div 10^1$	$\div 10^1$	$\div 10^1$
0	0	1	0	$\div 10^2$	Resets	Resets	$\div 10^2$	$\div 10^2$	$\div 10^2$
0	0	1	1	$\div 10^3$			$\div 10^3$	$\div 10^3$	$\div 10^3$
0	1	0	0	$\div 10^4$	Counters	Counters	$\div 10^4$	$\div 10^4$	$\div 10^4$
0	1	0	1	$\div 10^5$			$\div 10^2$	$\div 10^5$	$\div 10^2$
0	1	1	0	$\div 10^6$	to their	to their	$\div 10^3$	$\div 10^6$	$\div 10^3$
0	1	1	1	$\div 10^7$			$\div 10^4$	$\div 10^7$	$\div 10^4$
1	0	0	0	$\div 10^8$	Highest	Lowest	$\div 10^5$	$\div 10^5$	$\div 10^2$
1	0	0	1	$\div 6\times10^7$			$\div 6\times10^4$	$\div 6\times10^4$	$\div 6\times10^1$
1	0	1	0	$\div 36\times10^8$	States	States	$\div 36\times10^5$	$\div 36\times10^5$	$\div 36\times10^2$
1	0	1	1	$\div 6\times10^8$			$\div 6\times10^5$	$\div 6\times10^5$	$\div 6\times10^2$
				—			—	—	—
1	1	1	0	$\div 2\times10^4$			$\div 2\times10^1$	$\div 2\times10^1$	$\div 2\times10^1$
1	1	1	1	Ext. In.	Ext. In.	Ext. In.	Ext. Int.	Ext. Int.	Ext. Int.

*Addresses 1100 and 1101 result in Logic 0 at the output regardless of the state of the Reset Max. and Reset 0 inputs.

Logic 1 = High = V_{SS}

Logic 0 = Low = V_{DD}

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} . . . . . + 0.3V to − 20V
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Storage Temperature Range (Ambient) . . . . . − 55 C to + 150°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+ 4.5		+ 5.5	V	
V_{DD}	Supply Voltage	0.0		0.0	V	
V_{GG}	Supply Voltage	− 9.6		− 14.4	V	
f_{XTAL}	Crystal Frequency	0.1		2.0	MHz	
f_{RC}	RC Frequency	DC		200	kHz	
f_{EXT}	External Frequency	DC		2.0	MHz	
t_{PL}	Logic 0 Pulse Width, $\overline{CLAMP}$	—				Note 5
	Ext. Input	200			nsec	
t_{PH}	Logic 1 Pulse Width, Ext. Input	200			nsec	
	Reset Max	10.0			μsec	
	Reset 0	10.0			μsec	
R	Feedback Resistance	.01		2.5	MΩ	Fig. 1
V_{IL}	Input Voltage, Logic 0, Reset Inputs	0.0		0.8	V	
	Reset (Bypass Mode)	V_{GG}		V_{GG} + 1.0	V	Note 2
	All Other Logic Inputs			0.8	V	
V_{IH}	Input Voltage, Logic 1, All Logic Inputs	V_{SS}-1.0	V_{SS}	V_{SS} + 0.3	V	

ELECTRICAL CHARACTERISTICS

(V_{SS} +5V ± 10%; V_{DD} = 0 V; V_{GG} = −12.0 V ± 20%; 0 C $\leq T_A \leq$ 70 C)

	PARAMETER	MIN	TYP†	MAX	UNITS	NOTES
I_{SS}	Supply Current, V_{SS}		6.0	11.0	mA	Note 1
I_{GG}	Supply Current, V_{GG}		6.0	11.0	mA	
I_{IL}	Input Current, Logic 0			− 1.6	mA	Note 2; V_I = 0.4V
V_{OL}	Output Voltage, Logic 0			0.4	V	I_{OL} = 1.6mA*
V_{OH}	Output Voltage, Logic 1	2.4			V	I_{OH} = −40μA*
f_{STA}	Frequency Stability w/ Volt. Change, RC Mode		± 3.0		%/V	Note 3
	/ Temp. Change, RC Mode		− 0.2		%/ C	
	Crystal Mode		—			Note 4
t_{ϵ}	Jitter, Edge-to-Edge Variation		<15		nsec	Temp. & Supply Voltage Constant

†Typical values at V_{SS} = +5V, V_{DD} = 0V, V_{GG} = −12V, and T_A = 25°C

1 Logic inputs at V_{SS}, output open circuited. Each logic input (see Note 2) contributes an additional 1.6 mA (max.) to I_{SS} when at logic 0
2 Logic inputs are: Reset Max; Reset 0; Address Inputs; Ext. Input; Ext Int. Select; and $\overline{Clamp}$
3 Frequency variations due to power supply changes only
4 Crystal mode stability is dependent upon crystal
5 Minimum logic 0 time at clamp input is 50% of oscillator period.

*V_{OH}, V_{OL} apply only to Time Out.

DESCRIPTION OF OPERATION

The MK 5009 P consists basically of a series of counters, selectable via an internal multiplexer. The ÷ 10¹ counter output is used to generate an internal clock signal for the 10^2 through 36×10^4 counter stages, which are fully synchronous with each other.

OSCILLATOR CONTROLS

Operation in the RC oscillator mode is achieved as shown in Figure 1. Frequency, f, is approximately 0.8 RC. The clamp circuit can be used in the RC mode to provide one-shot or accurate start-up operations. When $\overline{\text{Clamp}}$ goes to a logic 0, the internal circuitry is held at a reference level so that upon release of the $\overline{\text{Clamp}}$ (return to logic 1), the oscillator's first cycle will be a full cycle.

The crystal oscillator mode is shown in Figure 2. Values for the resistors are chosen to bias the internal circuitry for optimum performance. The two capacitors are chosen to provide the loading capacitance (C_L) specified for the selected crystal. It is recommended that C1 = C2 = 2 C_L.

RESET/BYPASS CONTROLS

The MK 5009 P provides two different reset conditions. A positive-going pulse of 10 µs or longer on Reset 0 will reset counters to their lowest state, while a positive-going pulse at Reset Max will reset counters to their highest state. The Reset Max control enables the user to set up the counters to provide a falling edge at the next oscillator cycle or negative-going external input, regardless of which divider chain is selected.

In addition, taking one or both Reset Inputs to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes (see table on page 1).

EXTERNAL/INTERNAL FREQUENCY SOURCE

When using an external signal source to operate the MK 5009 P, that signal should be applied at the External Input (Pin 3), and the External/Internal Select (Pin 5) should be brought to logic 1.

For operation with an internal signal, the External Internal Select should be at logic 0.

OSCILLATOR OUTPUT

The oscillator output, provided at Pin 10, is not a true logic output, but may be used to drive a high impedance device such as a junction FET or other MOS circuitry.

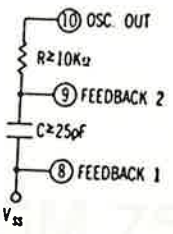


FIG. 1

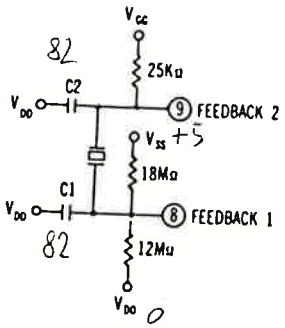
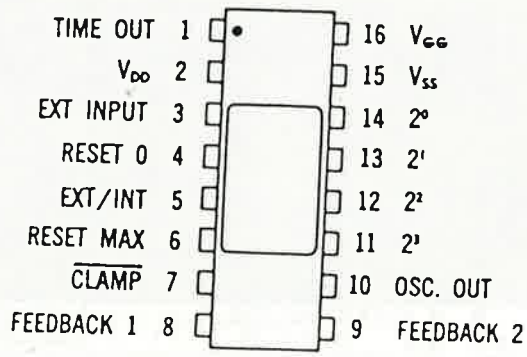
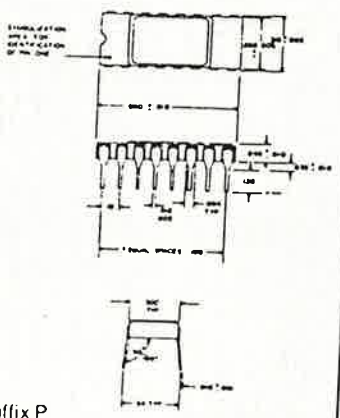


FIG. 2

PIN CONNECTIONS



PACKAGE
16-pin ceramic dual-in-line



Suffix P

PACKAGE
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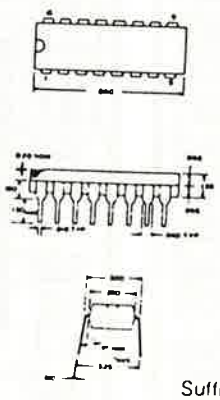
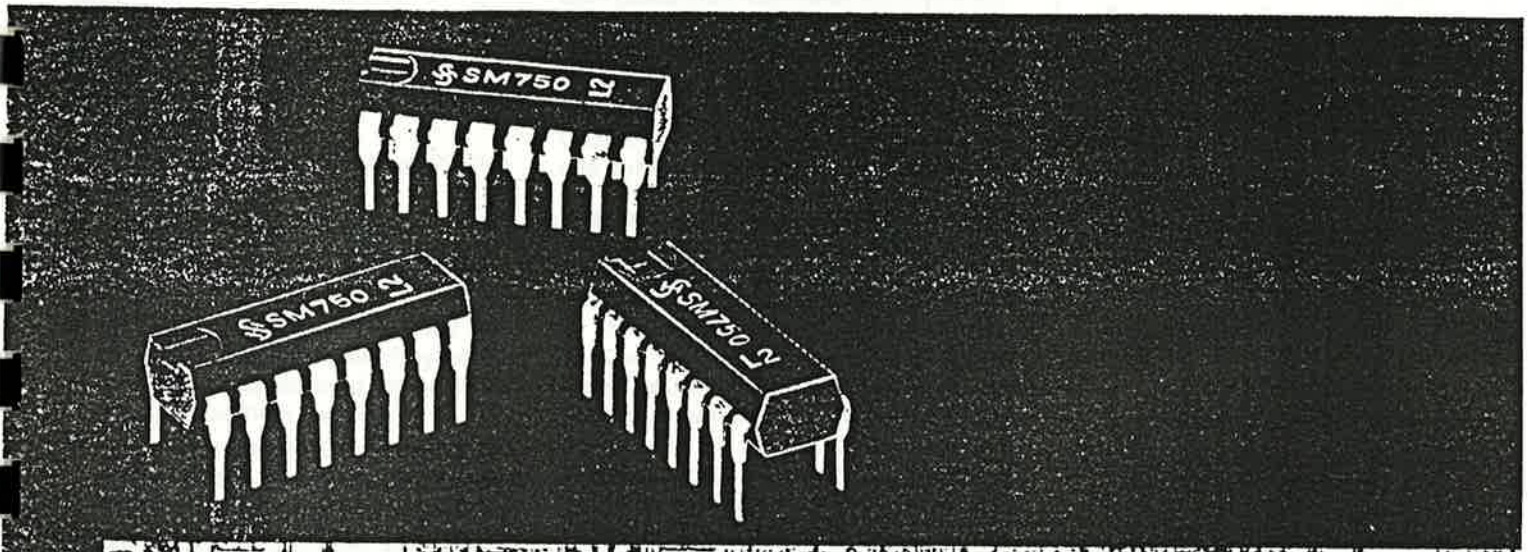


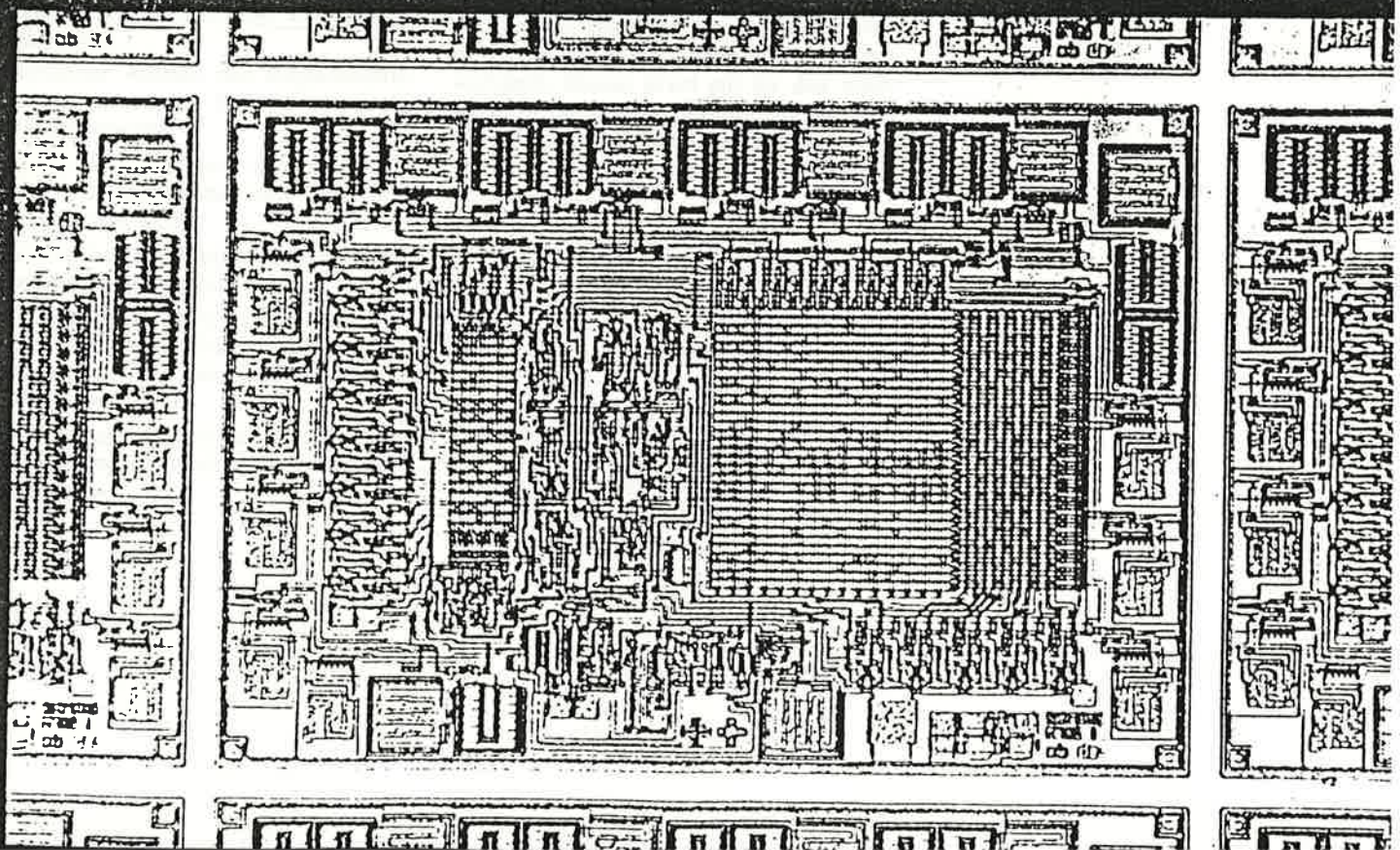
Suffix N

SIEMENS

Rhythmusgenerator für elektronische Orgeln SM 750

Ausgabe 1979





Rhythmusgenerator für elektronische Orgeln

Der in p-Kanal-Depletion-Load-Technik ausgeführte MOS-Baustein SM 750 erzeugt für 6 Rhythmen die Impulsmuster zum Triggern von 5 Begleitinstrumenten. Der SM 750 ist vorwiegend für den Einsatz in einfachen elektronischen Orgeln und anderen Musikinstrumenten konzipiert.

Besondere Merkmale

- Frei wählbare Programmierung von 6 Rhythmen
- 5 Triggerausgänge für Begleitinstrumente
- Integrierter Tempo-Oszillator
- Zählzyklus mit max. 32 Elementarzeiten
- Die Zählzyklusdauer (Taktzahl pro Minute) ändert sich beim Rhythmuswechsel entsprechend dem rhythmusspezifischem Tempo
- Variabel gestaltete Begleitung durch wahlweises Aufteilen der 32 Elementarzeiten auf 2 oder 4 Rhythmustakte
- Alle 6 Rhythmen sind zueinander addierbar
- Einfacher Aufbau der Begleitinstrumente durch auf 8,4 ms verkürzte Triggerimpulse
- Down Beat Ausgang zum Anzeigen des Taktbeginns über eine direkt anschließbare LED
- Definierter Spielbeginn durch Rücksetzeingang möglich
- Variation des Tempos in einem Bereich von einem Drittel bis zum Vierfachen der maskenprogrammierten Zählzyklusdauer
- Wahlweise Push-Pull oder Open Drain Ausgangsstufen für die Triggerausgänge

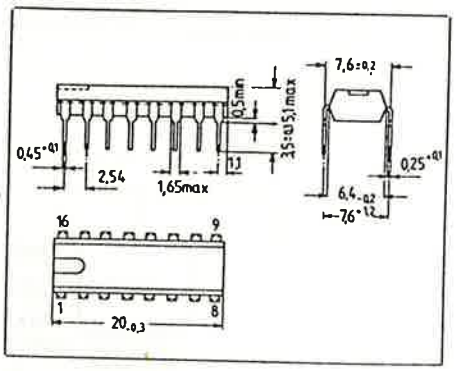
Funktionsbeschreibung anhand des Blockschaltbildes

Die im internen Tempo Oszillator erzeugte Frequenz wird in einem 7-Bit Taktfrequenzzähler geteilt. Aus diesem Zähler wird im Dekoder entsprechend dem gewählten Rhythmus ein rhythmusspezifischer Takt RCF abgeleitet. Im gleichen Block wird ein Signal zum Verkürzen der Triggerimpulse auf 8,4 ms bei Standardtempo (entspricht einer Oszillatorfrequenz von 1,5 kHz) erzeugt, das auf die Ausgangslogik einwirkt.

Aus den rhythmusspezifischen Takt RCF werden in einem weiteren Teiler die internen Steuertakte TUM und TUS für den 5-Bit Zähler erzeugt. Der 5-Bit Zähler steuert über einen Dekoder in max. 32 Elementarzeitschritten die Zeilen eines 960-Bit ROM an. Sämtliche 30 Spalteninformationen laufen über einen Multiplexer, wo nur die dem gewählten Rhythmus zugehörigen 5 Spalteninformationen weiter an die Ausgangslogik durchgeschaltet werden. Die Triggerimpulse für die Begleitinstrumente werden über die Ausgangslogik auf 8,4 ms verkürzt. Dieser Wert gilt für das maskenprogrammierte Standardtempo des jeweiligen Rhythmus und er ändert sich entsprechend, wenn von diesem Tempo abgewichen wird.

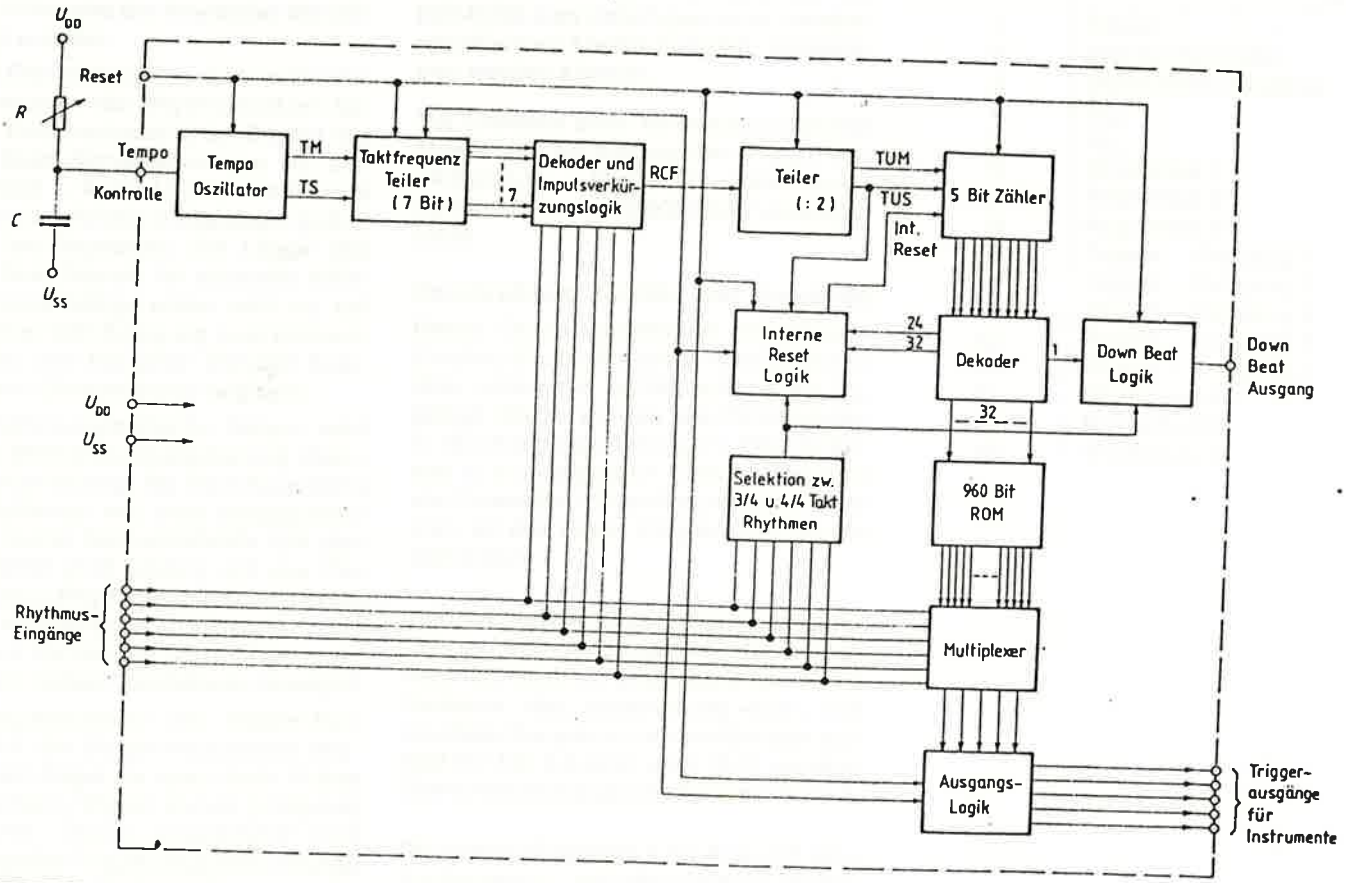
Der eingegebene Rhythmus wird auf ¾ oder ⁴⁄₄ Takt selektiert. Bei einem ¾ Takt Rhythmus wird der 5-Bit Zähler bereits nach 24 Elementarzeitschritten über die interne Reset Logik zurückgesetzt.

Werden mehrere Rhythmen zueinander addiert, so bestimmt der Rhythmus mit dem langsamsten Standardtempo bzw. der ¾ Takt Rhythmus die Frequenz des rhythmusspezifischen Taktes RCF.

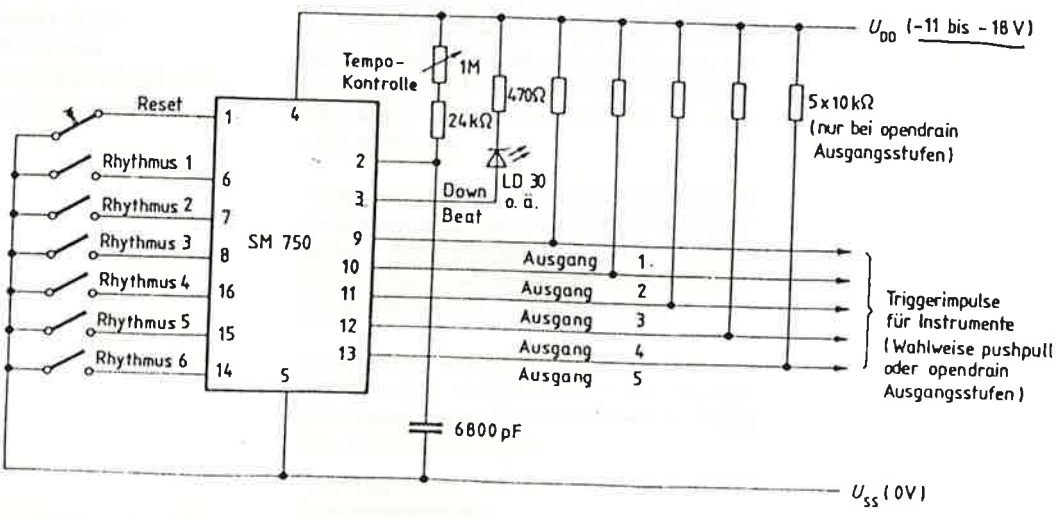


Kunststoff-Steckgehäuse
16 Anschlüsse
20 A 16 DIN 41 866
Gewicht etwa 1,2 g

Blockschaltbild



Anwendungsschaltung



Variationsmöglichkeiten des SM 750

Neben der ROM-Belegung können bei der Maskenprogrammierung noch folgende Wünsche der Anwender berücksichtigt werden:

Die 32 Elementarzeiten sind wahlweise mit zwei oder vier Rhythmustakten belegbar. Entsprechend ist der Beginn des Down Beat Signal wahlweise zur Elementarzeit 1, 9 (7), 17 (13) und 25 (19) möglich. Die Zahlen in Klammern gelten für ¾-Takt-Rhythmen. Die Länge des Down Beat Signals ist ebenfalls wählbar. Zweckmäßigerweise wird es bei einer Zwei-Takt-Belegung zwei Elementarzeiten und bei einer Vier-Takt-Belegung eine Elementarzeit lang sein.

Das rhythmusspezifische Tempo wird bei der Maskenprogrammierung ebenfalls berücksichtigt. Als Grundlage dient der Rhythmus mit dem langsamsten Tempo. Seine Taktzahl/Minute füllt den 7-Bit Zähler (128 Stufen) voll aus. Die restlichen 5 Rhythmen mit schnellerem Tempo werden dann so auskodiert, daß in keinem Fall die Soll-Taktzahl um mehr als einem halben Takt/Minute abweicht.

Die Ausgangsstufen der Trigger-Ausgänge für die Begleitinstrumente werden in der Regel als open drain Stufen mit positivem Trigger Impuls (H-Signal) ausgeführt. Davon abweichend sind auch negative Trigger Impulse (L-Signal) bzw. Push-pull Stufen möglich. In der nachfolgenden Leertabelle für die Programmierung des SM 750 steht unter der Rubrik Ausgangsart

- OD für open drain,
- PP für Push-pull.
- \+ für H-Triggersignal und
- \- für L-Triggersignal.

Programmierung des SM 750

Auf Seite 8 befindet sich eine Leertabelle, in die alle Informationen, die SIEMENS zum Anfertigen einer kundenspezifischen Maske benötigt, eingetragen werden können.

Vor Erstellen einer kundenspezifischen Maske wird ein Auftrag über eine zu vereinbarende Mindestabnahmemenge (Größenordnung 10.000 Stck) vorausgesetzt.

Beschreibung der Ein- und Ausgänge

Reset: Durch kurzzeitiges Offenlassen (Taster) dieses Eingangs wird er intern über einen pull up-Widerstand an U_{DD} gelegt. Dabei werden alle Zählerstufen in die Ausgangsstellung (= Elementarzeit 1) zurückgesetzt. Gleichzeitig wird ein Down-Beat-Signal erzeugt. Ansonsten ist der Reset Eingang mit U_{SS} zu verbinden.

Tempokontrolle ist der Eingang des integrierten Tempo-Oszillators, der mit einem RC-Glied zu beschalten ist. Durch Variieren des Widerstands kann die Oszillatorfrequenz in einem Bereich von 500 Hz bis 5,5 kHz verändert werden. Siehe Anwendungsschaltung auf Seite 3.

Rhythmus-Eingänge 1 bis 6: Durch Verbinden mit U_{SS} wird der jeweilige Rhythmus gewählt. Gleichzeitig können auch mehrere Eingänge an U_{SS} gelegt werden. Die zugehörigen Rhythmen werden dann zueinander addiert. Die Eingänge der nicht gewählten Rhythmen werden nicht beschaltet. Ist kein Rhythmus gewählt, so steht der SM 750 in Rücksetzstellung (= Elementarzeit 1, Down Beat LED leuchtet).

Triggerausgänge für Instrumente 1 bis 5: An diesen Ausgängen erscheinen in zeitlicher Aufeinanderfolge die Impulsmuster zum Aktivieren der jeweils angeschlossenen Begleitinstrumente.

Down-Beat Ausgang dient zur Anzeige des Tempos mittels einer LED. Zu Beginn eines jeden Zählzyklus oder Taktes erscheint ein H-Signal.

U_{DD}, U_{SS} sind die Anschlüsse für die Speisespannung

Anschlußbelegung

Anschluß Nr.	Anschlußbezeichnung
1	Reset
2	Tempo Kontrolle
3	Down Beat Ausgang
4	U_{DD}
5	U_{SS}
6	Rhythmus 1
7	Rhythmus 2
8	Rhythmus 3
9	Trigger – Ausgang 1
10	Trigger – Ausgang 2
11	Trigger – Ausgang 3
12	Trigger – Ausgang 4
13	Trigger – Ausgang 5
14	Rhythmus 6
15	Rhythmus 5
16	Rhythmus 4

Standardbelegung

Rhythmus Bezeichnung	Takte/ Minute
Rhythmus 1: Samba	23
Rhythmus 2: Rock	35
Rhythmus 3: Bossa Nova	37
Rhythmus 4: Swing	43
Rhythmus 5: Slow-Rock	40
Rhythmus 6: Walzer	59

Begleitinstrument Bezeichnung	Ausgangsart OD	PP	+	-
Ausgang 1: Bass	X		X	
Ausgang 2: Akkord	X		X	
Ausgang 3: Bass Trommel	X		X	
Ausgang 4: Kleine Trommel / Holz wood.	X		X	
Ausgang 5: Becken cymbal.	X		X	

Elementarzeit Nr.	1	9 (7)	17 (13)	25 (19)
Down Beat Signal (Beginn)	X		X	

Dauer des Down-Beat Signals in Elementarzeiten: 2

Elementar-Zeit Nr. (Zählerstand)	Rhythmus 1					Rhythmus 2					Rhythmus 3					Rhythmus 4					Rhythmus 5					Rhythmus 6				
	Ausgang Nr.					Ausgang Nr.					Ausgang Nr.					Ausgang Nr.					Ausgang Nr.					Ausgang Nr.				
	1	2	3	4	5	1	2	3	4	5	1	2	3	4	5	1	2	3	4	5	1	2	3	4	5	1	2	3	4	5
1	X	X			X	X	X	X		X	X	X	X	X	X	X		X		X	X	X	X		X	X		X		X
2																														
3				X	X					X					X		X					X			X					
4																		X	X	X										
5	X	X			X				X	X		X			X							X			X		X		X	X
6																				X										
7				X	X		X	X		X			X	X	X	X	X	X		X		X		X	X					
8																														
9	X	X			X	X		X		X	X		X		X							X			X		X		X	X
10																		X	X	X										
11				X	X					X		X			X							X	X		X					
12				X																X										
13		X			X				X	X				X	X	X	X	X		X	X	X	X		X	X		X		X
14																														
15	X			X	X				X	X		X			X							X			X					
16			X															X	X	X										
17	X	X			X	X	X	X		X	X		X		X							X			X		X		X	X
18																	X			X										
19	X	X		X	X					X		X			X	X		X		X		X		X	X					
20																														
21					X				X	X				X	X							X			X		X		X	X
22																		X	X	X										
23	X	X		X	X		X	X		X		X	X		X							X	X		X					
24																				X										
25	X	X			X	X		X		X	X		X		X															
26																														
27				X	X		X			X		X		X	X															
28				X																										
29		X			X				X	X					X															
30																														
31		X		X	X				X	X					X															
32			X																											

Grenzdaten
(Alle Spannungen sind auf U_{SS} = 0V bezogen)

		untere Grenze B	obere Grenze A	Einheit
Eingangsspannung	U_{IM}	−18	+0,3	V
Speisespannung	U_{DD}	−18	+0,3	V
Ausgangsstrom für Down Beat (Anschluß 3)	I_A		20	mA
Ausgangsstrom für Instrumentenausgänge	I_A		3	mA
Umgebungstemperatur	T_U	0	70	°C
Lagertemperatur	T_s	−55	125	°C
Gesamtverlustleistung	P_{tot}		100	mW
Verlustleistung je Ausgang	P_Q		10	mW

Kenndaten (T_U = 0 ... 70°C)
(Alle Spannungen sind auf U_{SS} = 0V bezogen)

		Prüfbedingung	untere Grenze B	typ.	obere Grenze A	Einheit
Speisespannung	U_{DD}		−18		−10	V
Speisestrom	I_{DD}	U_{DD} = −18 V I_Q (Anschluß 3) = 0			5	mA

Tempo Kontroll-Eingang
Prozentuelle Veränderung des max. Tempos in Abhängigkeit von der Speisespannungs- und Temperaturänderung

Tempo Oszillatorfrequenz	f	Siehe Prüfschaltung 1	0,5	1,5	5,5	kHz
Max. Tempo-Veränderung		U_{DD} von −10 V auf −18 V			5	%
Max. Tempo-Veränderung		T von 25°C auf 70°C R = Kohleschichtwiderstand C = Styroflexkondensator			5	%

Reset-Eingang

H-Eingangsspannung	U_{IH}		−0,8		U_{SS}	V
L-Eingangsspannung	U_{IL}		U_{DD}		−4,1	V
H-Impulsbreite	t_{WH}		5			µs
H-L Übergangszeit	t_{THL}				0,5	µs
L-H Übergangszeit	t_{TLH}				0,7	µs

Rhythmus-Eingänge 1–6

H-Eingangsspannung	U_{IH}		−0,8		U_{SS} ·	V
L-Eingangsspannung	U_{IL}		U_{DD}		−4,1	V

Ausgänge 1–5
Open Drain Ausführung

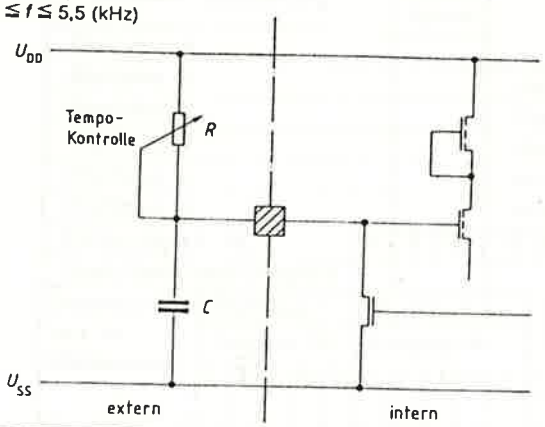
H-Ausgangsspannung	U_{QH}	Siehe Prüfschaltung 2	−0,3		U_{SS}	V
L-Ausgangsspannung	U_{QL}	Siehe Prüfschaltung 2	U_{DD}		U_{DD} +3,5	V
Widerstand nach U_{SS} (Ausgang im H-Zustand)	R_{ON}	R_L = 10 kΩ nach U_{DD}			250	Ω
Ausgangsleckstrom	I_{QL}	$U_{QL} = U_{DD}$			−10	µA
Push Pull Ausführung						
H-Ausgangsspannung	U_{QH}	Siehe Prüfschaltung 3	−0,3		U_{SS}	V
L-Ausgangsspannung	U_{QL}	Siehe Prüfschaltung 4	U_{DD}		U_{DD} +3,5	V
Widerstand nach U_{SS} (Ausgang im H-Zustand)	R_{IN}	I_{QH} = −1 mA $U_A = U_{QH}$			500	Ω
Ausgangsleckstrom	I_{QL}	$U_{QL} = U_{DD}$			−10	µA

Down Beat-Ausgang
Open Drain mit Hilfslastelement

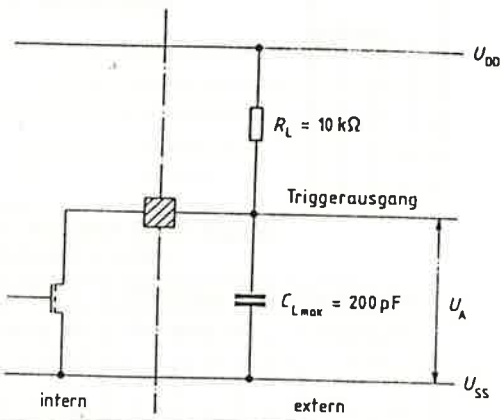
H-Ausgangsspannung	U_{QH}	Siehe Prüfschaltung 5	−0,6		U_{SS}	V
L-Ausgangsspannung	U_{QL}	Siehe Prüfschaltung 6	U_{DD}		U_{DD} +1	V
Widerstand nach U_{DD}	$R_{IN\,L}$	$U_A = U_{SS}$ −5 V U_{DD} = −10 V			300	kΩ
Widerstand nach U_{SS}	$R_{IN\,H}$	$U_A = U_{SS}$ −0,5 V			500	Ω
Ausgangsstrom						

Prüfschaltungen

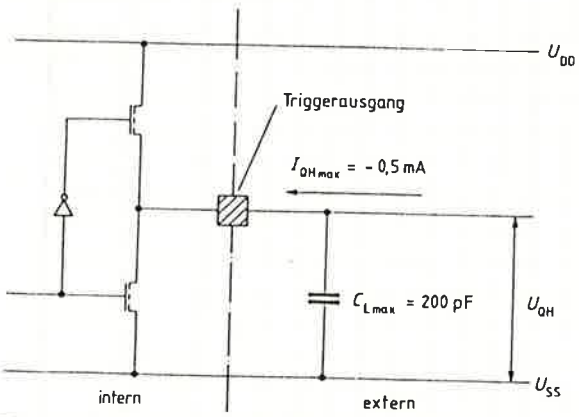
Prüfschaltung 1:
$0{,}024 \leq R\ 1{,}02\ (M\Omega)$
$C = 6800$ pF
$0{,}5 \leq f \leq 5{,}5$ (kHz)



Prüfschaltung 2:



Prüfschaltung 3:



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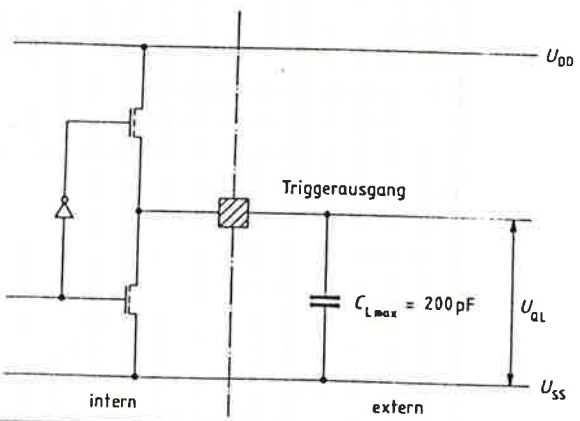

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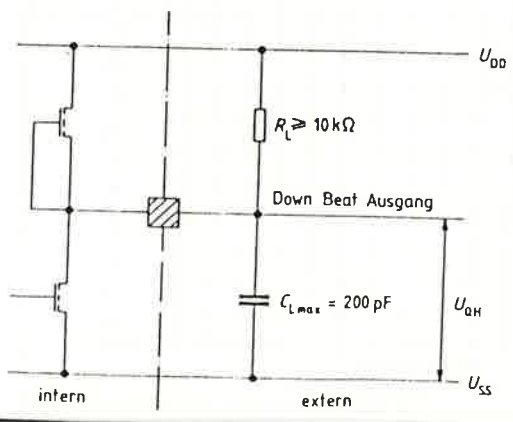
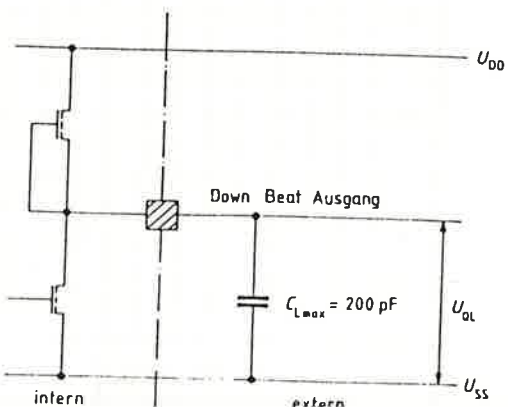


Prüfschaltung 6:



Leertabelle

Rhythmus Bezeichnung	Takte / Minute	Begleitinstrument Bezeichnung	Ausgangsart OD	PP	+	-
Rhythmus 1:						
Rhythmus 2:		Ausgang 1:				
Rhythmus 3:		Ausgang 2:				
Rhythmus 4:		Ausgang 3:				
Rhythmus 5:		Ausgang 4:				
Rhythmus 6:		Ausgang 5:				

Elementarzeit Nr.	1	9 (7)	17 (13)	25 (19)	Dauer des Down-Beat Signals in Elementarzeiten:
Down Beat Signal (Beginn)					

Elementar-zeit Nr. (Zählerstand)	Rhythmus 1 Ausgang Nr. 1	2	3	4	5	Rhythmus 2 Ausgang Nr. 1	2	3	4	5	Rhythmus 3 Ausgang Nr. 1	2	3	4	5	Rhythmus 4 Ausgang Nr. 1	2	3	4	5	Rhythmus 5 Ausgang Nr. 1	2	3	4	5	Rhythmus 6 Ausgang Nr. 1	2	3	4	5
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Firma:	Unterschrift: Datum:	Typ[1] SM 750 .....

XR-2242

Long-Range Timer

GENERAL DESCRIPTION

The XR-2242 is a monolithic Timer/Controller capable of producing ultra-long time delays from micro-seconds to days. Two timing circuits can be cascaded to generate time delays or timing intervals up to one year. The circuit is comprised of an internal time-base oscillator, an 8-bit binary counter and a control flip-flop. For a given external R-C network connected to the timing terminal, the circuit produces an output timing pulse of 128 RC. If two circuits are cascaded, a total time delay of $(128)^2$ or 16,384 RC is obtained.

The timing cycle for the XR-2242 is initiated by applying a positive-going trigger pulse to pin 6. The trigger input actuates the time-base oscillator, enables the counter section, and sets the output to "low" state. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to pin 5.

In monostable timer applications, the output terminal (pin 3) is connected back to the reset terminal. In this manner, after 128 clock pulses are applied to the circuit, this output goes to "high" state and resets the circuit thus completing the timing cycle. Thus, subsequent to triggering, the output at pin 3 will produce a total timing pulse of 128 RC before the circuit resets itself to complete the timing cycle. During the timing interval, the secondary output at pin 2 produces a square-wave output with the period of 2 RC.

If the output at pin 3 is not connected back to the reset terminal, the circuit continues to operate in an astable mode, subsequent to a trigger input.

FEATURES

Timing from micro-seconds to days
Wide supply range: 4.5V to 15V
TTL and DTL compatible outputs
High accuracy: 0.5%
Excellent Supply Rejection: 0.2%/V
Monostable and Astable Operation

APPLICATIONS

Long Delay Generation
Sequential Timing
Precision Timing
Ultra-Low Frequency Oscillator

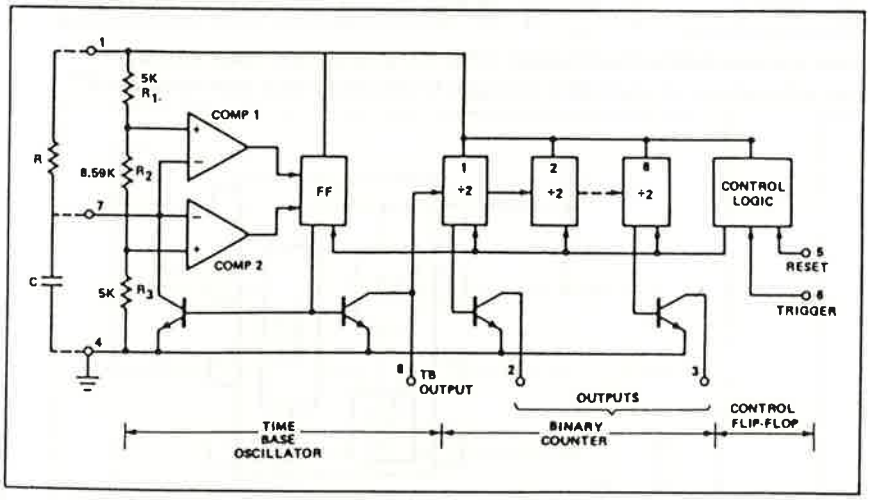
ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation (package limitation)	
Ceramic package	385 mW
Plastic Package	300 mW
Derate above +25°C	2.5 mW/°C
Temperature Range	
Operating	
XR-2242M	−55°C to +125°C
XR-2242C	0°C to +75°C
Storage	−65°C to +150°C

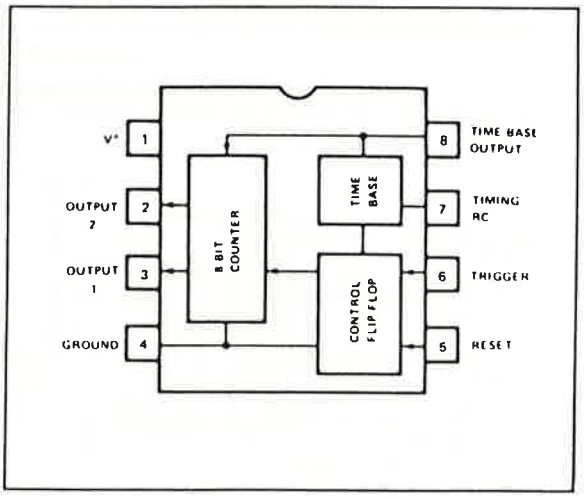
AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-2242M	Ceramic	−55°C to + 125°C
XR-2242CN	Ceramic	0°C to +75°C
XR-2242CP	Plastic	0°C to +75°C

SIMPLIFIED SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 3, $V^+ = 5V$, $T_A = 25°C$, $R = 10\ k\Omega$, $C = 0.1\ \mu F$, unless otherwise noted.

PARAMETERS	XR-2242M			XR-2242C			UNIT	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage	4		15	4		15	V	
Supply Current		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
Total Circuit		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
TIME BASE SECTION								See Figure 3
Timing Accuracy *		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ $0°C \leq T \leq 75°C$
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geq 8$ Volts
Max Frequency	100	130			130		kHz	$R = 1\ k\Omega$, $C = 0.007\ \mu F$
Recommended Range of Timing Components								See Figure 5
Timing Resistor, R	0.001		10	0.001		5	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	Low-Leakage Capacitor Required.
TRIGGER/RESET CONTROLS								
Trigger								Measured at Pin 6, $V_{RS} = 0$
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time **		1			1		μsec	
Reset								Measured at Pin 5, $V_{TR} = 0$
Reset Threshold		1.4	2.0		1.4	2.0	V	
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time **		0.8			0.8		μsec	
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.5	1.0			1.0		MHz	$V_{RS} = 0$, $V_{TR} = 5V$
Input:								
Impedance		20			20		kΩ	
Threshold	1.0	1.4		1.0	1.4		V	
Output:								
Rise Time		180			180		nsec.	Measured at Pins 2 and 3
Fall Time		180			180		nsec.	$R_L = 3K\Omega$, $C_L = 10\ pF$
Sink Current	3	5		2	4		mA	$V_{OL} \leq 0.4V$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} \leq 15V$

*Timing error solely introduced by XR-2242, measured as % of ideal time-base period of T = 1.00 RC.

**Propagation delay from application of trigger (or reset) input to corresponding state change in first stage counter output at pin 2.

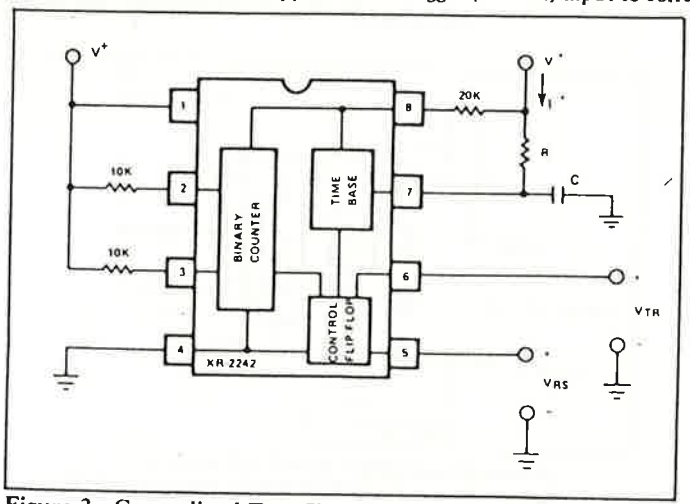


Figure 3. Generalized Test Circuit

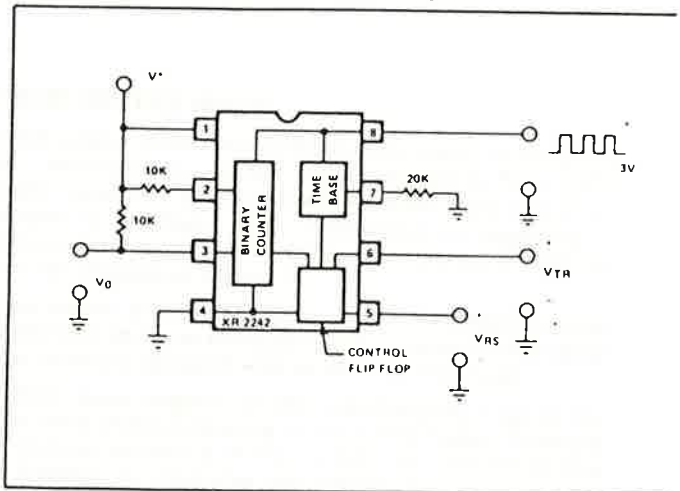


Figure 4. Test for Counter Section

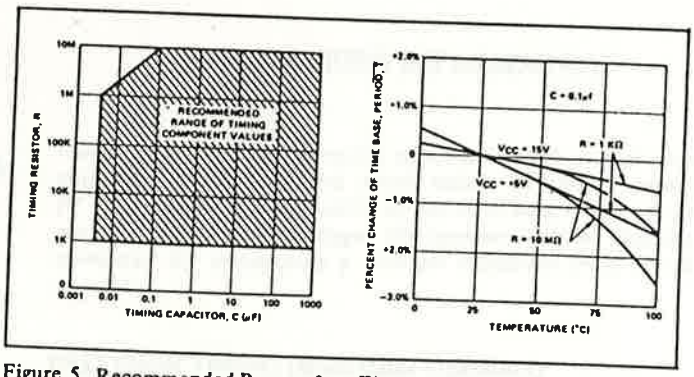


Figure 5. Recommended Range of Timing Component Values

Figure 6. Temperature Drift of Time-Base Period, T

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 2 AND 3)

The binary counter outputs are buffered "open-collector" type stages, as shown in Figure 1. Each output is capable of sinking ≈ 5 mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 7.

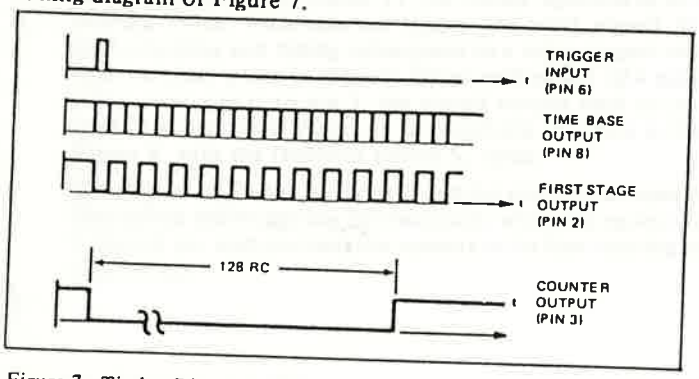


Figure 7. Timing Diagram of Output Waveforms

Basic circuit connection for timing applications is shown in Figure 8. Subsequent to a positive trigger pulse applied to pin 6, the timing output at pin 3 goes to a "low" state and will stay low for a total time duration T_O = 128 RC, where R and C are the timing components connected to pin 7. If the switch S_1 is *open*, then the output at pin 3 would alternately change state every T_O interval of time, and the circuit would operate in its "astable" mode. If the switch S_1 is *closed*, the circuit will reset itself and complete its timing cycle after a time interval of T_O, when the output at pin 3 goes to a "high" state. This corresponds to the "monostable" mode of operation.

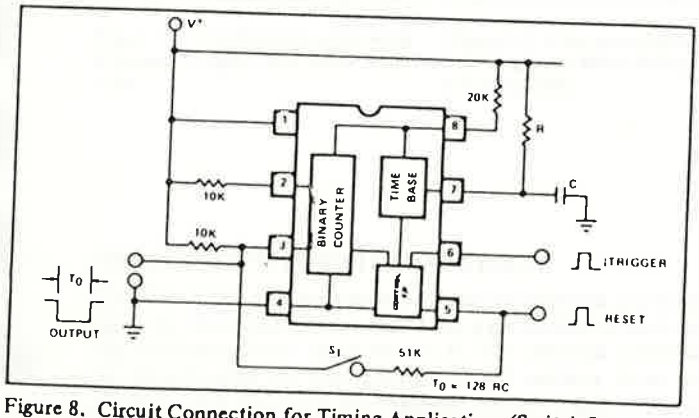


Figure 8. Circuit Connection for Timing Applications (Switch S_1 Open for Astable Operations, Closed for Monostable Operations)

RESET AND TRIGGER INPUTS (PINS 5 AND 6)

The circuit is reset or triggered with positive-going control pulses applied to pins 5 and 6. The threshold level for these controls is approximately two diode drops (≈ 1.4V) above ground.

Minimum pulse widths for reset and trigger inputs, minimum trigger delay time and minimum re-trigger delay time are shown in Figures 9 and 10. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Note: In noisy operating environment, 0.01 μF capacitors to ground are recommended from reset and trigger terminals.

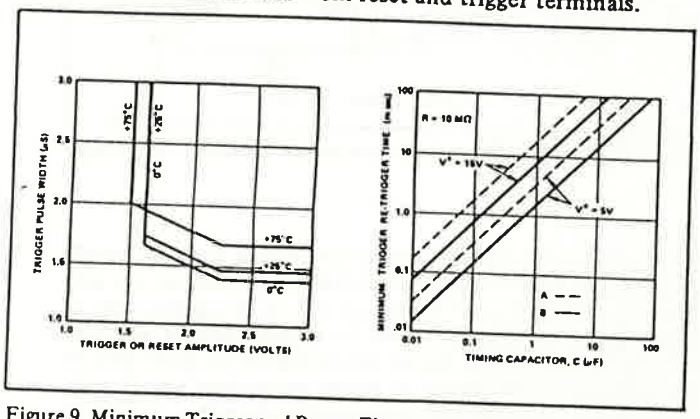


Figure 9. Minimum Trigger and Reset Pulse Widths at Pins 5 and 6

Figure 10. Trigger and Retrigger Delay Time

(A) Minimum Trigger Delay Time Subsequent to Application of Power

(B) Minimum Re-trigger Time, Subsequent to a Reset Input

When power is applied with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously, trigger overrides reset.

TIMING TERMINAL (PIN 7)

The time-base period T is determined by the external R-C network connected to this pin. When the time-base is triggered, the waveform at pin 7 is an exponential ramp with a period T = 1.0 RC.

TIME-BASE OUTPUT (PIN 8)

Time-base output is an open-collector type stage, as shown in Figure 1 and requires a 20 KΩ pull-up resistor to Pin 1 (V^+) for proper operation of the circuit. At reset state, the time-base output is at "high" state. Subsequent to triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of Figure 7.

Time-base output is internally connected to the binary counter section and also serves as the input for the external clock signal when the circuit is operated with an external time-base.

The counter input triggers on the negative-going edge of the timing or clock pulses appearing at pin 8. The trigger threshold for the counter section is ≈ +1.5 volts. The counter section can be disabled by clamping the voltage level at pin 8 to ground.

APPLICATIONS INFORMATION

Note: Under certain operating conditions such as high supply voltages ($V^+ > 7V$) and small values of timing capacitor ($C < 0.1\ \mu F$) the pulse-width of the time-base output at pin 8 may be too narrow to trigger the counter section. This can be corrected by connecting a 500 pF capacitor from pin 8 to ground.

PRECISION TIMING (Monostable Operation)

In precision timing applications, the XR-2242 is used in its monostable or "self-resetting" mode. The circuit connection for this application is shown in Figure 8, with switch S_1 closed.

ASTABLE OPERATION

The XR-2242 can be operated in its astable or free-running mode by disconnecting the reset terminal (pin 5) from the counter output (pin 3). Two typical circuit connections for this mode of operation are shown in Figures 11 and 12. In the circuit connection of Figure 11, the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 5, the circuit reverts back to its rest state. The circuit of Figure 11 is essentially the same as that of Figure 8, with the feedback switch S_1 open.

The circuit of Figure 12 is designed for continuous operation. The circuit self-triggering automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

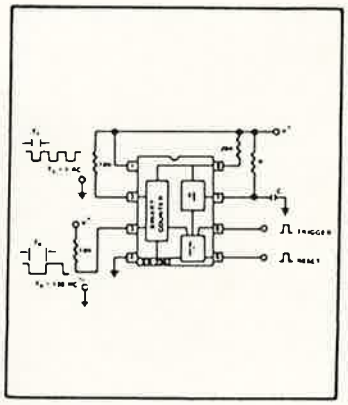


Figure 11. Astable Operation with External Trigger and Reset Controls.

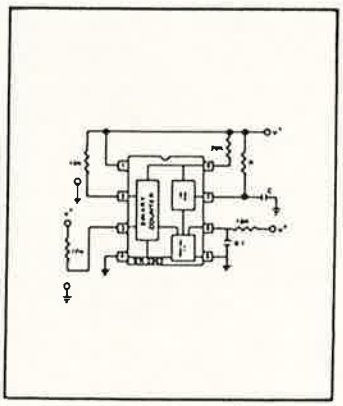


Figure 12. Free-running Operation Self-Triggered When Power Supply is Turned ON.

OPERATION WITH EXTERNAL CLOCK

The XR-2242 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 8. The internal time-base can be de-activated by connecting a 1 KΩ resistor from pin 7 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width must be $\geq 1\ \mu S$.

CASCADED OPERATION:

a) Ultra-Long Delay Generation:

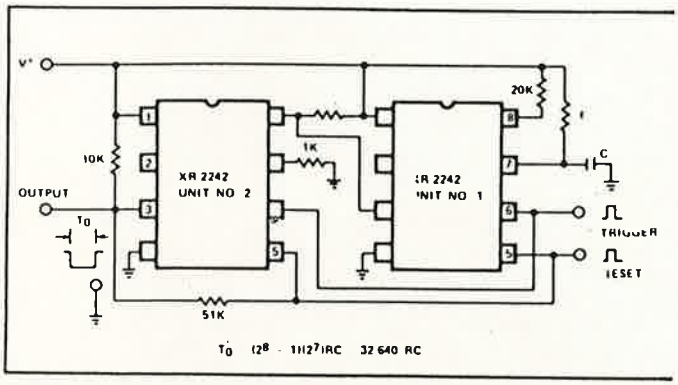


Figure 13. Cascaded Operation of Two XR-2242 Timer Circuits.

Ultra-long time delays, up to one-year duration, can be generated by cascading two XR-2242 timers as shown in Figure 13. In this configuration, the counter section of Unit 2 is cascaded with the counter output of Unit 1, to provide a total count of 32,640 clock cycles before the output (pin 3 of Unit 2) changes state. In the application circuit of Figure 13, the output (pin 3) of Unit 1 is directly connected to the time-base output (pin 8) of Unit 2, through a common pull-up resistor. In this manner, the counter section of Unit 2 is triggered every time the output of Unit 1 makes a *positive-going* transition. The time-base section of Unit 2 is disabled by connecting pin 7 of Unit 2 to ground through a 1 KΩ resistor. The reset and trigger terminals of both units are connected together for common controls.
If an additional XR-2242 were cascaded with Unit 2 of Figure 13, the total available time delay can be extended to (1.065) (10^9) RC. With an external RC = 0.1sec, this would correspond to a time delay of 3.4 years.

b) Sequential Timing:

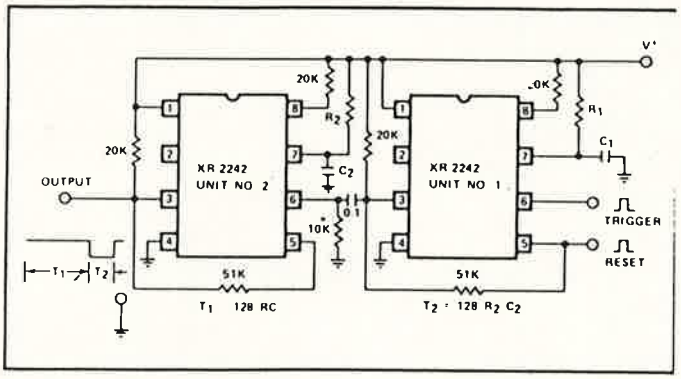


Figure 14. Sequential Timing Using Two XR-2242 Timer Circuits.

Two XR-2242 timers can be cascaded to produce sequential or delayed-timing pulses as shown in Figure 14. In this configuration, the second timer is triggered by the first timer, subsequent to the completion of its timing cycle. Thus, the triggering of Unit 2 is delayed by a time interval, T_1 (= 128 $R_1 C_1$) corresponding to the timing cycle of Unit 1.

The output of Unit 2, which is normally at "high" state will stay high for a duration of T_1 = 128 $R_1 C_1$, subsequent to the application of a trigger pulse; then go to a low state for a duration of T_2 = 128 $R_2 C_2$ corresponding to the timing interval of Unit 2; and finally revert back to its rest state after the comple- of the entire timing sequence.