

COINCIDENCE - TRIPLE 2 FOLD OVERLAP- N6237SPECIFICATIONS

Outputs are produced when coinciding signals are applied to the activated inputs.

Logic pulses are required for coincidence operation, complementary logic for anti-coincidence operation.

The individual sections can be gated by a common gate signal.

Input and output specifications apply to every individual channel:

INPUT

Number: 2

Impedance:  $50\Omega$

Reflections:

In "ON" State:  $\leq 20\%$  (capacitive)

In "OFF" State:  $\leq 20\%$  (inductive)

Voltage: Logic, -800 mV for coincidence.

Complementary logic for anti-coincidence.

Width: Minimum width or overlap (at minimum input "1" level = -600 mV) to produce outputs  $\leq 2.0$  ns

Maximum D.C.

Maximum rate:  $\geq 150$  Mc/s determined by output specifications.

OUTPUT

Number: 2 logic

2 complementary

Impedance: High, current source, unused outputs need not be terminated.

Rise and fall times: Logic:  $t_{01} \leq 1.7$  ns,  $t_{10} \leq 2.0$  ns

Complementary:  $t_{10} \leq 1.5$  ns,  $t_{01} \leq 2.0$  ns

Width: Equal to input width or overlap at minimum input "1" level (-600 mV), with the following tolerances,

Logic: -0.5 to +1.0 ns at minimum input "1" (-600 mV)

Complementary: +0 to +1.3 ns at maximum input "0" (-200 mV)

Maximum rate:  $\geq 150$  Mc/s.

Propagation delay:  $7.5 \pm 1.2$  ns (between min. input and output "1")

Feedthrough: for  $n-1 \leq \left| \frac{+}{-} 5 \right|$  mV

#### GATE

Front panel switch controlled. In position "ON" outputs are produced on the application of input signals, without the necessity of a gate signal. In position "GATED" inputs will produce outputs only if the logic level (min. -600 mV) -D.C. or pulse - is present at the gate input.

Impedance:  $50 \Omega$

Reflections:  $\leq 20\%$

Voltage: Logic, -800 mV for "ON" gating.

Complementary logic for "OFF" gating.

Width: Shortest pulse to open or close gate  $\leq 2.5$  ns at minimum input "1" level (-600 mV)

Minimum overlap with input pulses to produce output of min. output "1"  $\leq 2.5$  ns.

Maximum D.C.

Maximum Rate:  $\geq 125$  Mc/s.

Propagation Delay: Delays of INPUT and GATE are equalized up to input AND-gate.

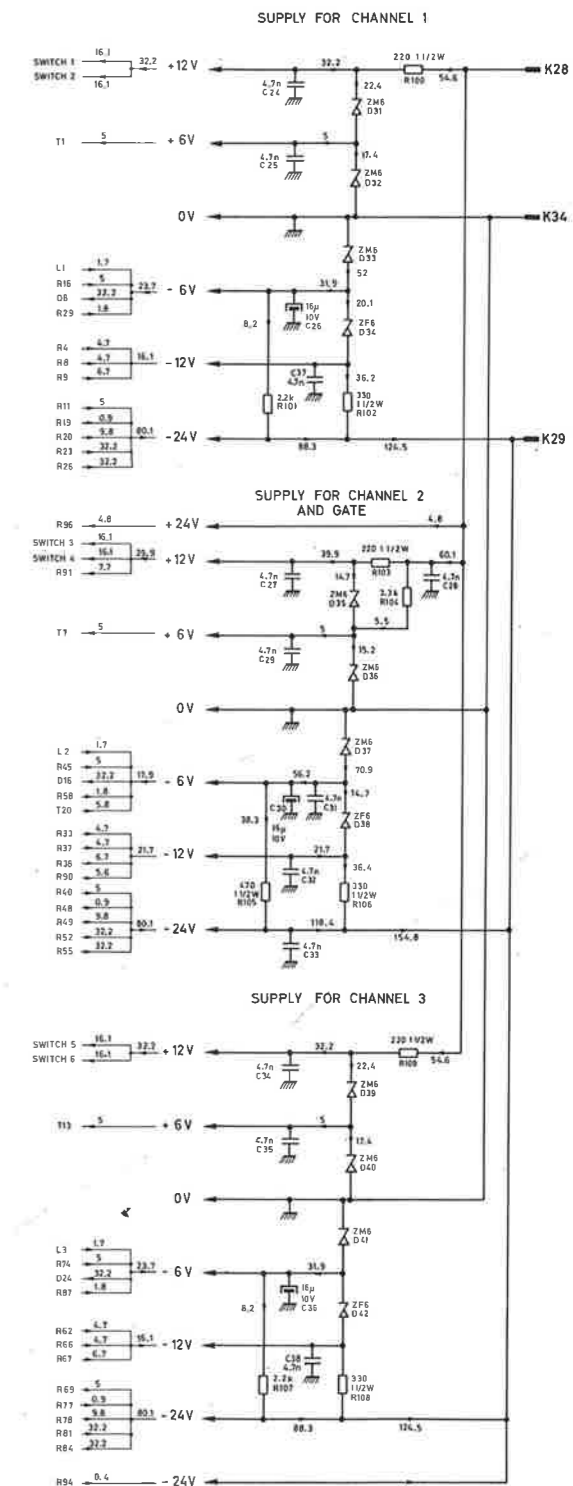
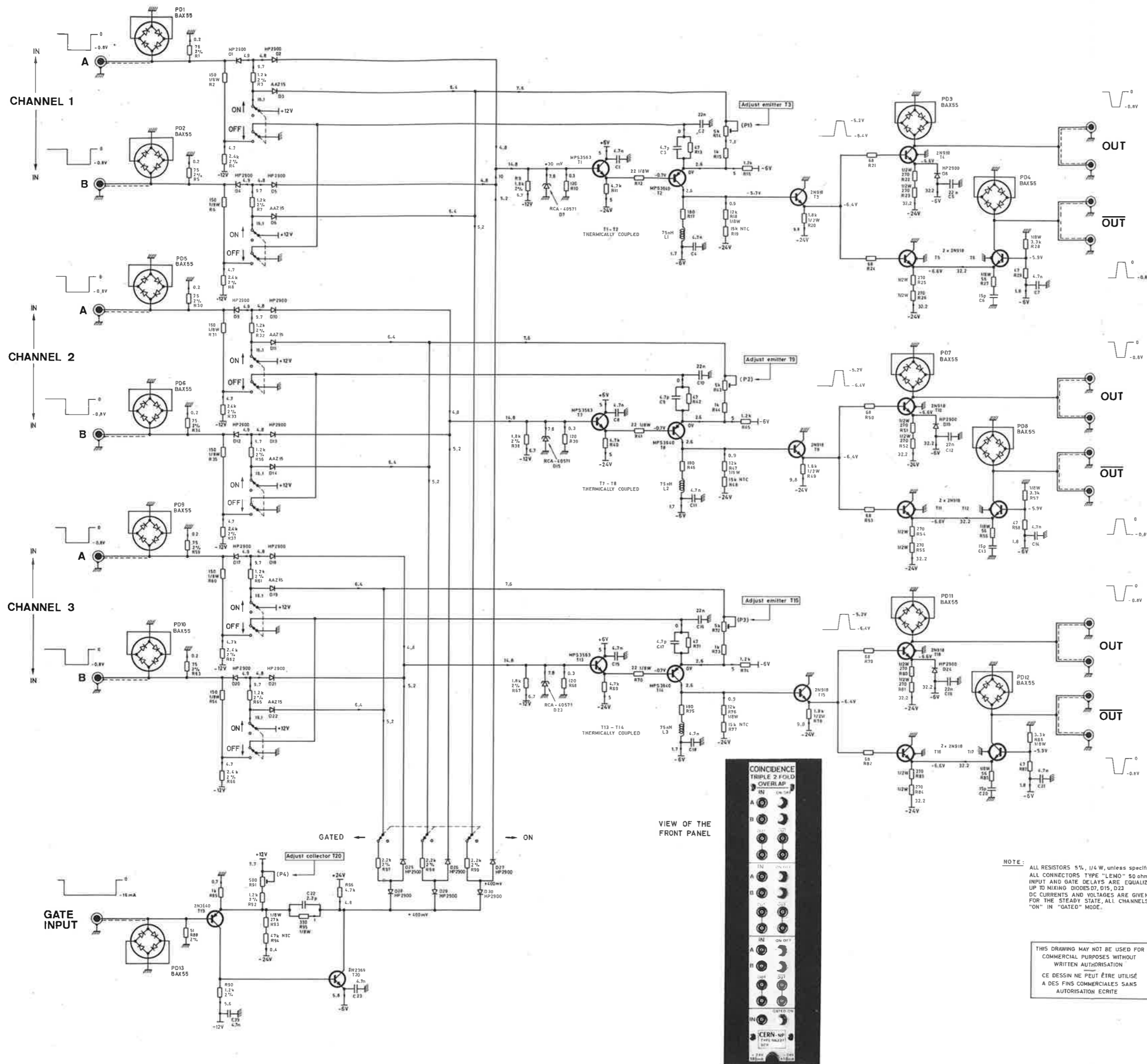
#### POWER CONSUMPTION

-24 V 410 mA  $\pm$  20 mA

+24 V 180 mA  $\pm$  10 mA

N.B. 1) Rise ( $T_{01}$ ) and fall-times ( $T_{10}$ ) are measured between maximum output "0" (-100 mV) and minimum output "1" (-700 mV)

2) All parameters have been determined with input signals having rise and fall times of 0.7 ns.



NOTE: ALL RESISTORS 5%, 1/4 W, unless specified  
ALL CONNECTORS TYPE "LEMO" 50 ohm  
INPUT AND GATE DELAYS ARE EQUALIZED  
UP TO MIXING DIODES D1, D2, D3  
DC CURRENTS AND VOLTAGES ARE GIVEN  
FOR THE STEADY STATE, ALL CHANNELS  
"ON" IN "GATED" MODE.

THIS DRAWING MAY NOT BE USED FOR  
COMMERCIAL PURPOSES WITHOUT  
WRITTEN AUTHORIZATION  
CE DESSIN NE PEUT ÊTRE UTILISÉ  
À DES FINS COMMERCIALES SANS  
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Total currents: +24V → 180mA  
-24V → 410mA