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TWO TRIPLE TWOFOLD GATED COINCIDENCE UNITS

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G E N E V A

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SUMMARY

Two coincidence units, types N6235 and N6237, are described. They both contain three independent twofold channels which can be gated by one common signal. They have been designed to operate with standard NIM[1] signal levels (-800 mV = "1", 0 mV = "0"). The two units have identical input AND-gates and gate circuitry, but they have different output facilities. The type N6235 has an output shaper and provides output signals of standard width (8.5 nsec). The type N6237 delivers output signals that have a width equal to the time overlap of the input signals. The minimum resolving time of the instruments is $\leq$ 1.5 nsec and the minimum gate width $\leq$ 2.5 nsec.

The units are part of the CERN-NIM compatible nucleonic instrument range[2].

CONTENTS

1. INTRODUCTION

Coincidence circuits[3-6] produce outputs when the activated inputs overlap in time.

A survey of recently published circuits has been given elsewhere[7].

In the present designs, the input and output circuitry has been devised to operate with signals according to the NIM/ESONE fast logic level specifications[1]. This implies that signals from photomultipliers must pass via an amplitude standardizer (limiter, shaper, discriminator, etc.) before being connected to the unit.

The resolving time is equal to the time overlap of the input pulses.

The inputs are d.c. coupled; therefore logic input pulses give coincidence operation, and complementary logic input pulses give anticoincidence or veto operation.

The modules have three independent channels; each of these has two inputs, which can be switched "ON" or "OFF" independently from the front panel.

Every channel delivers logic and complementary logic outputs. These outputs are of preset width (8.5 nsec) from the N6235 and have a width equal to the time overlap of the input signals in the case of the N6237. In both units all three channels can be gated simultaneously by a common gate input.

Functional block diagrams of the two different units are given in Figs. 1 and 2.

The input AND-gate and the common gate input circuit are nearly identical in the two units, and will therefore be discussed under the same heading. The output circuit and the performance are different and will be treated separately.

2. THE INPUT AND-GATE

As a model for the description of this gate, the top channel of the unit N6235 (see Fig. 3) will be taken.

The basic gate consists of two matched-diode current switches (D_{15}-D_{16}, etc., see Figs. 3 and 4), which feed into a tunnel diode d.c. trigger (D_{23}) [8,9]. A detailed description of this type of gate has been given in Ref. 7.

The situation shown in Fig. 4a occurs when one input (A) is switched "ON" and the common gate is disabled. Diodes D_{15} and D_{16} will be conducting $\sim$ 5 mA; D_{23} is in the low state and conducting $\sim$ 1.6 mA. A logic signal, applied to input A, will transfer the current from D_{16} into D_{15} and raise the current in the tunnel diode D_{23} by the same amount ($\sim$ 5 mA). This causes D_{23} to go to the high state and a signal will be delivered to the output circuits. When input B is set to the "ON" state, D_{23} will then be biased down by a further $\sim$ 5 mA (see Fig. 4b), and the diode will now only go to the high state during the time when the two input signals overlap.

In the absence of a pulse, a complementary logic input holds the current from D_{16} in D_{15}; thus also the current in the tunnel diode D_{23} is held high. During the pulse these currents are released, and so the tunnel diode is biased down. If complementary logic pulses are applied to one input, whilst logic pulses are connected to the other, then the tunnel diode will be in the low state when there is an overlap between the logic input pulses and the complementary logic input pulses (veto or anticoincidence).

The diode pair standardizes the current that is switched into the tunnel diode, whilst it also disconnects the input from the circuit when switched in the "OFF" state.

The input impedance consists of 75 Ω (R_{12}) in parallel with the diode current switch (D_{15}, D_{16}) and subsequent circuitry. This impedance is very non-linear but gives adequate 50 Ω matching over the signal amplitude range of interest. In the "OFF" state, a resistance of 150 Ω (R_{13}) is switched in parallel to R_{12}, so that good impedance matching is also maintained in this situation.

The diodes D_{11}, D_{12}, etc., and others in identical positions, are for input protection.

3. THE GATE INPUT CIRCUIT AND ITS COUPLING TO THE INPUT AND-GATES

The gate input circuit is common to the three channels. When the gate switch is set to the GATED position, the input AND-gate tunnel diodes D_{23}, D_{57}, and D_{91} are biased down by $\sim$ 5 mA by the currents through D_6, D_8, and D_{10} (see Fig. 4c). In this state the tunnel diodes can never go to the high state; thus no outputs can be produced, no matter what the input conditions are. A logic gate signal transfers the 5 mA from D_6 into D_5, etc., and so releases the veto. It will be clear that a complementary logic gate signal will not veto in the steady state, but only during the presence of a pulse.

When the gate is in the "ON" position, the gate circuit is disabled.

The current bias of 5 mA for each pair of gate circuit diodes (D_6, D_5 through R_6, etc.) is sent via the "ON-OFF" switches of all channels in order to avoid output signals, derived from pulses applied to the gate, in channels having all input switches in "OFF" position. Diodes D_{14}, D_{20}, etc., have been added to avoid d.c. interference between channels.

The driver in the gate circuit of the unit type N6237 (see Fig. 12) is a feedback amplifier, compared to a simple emitter follower in the unit type N6235. This feedback amplifier arrangement has a gain of 1.3 ($\approx R_{89} + R_{95}/R_{89}$). It causes the width of the output signal to follow more closely the time overlap across the AND-gate tunnel diode for gate signals with amplitudes down to the minimum input "1" (-600 mV).

4. THE UNIT WITH STANDARDIZED OUTPUTS, N6235

4.1 Discriminator and output fan-out

The complete circuit diagram and views of the unit are shown in Figs. 3 and 5. The top channel of Fig. 3 will again be taken for the description of this part of the circuit.

The signal from D_{23} drives the differentiator T_2 [10]. This differentiator shortens the effective drive to the following discriminator, so that no multiple pulsing occurs for long overlap times.

The discriminator is a slightly modified version of the trigger circuit as used in the pulse-shaper described in Ref. 10.

The signal from the differentiator T_2 drives tunnel diode D_{25} to the high state. D_{25} switches current into the tunnel diode D_{28} via the back diode D_{27}, so that also this diode goes to the high state. The current in the back diode D_{29} is transferred to the transistor T_4, producing a positive excursion at the collector of T_4.

The signal at the collector of T_4 drives the output fan-out[11], consisting of a buffer emitter follower T_6 and three transistor diode current switches (T_9-D_{33}, T_{10}-D_{37}, T_{11}-D_{41}), and one transistor-transistor current switch (T_7-T_8). The negative-going signal at the collector of T_7 is used for resetting the tunnel diode cascade via the PULSE WIDTH CABLE and T_3. The diodes D_{30}, D_{31}, D_{32} (and others in identical positions) are output clamping (when unloaded) and protection diodes.

4.2 Performance

The performance of the instrument is summarized by the specifications in Fig. 6.

In Fig. 7, examples are given of some input conditions and resulting waveforms in various points of the circuit. It is shown that the output waveform is independent of the time overlap of the input signals, and also that no output is produced when both input switches are "OFF" and the gate switch is in the position "GATED" (Fig. 7e).

The operation is, in practice, illustrated by the waveforms shown in Fig. 8. The inputs A and B are switched "ON" and the gate switch is in position "GATED". The logic input signals to A and B have a different frequency ($\sim$ 50 MHz and $\sim$ 33 MHz), so that periodically an overlap occurs. In Fig. 8a a logic gate pulse of $\sim$ 120 nsec is applied, while in Fig. 8b the complementary logic gate pulse (anti) is $\sim$ 60 nsec. The output signals are produced $\sim$ 10 nsec after the start of the time overlap of the inputs (= propagation delay).

Details of the standardized output signal (OUT and $\overline{\text{OUT}}$) at a low frequency are shown in Fig. 9. The width of this signal has been chosen to be about 8.5 nsec in the design. Other widths can be obtained by inserting different lengths of the PULSE WIDTH CABLE (see Fig. 3). The wave shape and the amplitude are independent of the number of activated inputs and their overlap. The output signal at the maximum repetition rate is given in Fig. 10; it is found to be 57 MHz for this unit, while $\geq$ 50 MHz is specified (see Fig. 6).

The minimum double pulse resolution is shown in Fig. 11; it is 400 psec in this case, and is thus well inside the specified $\leq$ 1.5 nsec.

5. THE UNIT WITH THE TIME OVERLAP OUTPUTS, N6237

5.1 Output amplifier and fan-out

The complete circuit diagram and views of the unit are shown in Figs. 12 and 13. The top channel (T_1, T_2, etc.) of the circuit (Fig. 12) will be taken for the description.

The signal from the AND-gate tunnel diode (D_7) is fed via buffer emitter follower T_1 to the amplifier T_2. The amplification of T_2 is $\sim$ 3×. This amplified signal ($\sim$ 1.3 V) is the input to the output fan-out consisting of buffer emitter follower T_3, one transistor-diode current switch (T_4, D_8), and one transistor-transistor current switch (T_5, T_6). These current switches produce outputs of logic amplitude and of a width equal to the overlap time.

When neither of the two inputs of a channel are activated (both switches in "OFF" position), then D_7 will go to the high state. This would normally cause d.c. outputs, which could be troublesome. This situation is avoided by disconnecting R_{13} from ground, thus suppressing the gain of T_2.

The package diodes PD_3 and PD_4 are output clamping (when unloaded) and protection diodes.

5.2 Performance

The performance of the instrument is summarized by the specifications in Fig. 14.

In Fig. 15 examples are again given of some input conditions and resulting waveforms in various points of the circuit. It can be noticed that the width of the output signal equals the time overlap of the input and gate signals.

The operation is further illustrated by the waveforms shown in Fig. 16. The two inputs are switched "ON", and the gate switch is in the "GATED" position. The input pulses have a different frequency, resulting in a periodic overlap. In Fig. 16a the unit is gated-on for $\sim$ 120 nsec, while in Fig. 16b it is gated-off for $\sim$ 60 nsec.

The output width, for a certain overlap of the input signals, is shown in Fig. 17. The rise- and fall-times and the amplitude (provided the overlap is $\geq$ 2.0 nsec) are independent of the number of inputs. The operation at the maximum repetition rate ($\geq$ 150 MHz) is shown in Fig. 18.

The minimum resolving-time for a double coincidence is demonstrated by Fig. 19, which happened to be 800 psec for this unit (specified $\leq$ 2.0 nsec).

6. SOME FINAL REMARKS

Both instruments have been designed to function in an environment with temperatures from 0°C to 60°C.

The results of an extensive range of tests on two units, which had been randomly selected from the production, have been described elsewhere[12,13].

In addition to the obvious applications of the units described, it may be mentioned that the type N6235 has been used as a gated shaper (also for photomultiplier pulses, provided a cable termination is present at the photomultiplier end), while the type N6237 has been used as an OR-gate (using complementary logic input signals) and for time-to-amplitude conversion by integrating its logic output signal.

REFERENCES

1) US-AEC report T.I.D.-20893 (Rev. 3), Dec. 1969.

2) H. Verweij, Proc. Int. Symposium on Nuclear Electronics, Versailles, 10-13 September 1968, Tome 1, p. 60.1 to 60.15.

3) I.A.D. Lewis and F.H. Wells, Millimicrosecond pulse techniques (Pergamon Press, London, New York, Paris, Los Angeles, 1959), p. 302.

4) J. Millman and H. Taub, Pulse, digital, and switching waveforms (McGraw-Hill Book Co., New York, 1965), p. 317.

5) R. Littauer, Pulse electronics (McGraw-Hill Book Co., New York, 1965), p. 486.

6) J.J. Samueli, J. Pignaret and A. Sarazin, Instrumentation électronique en physique nucléaire (Masson et Cie, Paris, 1968), pp. 170 and 252.

7) F. Nanni and H. Verweij, CERN 69-31 (1969).

8) See, for example, RCA Tunnel Diode Manual, TD-30 (1963), p. 44.

9) See, for example, W.F. Chow, Principles of tunnel diode circuits (John Wiley and Sons, Inc., New York, 1964), p. 212.

10) H. Verweij and G. Vismara, CERN 69-26 (1969).

11) F. Nanni and H. Verweij, CERN 68-39 (1968).

12) G. Bianchetti and B. Righini, CERN NP Internal Report 69-6 (1969).

13) B. Righini and D. Tserkezoglou, CERN NP Internal Report 70-5 (1970).

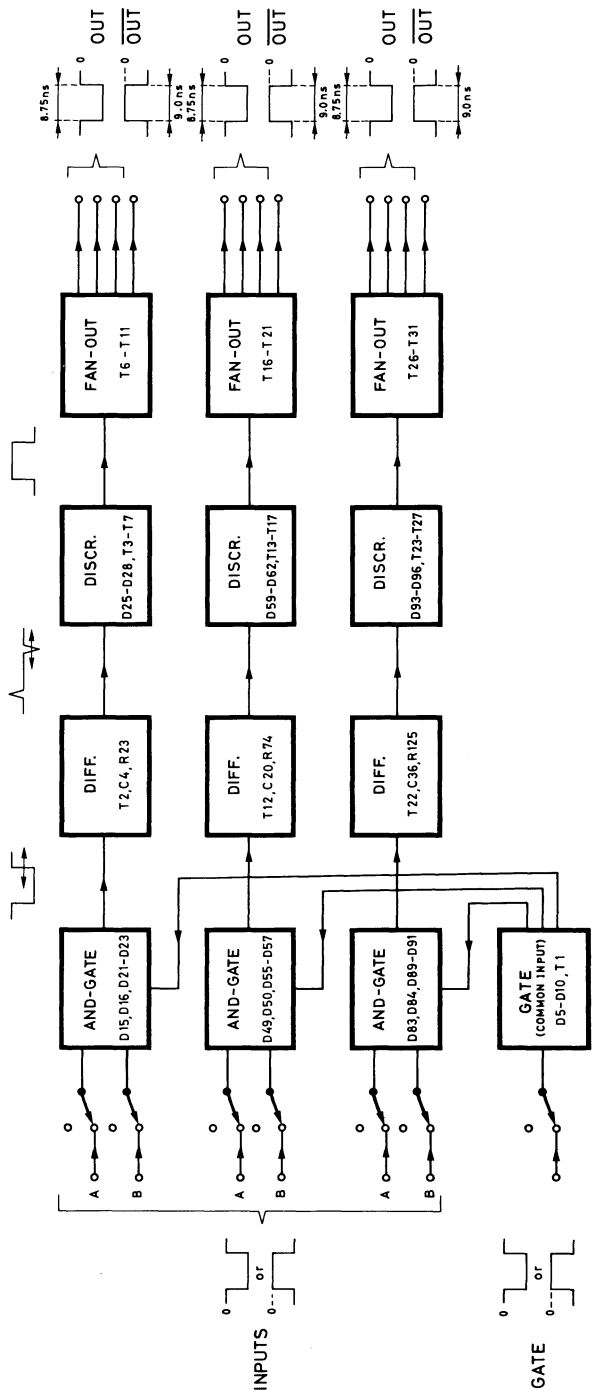


Fig. 1 Functional block diagram of the unit type N6235.

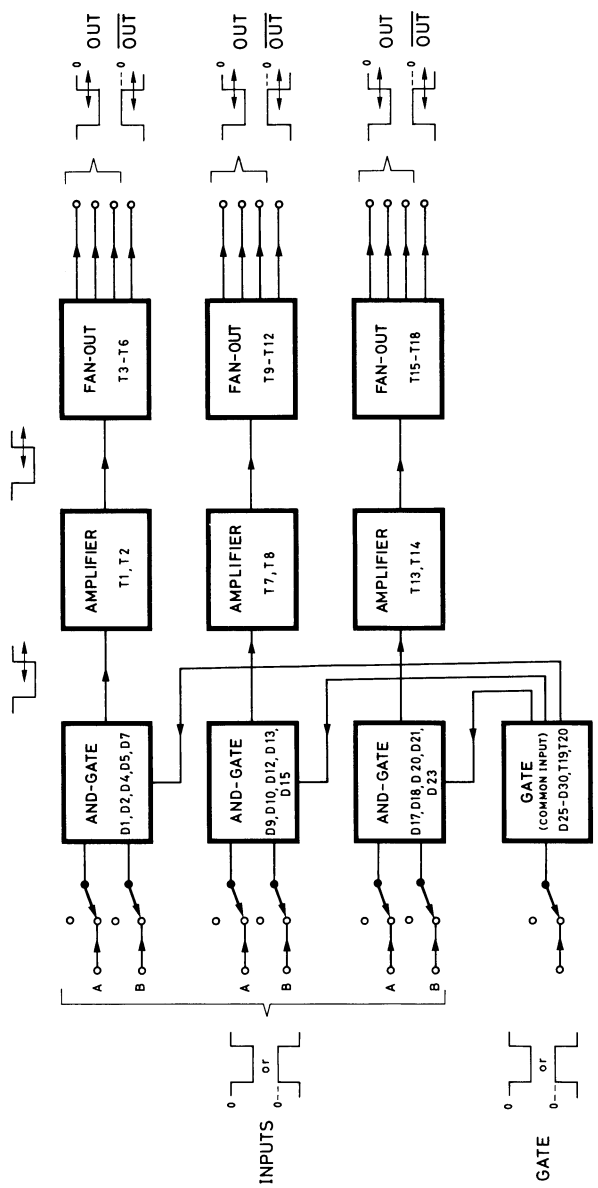


Fig. 2 Functional block diagram, type N6237.

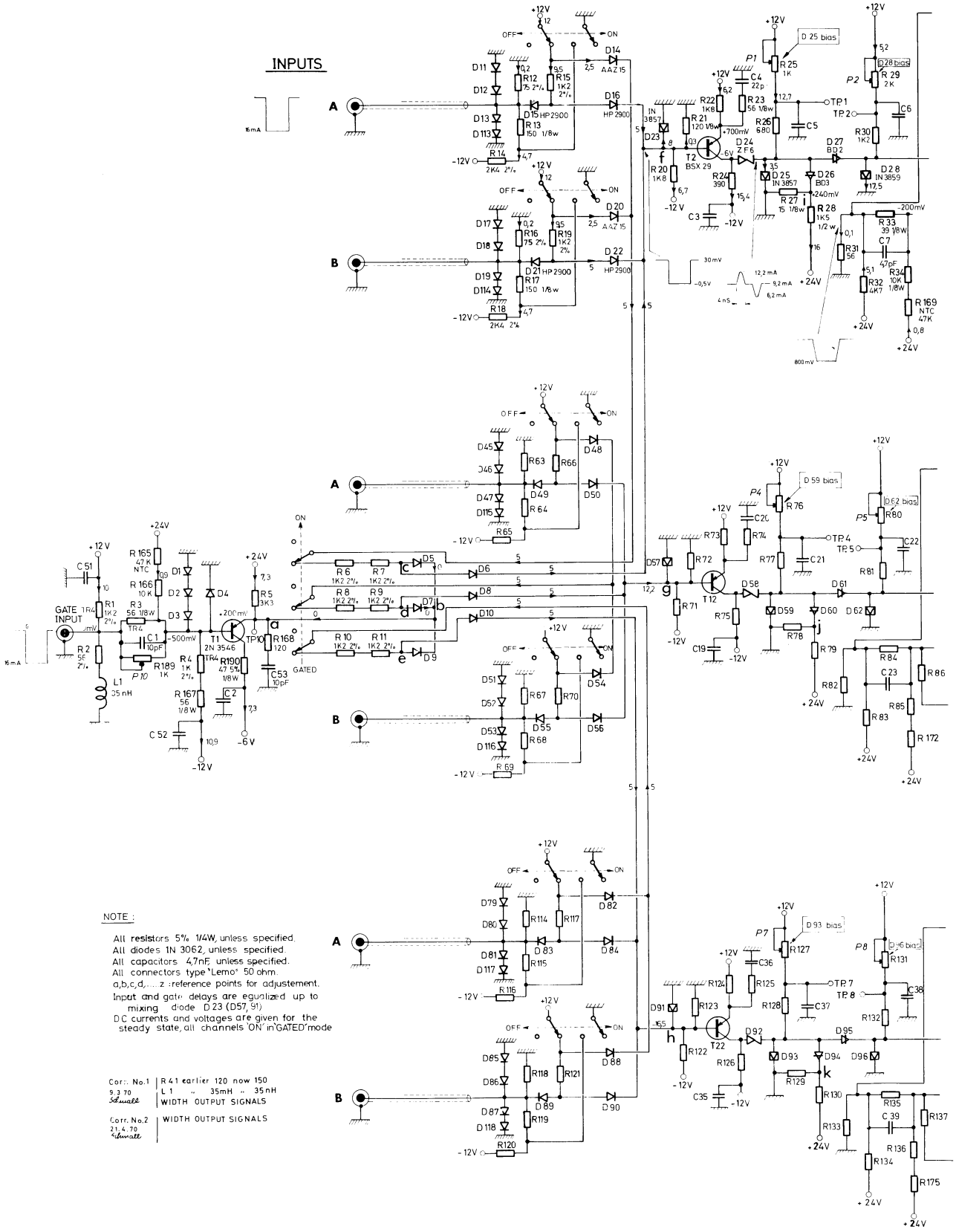
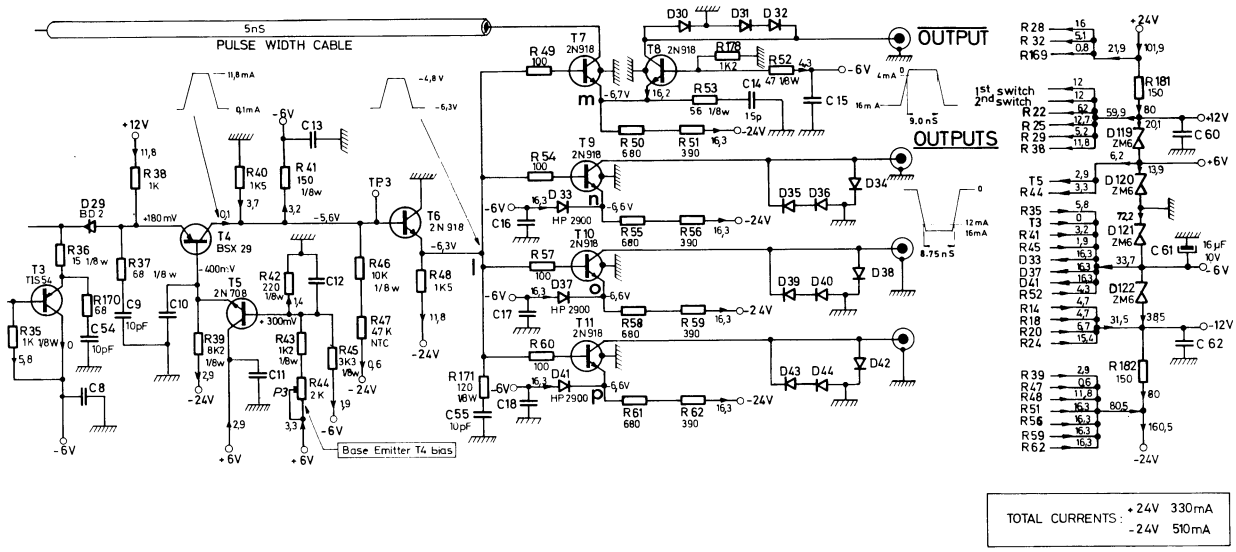
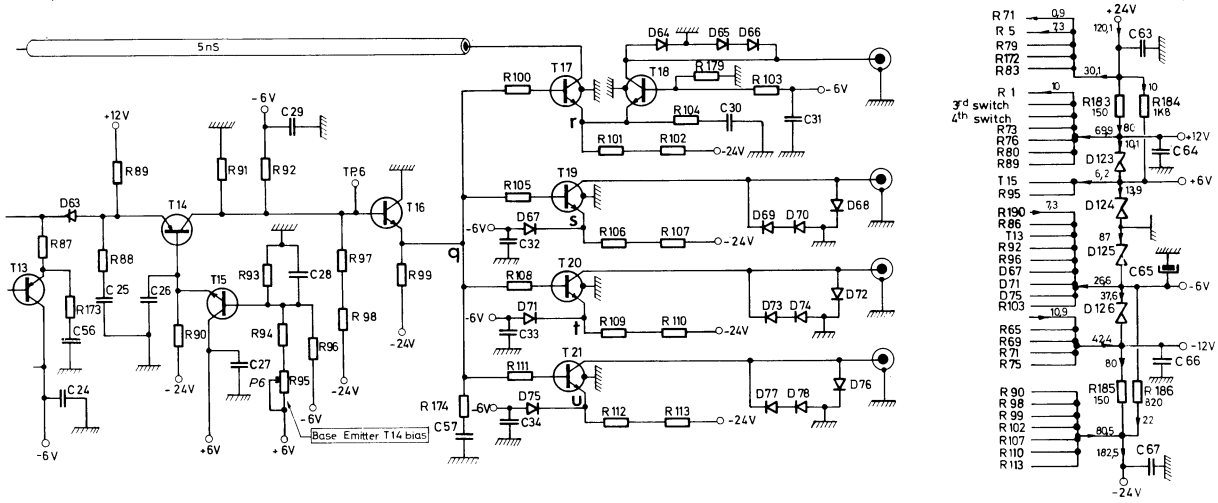
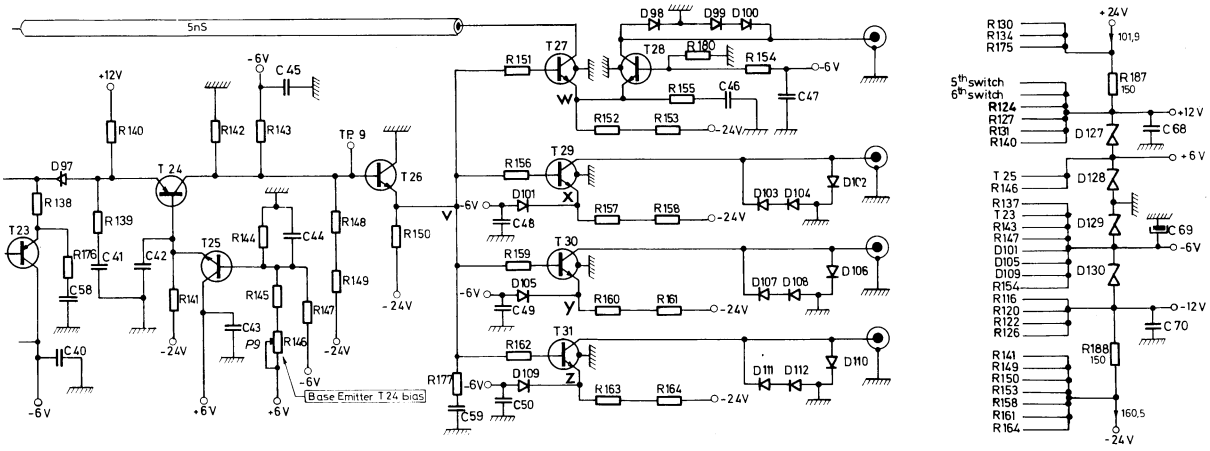
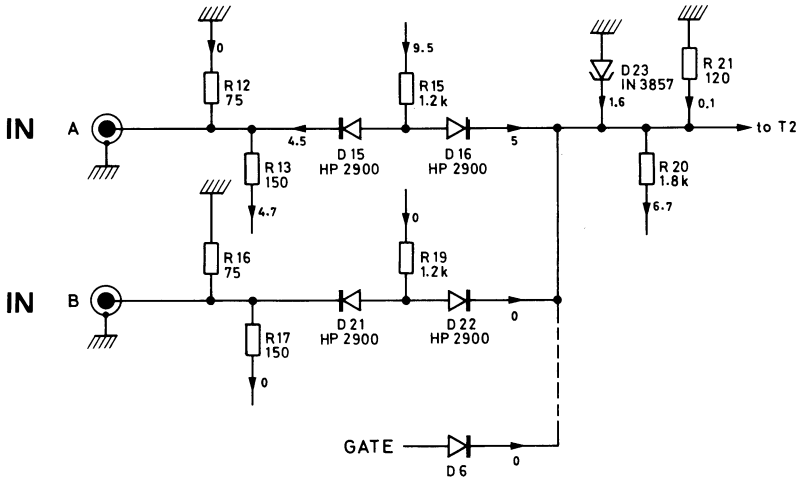


Fig. 3 Circuit diagram, type N6235.

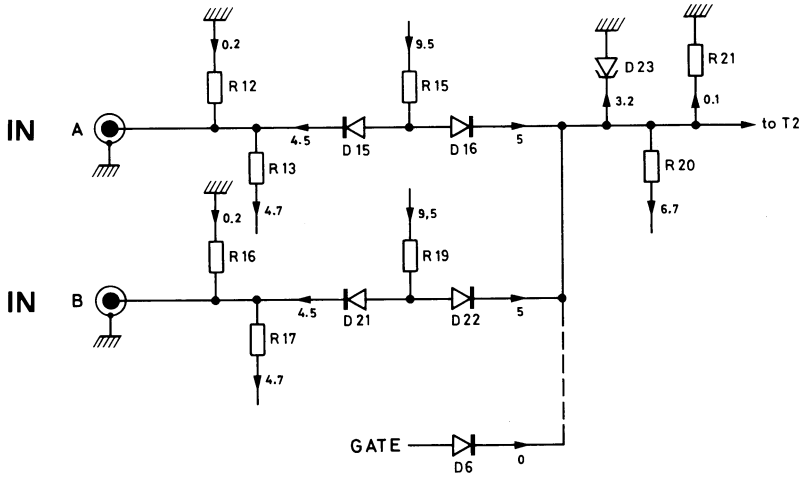

5nS
PULSE WIDTH CABLE
OUTPUT
OUTPUTS
Base Emitter T4 bias
TOTAL CURRENTS : +24V 330mA
-24V 510mA


5nS
Base Emitter T14 bias
1st switch
2nd switch
3rd switch
4th switch


5nS
Base Emitter T24 bias
5th switch
6th switch



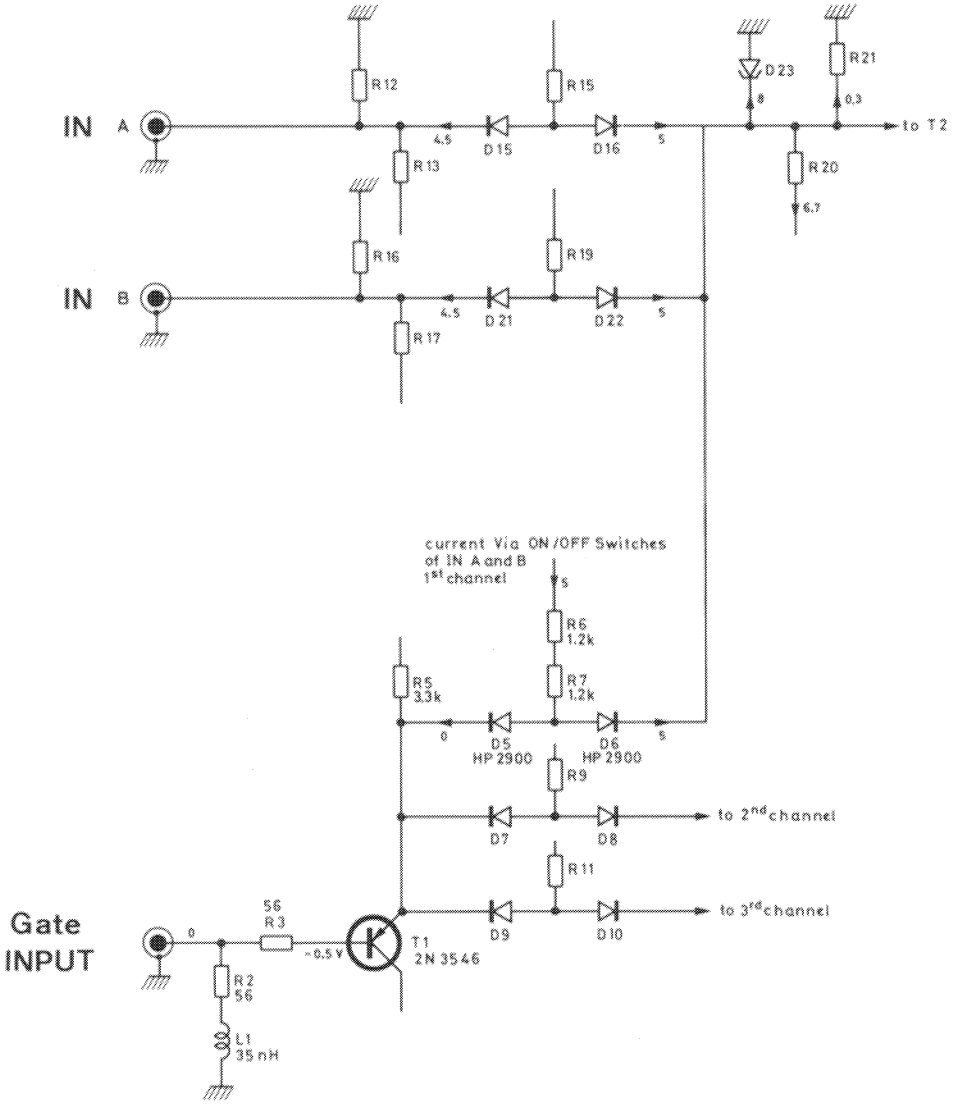
a



b

Fig. 4 The input AND-gate. (N6235 and N6237).

a) Simplified input AND-gate, one input "ON".
b) Simplified input AND-gate, two inputs "ON".



c

Fig. 4 The input AND-gate. (N6235 and N6237).
c) Simplified input AND-gate, two inputs "ON" and "GATED".

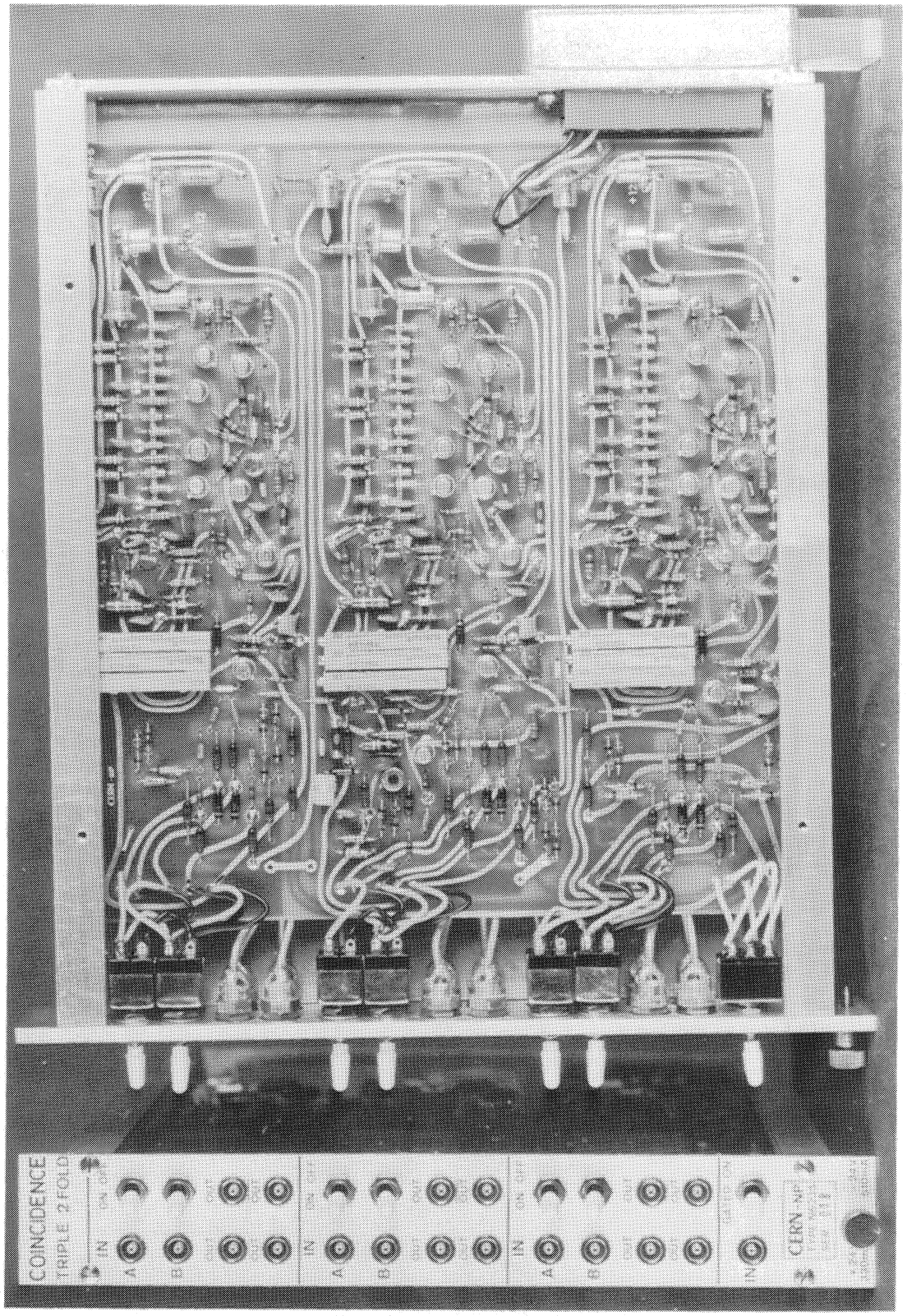


Fig. 5 View of the front panel and of the inside, type N6235.

INPUT

Number	:	2
Impedance	:	50 Ω
Reflections	:	In "ON" state : ≤ 20% (capacitive) In "OFF" state : ≤ 15% (inductive)
Voltage	:	Logic, -800 mV for coincidence Complementary logic for anticoincidence
Width	:	Minimum width or overlap (at minimum input "1" level = -12 mA) to produce outputs ≤ 1.5 nsec Maximum d.c.
Maximum rate	:	≥ 50 MHz, determined by output specifications

OUTPUT

Number	:	3 logic 1 complementary
Impedance	:	High, current source, unused outputs need not be terminated
Rise- and fall-times	:	Logic: $t_{01} \leq 1.5$ nsec, $t_{10} \leq 2.0$ nsec Complementary: $t_{10} \leq 1.5$ nsec, $t_{01} \leq 2.0$ nsec
Width	:	Logic: 8.75 ± 0.75 nsec at min. input "1" level (-12 mA) Complementary: 9.0 ± 0.75 nsec at max. input "0" level (-4 mA)
Max. rate	:	≥ 50 MHz
Propagation delay	:	10.0 ± 1.5 nsec (between min. input and output "1")

GATE

Front panel switch controlled. In position "ON", outputs are produced on the application of input signals, without the necessity of a gate signal. In position "GATED", inputs will produce outputs only if the logic level (min. -600 mV) -- d.c. or pulse -- is present at the gate input.

Impedance	:	50 Ω
Reflections	:	≤ 15%
Voltage	:	Logic, -800 mV for "ON" gating Complementary logic for "OFF" gating
Width	:	Shortest pulse to open or close gate ≤ 2.5 nsec (at minimum input "1" level -12 mA) Minimum overlap to make with inputs to produce outputs ≤ 3.5 nsec (at minimum input "1" level -12 mA) Maximum d.c.
Maximum rate	:	≥ 50 MHz determined by output specifications
Propagation delay	:	Delays of INPUT and GATE are equalized up to input AND-gate

POWER CONSUMPTION

-24 V 510 mA ± 30 mA
+24 V 330 mA ± 20 mA

N.B. 1) Rise-times (t_{01}) and fall-times (t_{10}) are measured between maximum output "0" (-100 mV) and minimum output "1" (-700 mV).

2) All parameters have been determined with input signals having rise-times and fall-times of 0.7 nsec.

Fig. 6 Specifications, type N6235.
The input and output specifications apply to every individual channel.

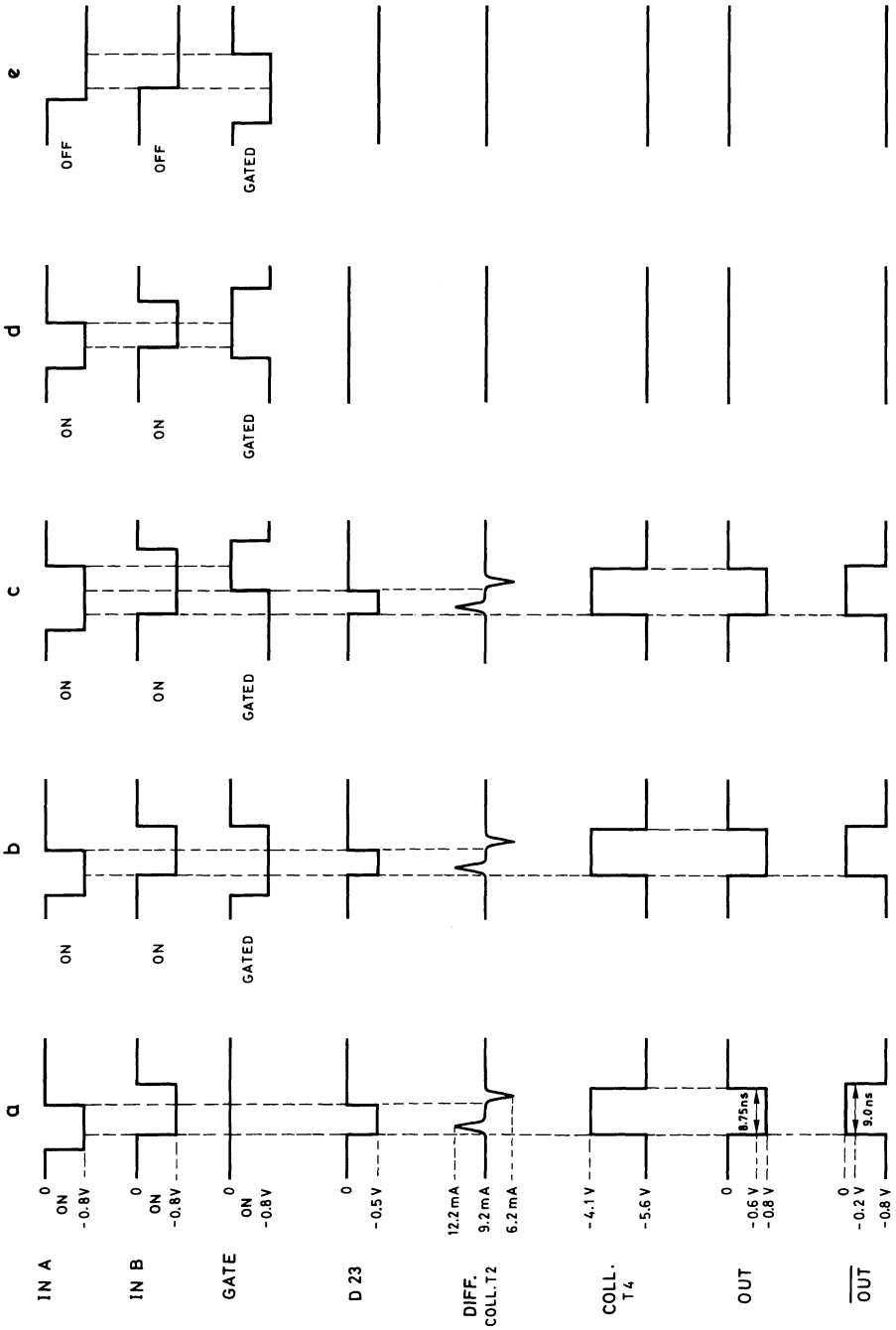


Fig. 7 Some input conditions and consequent waveforms in various points of the circuit (N6235).

a) Two logic input signals (while associated input switches in "ON" position), no gate input signal (gate switch in "ON" position).
b) Two logic input signals (switches in "ON" position) logic gate input signal (switch in "GATED" position).
c) Two logic input signals (switches in "ON" position), complementary logic gate input signal (switch in "GATED" position).
d) Like c), but now gate signal overlaps the two input signals.
e) Two logic input signals (switches in "OFF" position), logic gate input signal (switch in "GATED" position).

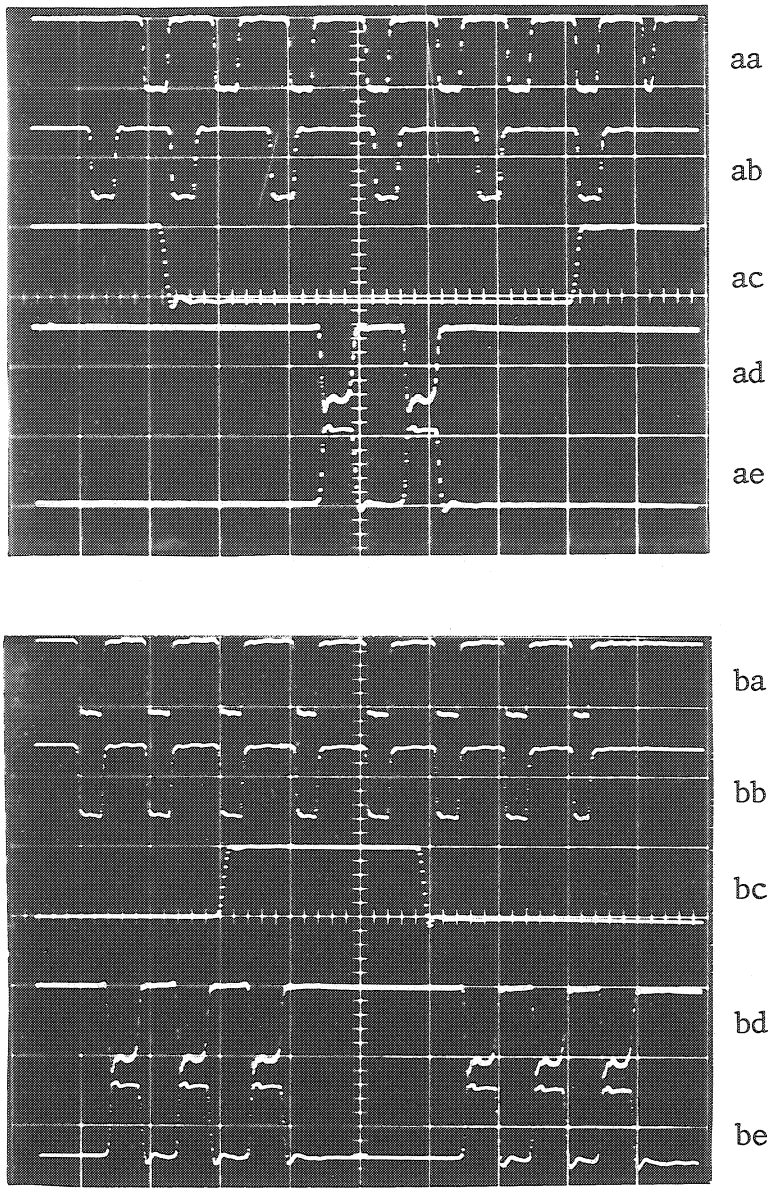


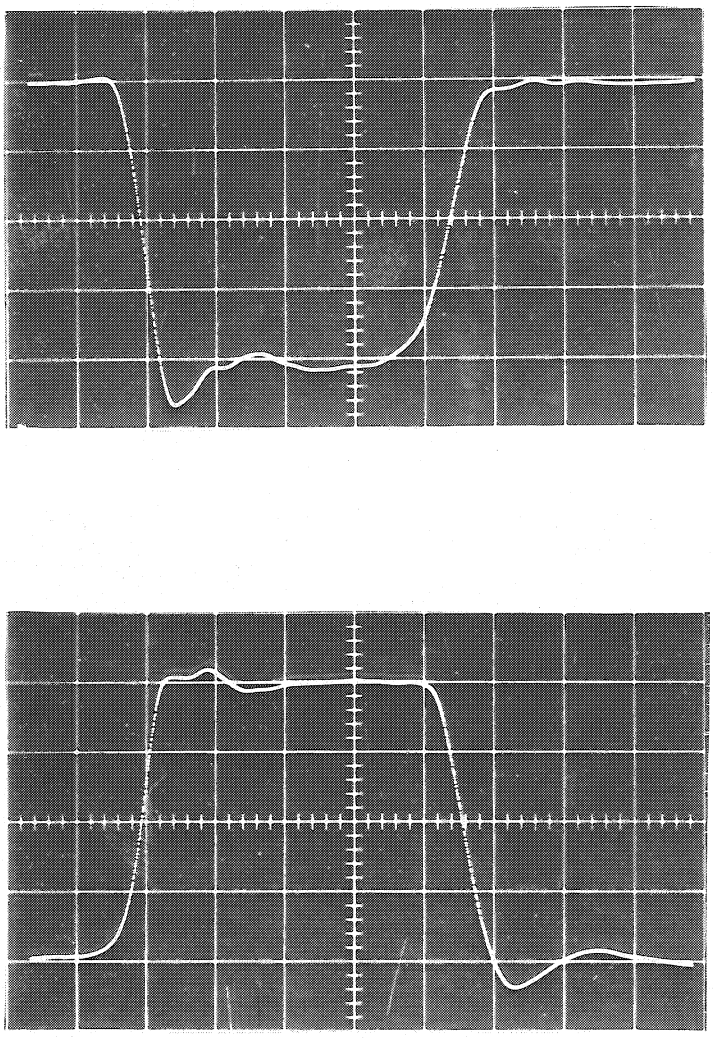
Fig. 8 Operation (N6235).

a) Two logic input signals and a logic gate signal:

aa Signal to input A.
ab Signal to input B.
ac Gate input signal.
ad Logic output.
ae Complementary logic output.

b) Two logic input signals and a complementary logic gate signal. Waveforms from same points as indicated under a).

Scale: Hor. 20 nsec/div. Vert. 800 mV/div.



a

b

Fig. 9 Output waveforms (N6235).

a) Logic.
b) Complementary logic.

Scale: Hor. 2 nsec/div. Vert. 200 mV/div.

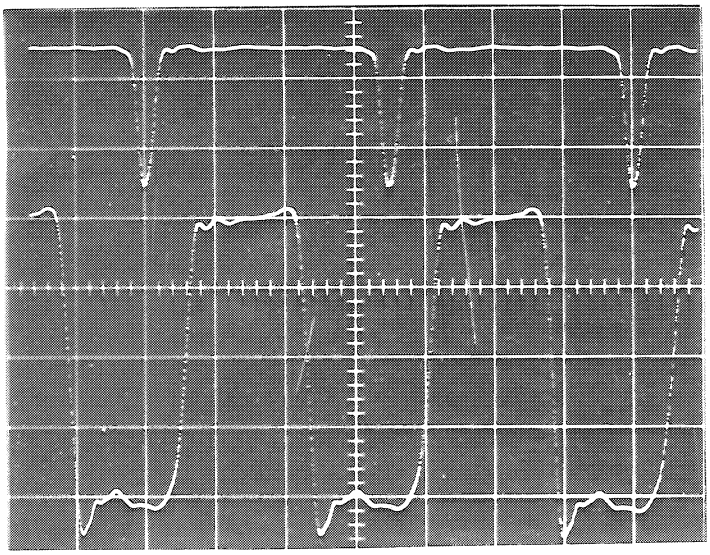


Fig. 10 Output waveform at maximum repetition rate (N6235).

a) Input signal.
b) Logic output.

Scale: Hor. 5 nsec/div. Vert. a) 400 mV/div, b) 200 mv/div.

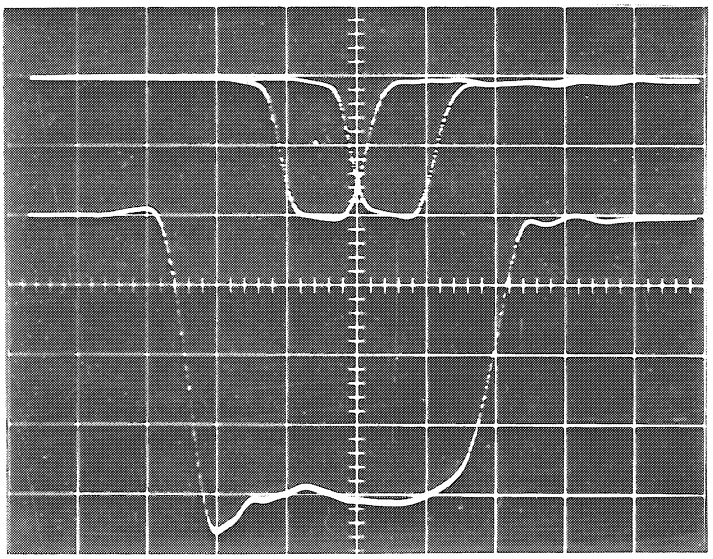
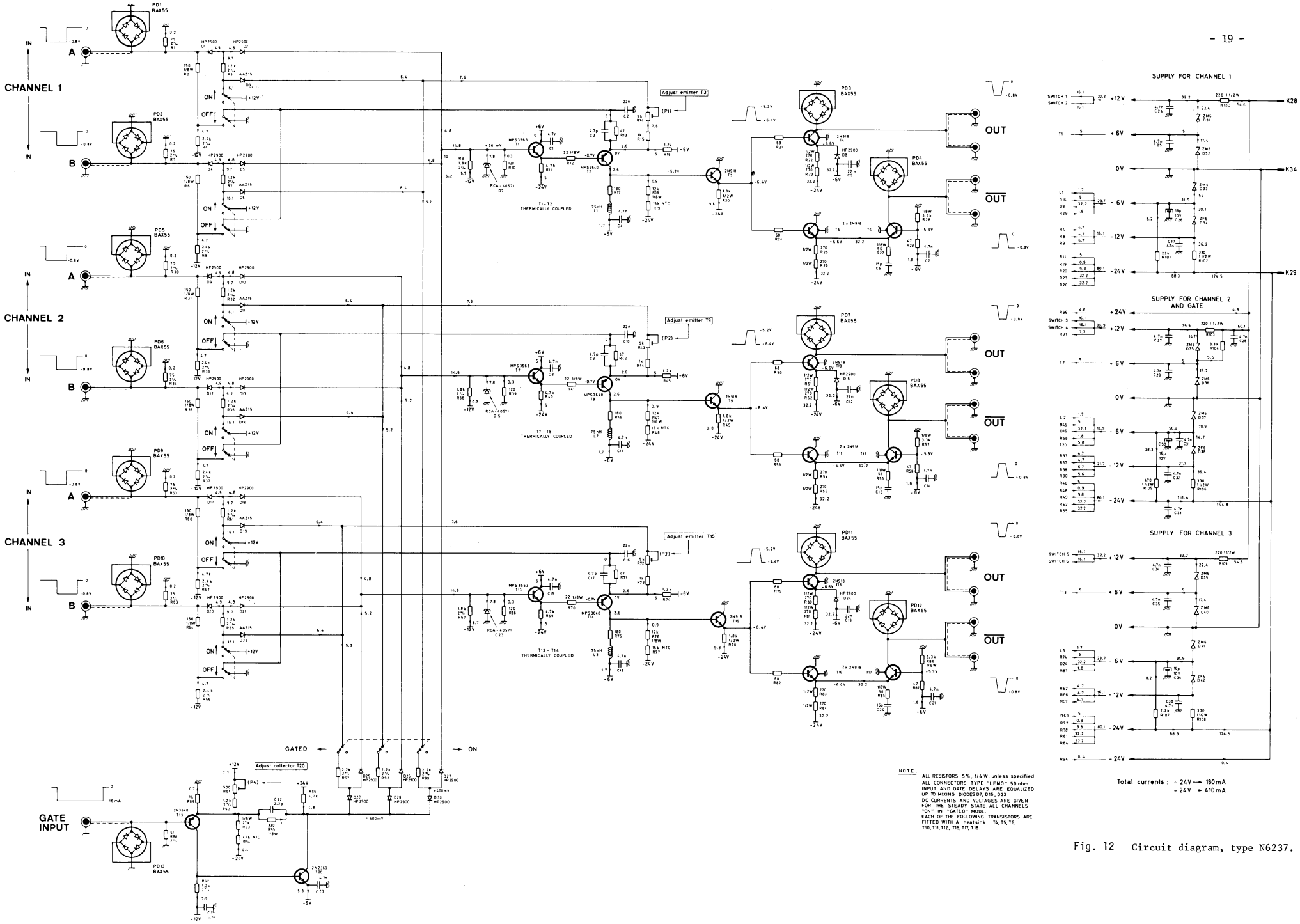


Fig. 11 Minimum double pulse resolution (N6235).

a) Two inputs with minimum overlap.
b) Output (logic).

Scale: Hor. 2 nsec/div. Vert. a) 400 mV/div, b) 200 mV/div.



NOTE:
ALL RESISTORS 5%, 1/4 W, unless specified
ALL CONNECTORS TYPE "LEMO" 50 ohm
INPUT AND GATE DELAYS ARE EQUALIZED UP TO MIXING DIODES D7, D15, D23
DC CURRENTS AND VOLTAGES ARE GIVEN FOR THE STEADY STATE. ALL CHANNELS "ON" IN "GATED" MODE
EACH OF THE FOLLOWING TRANSISTORS ARE FITTED WITH A heatsink : T4, T5, T6, T10, T11, T12, T16, T17, T18.

Fig. 12 Circuit diagram, type N6237.

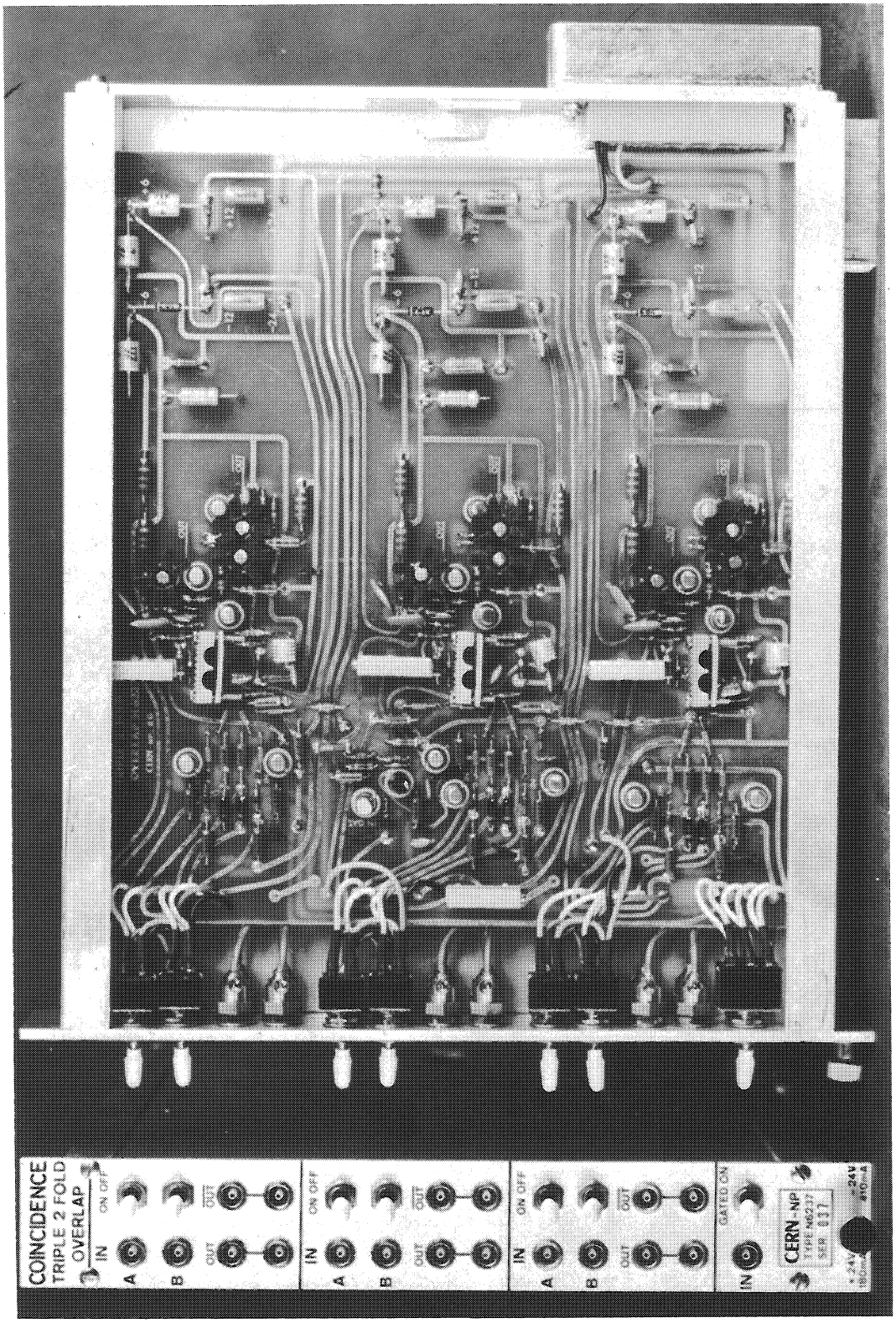


Fig. 13 View of the unit, type N6237.

INPUT

Number	:	2
Impedance	:	50 Ω
Reflections	:	In "ON" state : ≤ 20% (capacitive) In "OFF" state : ≤ 20% (inductive)
Voltage	:	Logic, -800 mV for coincidence Complementary logic for anticoincidence
Width	:	Minimum width or overlap (at minimum input "1" level = -600 mV) to produce outputs ≤ 2.0 nsec Maximum d.c.
Maximum rate	:	≥ 150 MHz determined by output specifications

OUTPUT

Number	:	2 logic 2 complementary
Impedance	:	High, current source, unused outputs need not be terminated
Rise- and fall-times	:	Logic: $t_{01} \leq 1.7$ nsec, $t_{10} \leq 2.0$ nsec Complementary: $t_{10} \leq 1.5$ nsec, $t_{01} \leq 2.0$ nsec
Width	:	Equal to input width or overlap at minimum input "1" level (-600 mV), with the following tolerances: Logic: -0.5 to +1.0 nsec at min. input "1" (-600 mV) Complementary: +0 to +1.3 nsec at maximum input "0" (-200 mV)
Maximum rate	:	≥ 150 MHz
Propagation delay	:	7.5 ± 1.2 nsec (between min. input and output "1")
Feedthrough	:	for n - 1 ≤ |±5| mV

GATE

Front panel switch controlled. In position "ON", outputs are produced on the application of input signals, without the necessity of a gate signal. In position "GATED", inputs will produce outputs only if the logic level (min. -600 mV) -- d.c. or pulse -- is present at the gate input.

Impedance	:	50 Ω
Reflections	:	≤ 20%
Voltage	:	Logic, -800 mV for "ON" gating Complementary logic for "OFF" gating
Width	:	Shortest pulse to open or close gate ≤ 2.5 nsec at minimum input "1" level (-600 mV) Minimum overlap with input pulses to produce output of min. output "1" ≤ 2.5 nsec Maximum d.c.
Maximum rate	:	≤ 125 MHz
Propagation delay	:	Delays of INPUT and GATE are equalized up to input AND-gate

POWER CONSUMPTION

-24 V 410 mA ± 20 mA
+24 V 180 mA ± 10 mA

N.B. 1) Rise- (t_{01}) and fall-times (t_{10}) are measured between maximum output "0" (-100 mV) and minimum output "1" (-700 mV).
2) All parameters have been determined with input signals having rise- and fall-times of 0.7 nsec.

Fig. 14 Specifications, type N6237.
The input and output specifications apply to every individual channel.

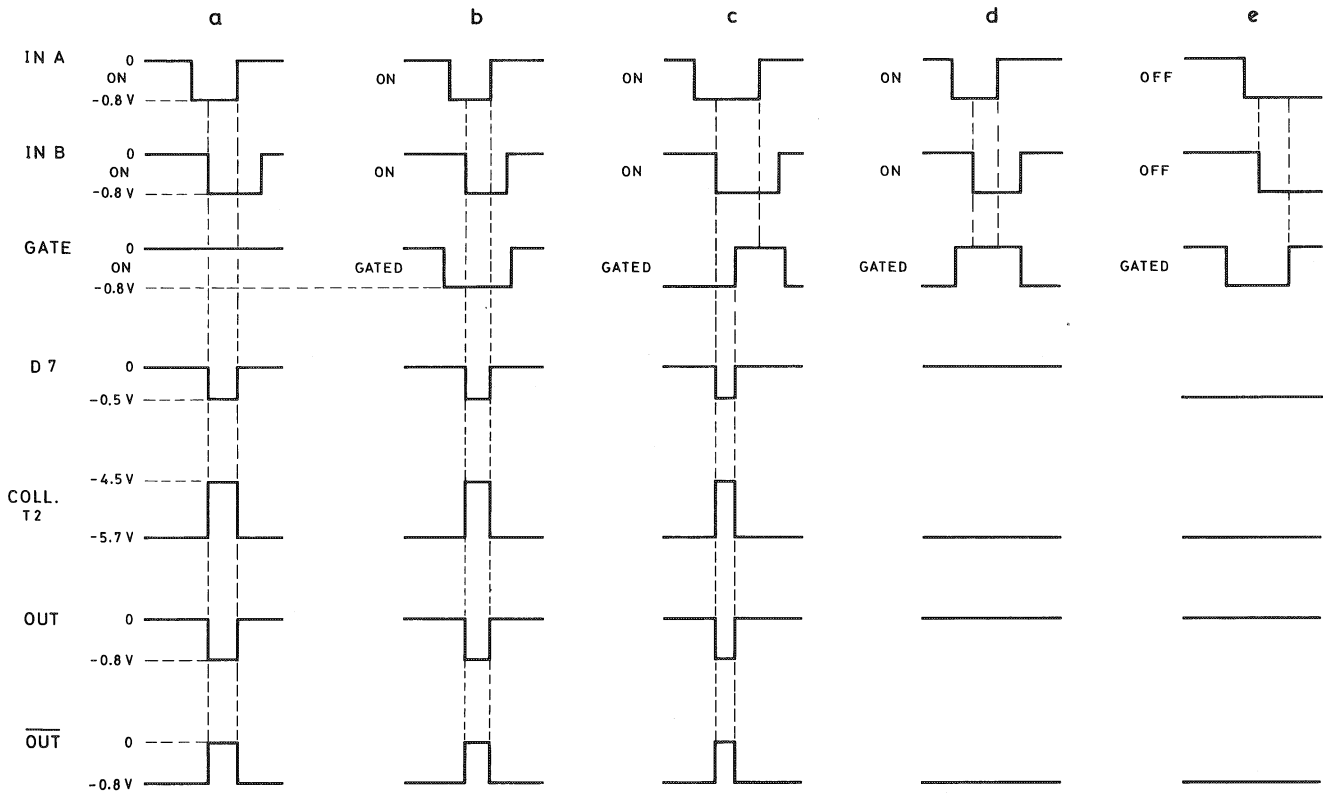


Fig. 15 Some input conditions and resulting waveforms (N6237).

a) Two logic input signals (input switches in "ON" position), no gate input signal (gate switch in "ON" position).
b) Two logic input signals (switches in "ON" position), logic gate input signal (switch in "GATED" position).
c) Two logic input signals (switches "ON"), complementary logic gate input signal (switch "GATED").
d) Like c), but now gate signal overlaps the two input signals.
e) Two logic input signals (switches "OFF"), logic gate input signal (switch "GATED").

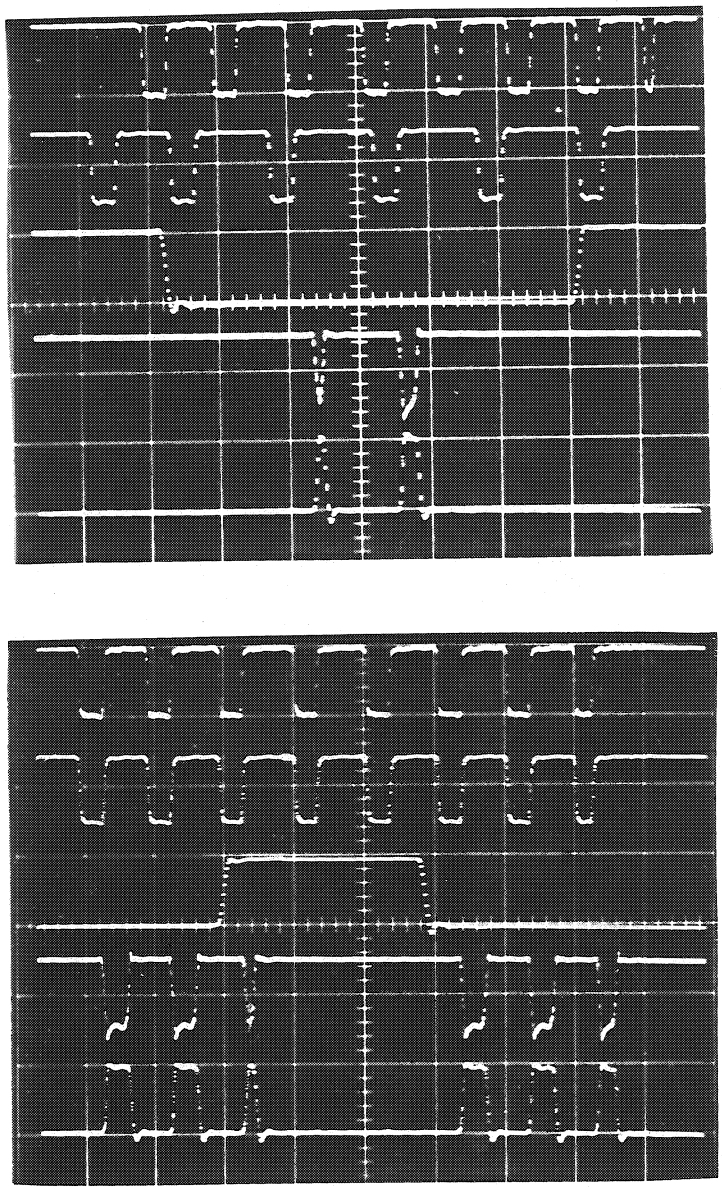


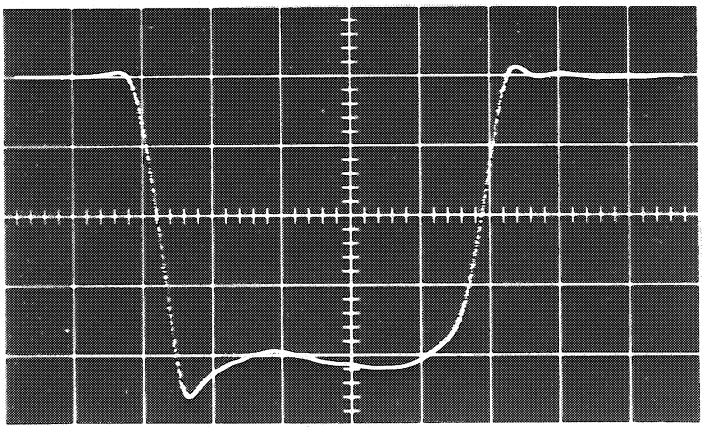
Fig. 16 Operation (N6237).

a) Two logic input signals and a logic gate signal:

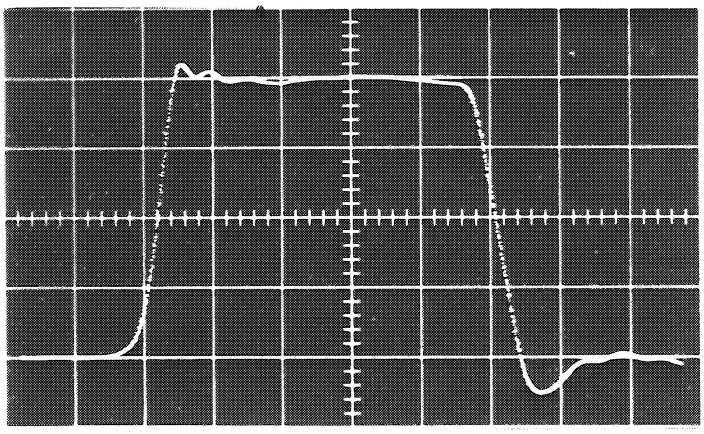
- aa Signal to input A.
- ab Signal to input B.
- ac Gate input signal.
- ad Logic output.
- ae Complementary logic output.

b) Two logic input signals and a complementary logic gate signal. Waveforms from same points as indicated under a).

Scale: Hor. 20 nsec/div. Vert. 800 mV/div.



a



b

Fig. 17 Output waveforms for a given overlap of the input signals (N6237):

a) Logic.
b) Complementary logic.

Scale: Hor. 2 nsec/div. Vert. 200 mV/div.

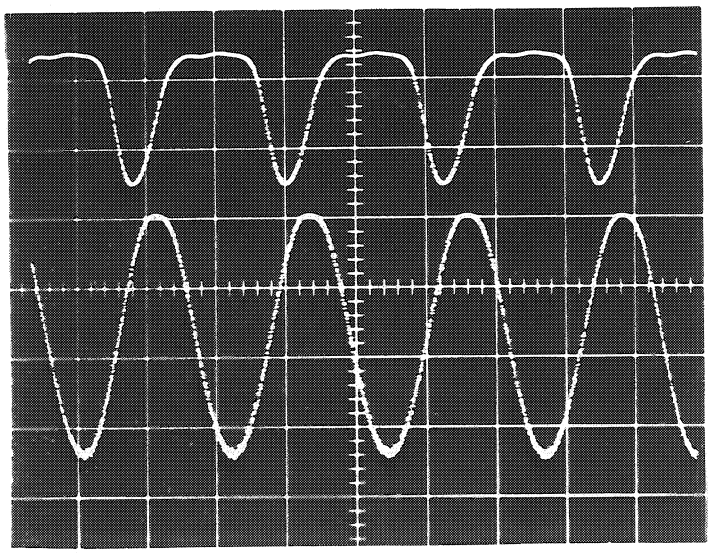


Fig. 18 Output waveform at the maximum repetition rate (N6237):

a) Input signal.
b) Logic output.

Scale: Hor. 2 nsec/div. Vert. a) 400 mV/div, b) 200 mV/div.

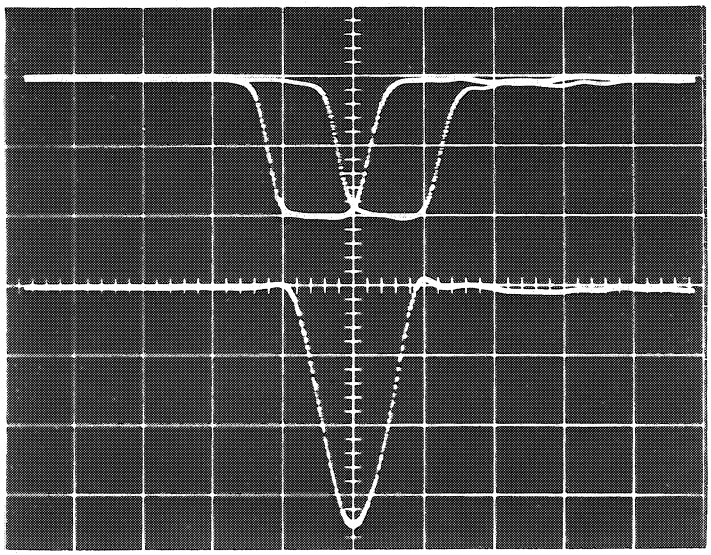


Fig. 19 Minimum double pulse resolution (N6237).

a) Two inputs with minimum overlap.
b) Output (logic).

Scale: Hor. 2 nsec/div. Vert. a) 400 mV/div, b) 200 mV/div.