

COINCIDENCE, 5 IN - 7 OUT, TYPE N6234, SPECIFICATIONS

Outputs are produced when coinciding signals are applied to the activated inputs.

Logic pulses are required for coincidence operation, complementary logic pulses for anti-coincidence operation.

INPUT

Number: 5

Impedance: 50 Ω

Reflections:

In "On" State: $\leq 20\%$, (capacitive)

In "Off" State: $\leq 15\%$, (inductive)

Voltage: Logic, - 800 mV for coincidence.

Complementary logic for anti-coincidence.

Width: Minimum width or overlap (at minimum input "1" level = - 12 mA) to produce outputs.

LIN: For singles ≤ 2.0 ns.

For 5-fold ≤ 2.0 ns.

OUT and $\overline{\text{OUT}}$: For singles ≤ 1.5 ns.

For 5-fold ≤ 1.25 ns.

Maximum Rate: Determined by output specifications.

OUTPUT

LIN: (Overlap Output)

Number: 2 logic

Impedance: High, current source, unused outputs need not be terminated.

Rise and fall time: $t_{01} \leq 1.8$ ns, $t_{10} \leq 2.0$ ns.

N6234-20A4

Width: Equal to input width or overlap at min input "1" level (- 12 mA)
+ ≤ 1.0 ns for singles,
- ≤ 1.0 ns for 5-fold

Maximum rate: ≥ 200 Mc/s

Propagation delay: 6.2 ± 0.75 ns (between min. input and output "1"),
for singles. For 5-fold it decreases by ≤ 0.5 ns.

Feedthrough: for n-1, $\leq \pm 50$ mV

OUT and $\overline{\text{OUT}}$: (Standardized output)

Number: 4 logic.

1 complementary.

Impedance: High, current source, unused outputs need not be terminated.

Rise and fall time: Logic: $t_{01} \leq 1.5$ ns, $t_{10} \leq 2.2$ ns

Complementary: $t_{10} \leq 2.0$ ns, $t_{01} \leq 2.2$ ns.

Width: Logic, 9.0 ± 1 ns at min input "1" level (- 12 mA).

Complementary, 9.0 ± 1 ns at max input "0" level (- 4 mA).

Maximum rate:

Up to a frequency of ≥ 70 Mc/s the output consists of pulses,
i.e. the level between pulses comes down inside the output "0" band.
At a frequency of ≥ 100 Mc/s the output has become D.C., when exceeding
this rate it turns into pulses again but counts will be lost.

Propagation delay: 9.5 ± 1.2 ns (between min. input and output "1"),
for singles. For 5-fold it decreases by ≤ 0.5 ns.

POWER CONSUMPTION

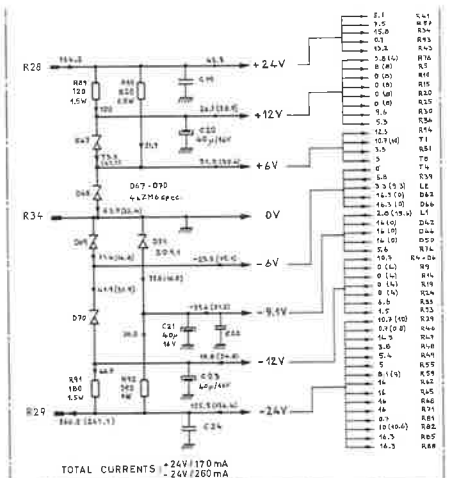
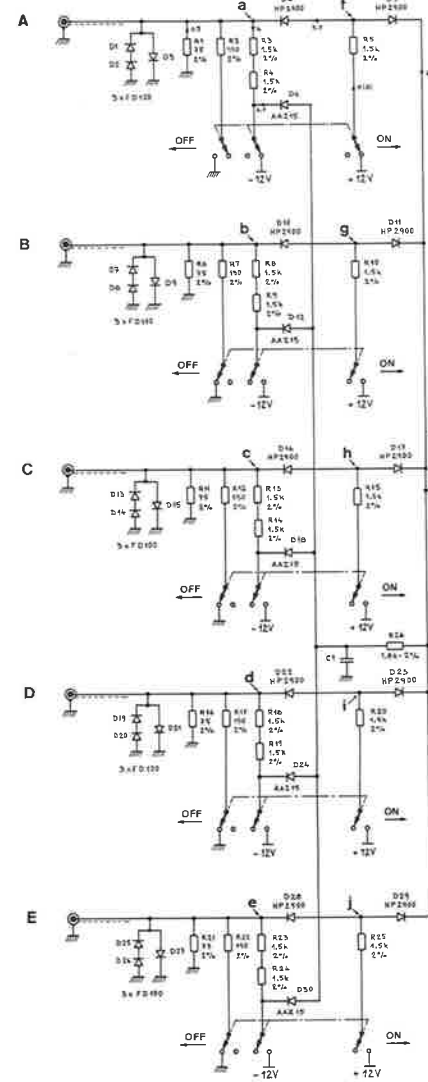
- 24 V ≤ 260 mA

+ 24 V ≤ 170 mA

- N.B.
- 1) Rise (t_{01}) and fall-times (t_{10}) are measured between maximum output "0" (- 100 mV) and minimum output "1" (- 700 mV)
 - 2) All parameters have been determined with input signals having rise and fall times of 0.7 ns

H. Verweij
F. Nanni

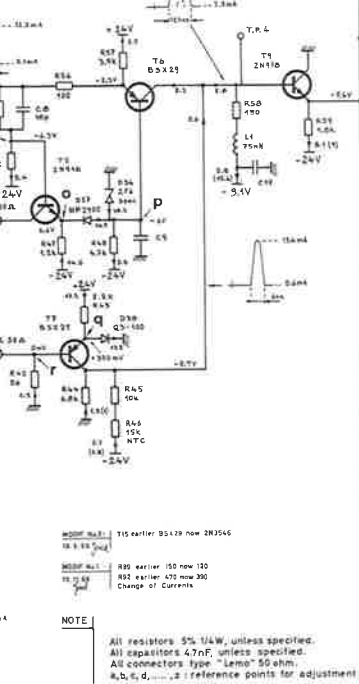
INPUTS



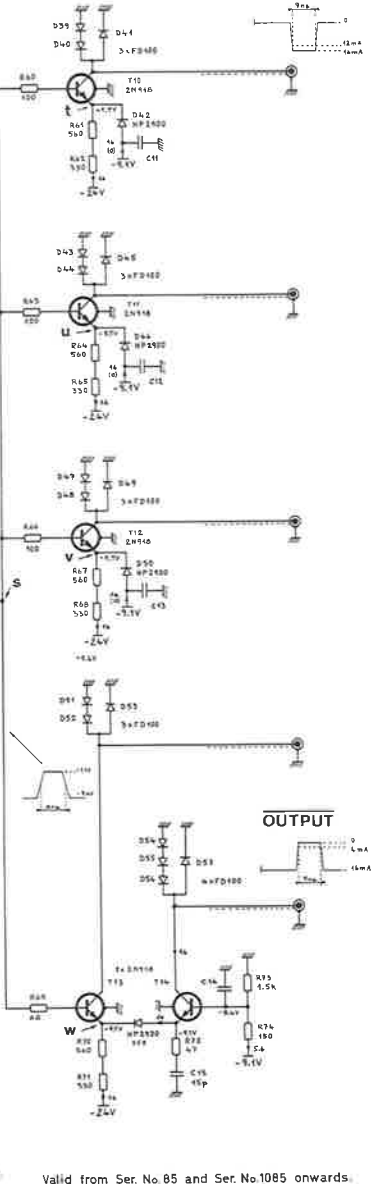
VIEW OF THE FRONT PANEL



LIN. OUTPUTS



OUTPUTS



NOTE
All resistors 5% 1/4W, unless specified.
All capacitors 47nF, unless specified.
All connectors type "Lemo" 50 ohm.
A, B, C, D, E: reference points for adjustment.
Currents in mA steady state.
1 channel "ON". Values in brackets when channels "ON", with signal present on all inputs.

Valid from Ser. No. 85 and Ser. No. 1085 onwards.

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N6234-27A1
REVISION: 1

S U M M A R Y

A coincidence unit, type N6234, is described which will process up to five independent inputs. It has been designed to operate with standard NIM¹⁾ signal levels ($-800 \text{ mV} = "1"$, $0 \text{ mV} = "0"$). A discriminator is incorporated which provides four standardized logic outputs and one standardized complementary logic output. In addition, two time overlap outputs are available. The minimum resolving time is $\leq 2.0 \text{ nsec}$. Proper functioning is guaranteed for rates up to 100 MHz via the discriminator, and up to 200 MHz via the overlap circuit. The unit is part of the CERN-NIM compatible nucleonic instrument range²⁾.

1. INTRODUCTION

Coincidence circuits³⁻⁶⁾ or AND-gates produce outputs when the activated inputs overlap in time.

A variety of these circuits have been published in recent years⁷⁻¹⁰⁾.

In the present design, the input and output circuitry has been devised to operate with signals according to the AEC/NIM/ESONE fast logic level specifications¹⁾. This implies that signals from photomultipliers must pass via an amplitude standardizer (limiter, shaper, discriminator, etc.) before being connected to the unit.

The resolving time is equal to the time overlap of the input pulses.

The input AND-gate is d.c. coupled; therefore logic input pulses give coincidence operation and complementary logic input pulses give anticoincidence or veto operation.

The unit will handle up to five inputs, which can be switched "ON" or "OFF" independently from the front panel.

Two independent coincidence overlap outputs of logic amplitude are provided and, in addition, four independent logic outputs and one complementary logic output of preset width. This preset width output has a maximum pulse duty cycle of 100%.

A close-up of the unit is given in Fig. 1, whilst a functional block diagram is shown in Fig. 2.

2. CIRCUIT DESCRIPTION

2.1 The input AND-gate

The gate consists of five matched-diode current switches (D_4 - D_5 , etc., see Fig. 3), which feed into a tunnel diode d.c. trigger (D_{31})^{19,20)}.

Assume that channel A is in the "ON" state, whilst all other channels are "OFF". Diodes D_4 and D_5 will be conducting ~ 4.0 mA, whilst D_{31} is in the low state and conducting ~ 2.2 mA (situation indicated in diagram, Fig. 3). A logic signal, applied to channel A, will transfer the current from D_5 into D_4 and raise the current in the tunnel diode D_{31} by the same amount (~ 4.0 mA). This causes D_{31} to go to the high state and a signal will be delivered to the output circuits. Every additional channel that is set to the "ON" state will bias D_{31} further down by ~ 4.0 mA, and the diode will now only go to the high state during the time when the input signals overlap.

In the absence of a pulse, a complementary logic input holds the current from D_5 in D_4 , and thus also holds the current in the tunnel diode D_{31} high. During the pulse, these currents are released and so the tunnel diode is biased down. If complementary logic pulses are applied to one or more inputs, whilst to some others logic pulses are connected, then the tunnel diode will be in the low state when there exists an overlap between the logic input pulses and any of the complementary logic input pulses.

In Fig. 4 examples are given of some input conditions and resulting waveforms in various points of the circuit.

The diode pair standardizes the current that is switched into the tunnel diode, whilst it also disconnects the input from the circuit when switched in the "OFF" state.

The diodes are hot carrier diodes with very short reverse recovery-time²¹⁾. They considerably improve the fan-in properties of the gate.

A more detailed understanding of the operation can be obtained from Fig. 5, in which the tunnel diode characteristic of D_{31} with a number of loadlines has been drawn. These loadlines are determined by calculating the current that is absorbed by R_{27} and the input circuit(s) as function of the voltage across tunnel diode D_{31} . The equivalent circuit, which has been used for this calculation, is given in Fig. 6. (The small difference between the indicated diode currents in Fig. 3 and Fig. 6 is caused by the fact that in Fig. 3 nothing is connected to the input A, while in Fig. 6 a generator with 50Ω source impedance is connected.) P_1, P_2, P_3, P_4, P_5 (Fig. 5) are steady-state operating points or intermediate operating points when the input signals at the activated inputs do not coincide. All loadlines converge in point L_0 , which represents the theoretical case where the voltage across D_{31} has gone so far positive that the current in D_5 and equivalent has been cut. When coinciding logic input signals are present at the activated inputs, the operating point is H , and all loadlines will move to the right (by $800 + 4 \times 30 = 920$ mV) such that the converging point is now L_1 .

The bias current of D_{31} (through R_{26}) passes via the ON/OFF switches. If all channels are "OFF" then D_{31} does not have any bias current, so that it will stay in the low-state and thus the outputs will stay at the steady-state level. (The logic outputs at "0" level and the complementary logic output at "1" level.)

The input impedance consists of 75Ω (R_1) in parallel with the diode current switch (D_4, D_5) and subsequent circuitry. This impedance is very non-linear but gives adequate 50Ω matching over the signal amplitude range of interest. In the "OFF" state, a resistance of 150Ω (R_2) is switched in parallel to R_1 so that good impedance matching is also maintained in that situation.

The diodes D_1, D_2, D_3 and others in identical positions are input protection diodes.

2.2 The overlap output channel

The signal from the AND-gate tunnel diode (D_{31}) is fed, via buffer emitter follower T_1 , to the amplifier T_{15} . The amplification of T_{15} is $\sim 2\times$. This amplified signal (~ 1.0 V) is the input to the output fan-out²²⁾, which consists of two transistor-diode current switches ($T_{17}-D_{62}, T_{18}-D_{66}$). These current switches produce outputs of logic amplitude and of a width equal to the overlap time.

The diodes D_{59}, D_{60}, D_{61} , and D_{63}, D_{64}, D_{65} , are output clamping (when unloaded) and protection diodes.

2.3 The discriminator output channel

The signal from emitter follower T_1 also drives the differentiator T_2 ²³⁾. This differentiator shortens the effective drive to the following discriminator, so that no multiple pulsing occurs for long overlap times.

The discriminator is a modified version of the trigger circuit as used in the pulse-shaper described in Ref. 23. The difference lies in the way the reset signal is derived and also the maximum output pulse duty cycle has been made 100% (a trigger circuit with this output property is sometimes erroneously said to be dead-timeless).

The signal from the differentiator T_2 drives tunnel diode D_{34} to the high state. D_{34} switches current into tunnel diode D_{35} via back diode D_{33} so that also this diode goes to the high state. The current in back diode D_{72} is transferred to transistor T_3 , producing a positive excursion at the collector of T_3 , the base of T_5 , and the collector of T_6 .

The positive signal at the base of T_5 transfers the current from D_{37} into T_5 causing a negative excursion at the collector of T_5 . This information is sent to the base of T_4 , via the 1 nsec timing cable, where it turns on T_4 which resets D_{35} and D_{34} . T_3 and T_5 are then cut off, whilst the first positive excursion at the collector of T_6 ends.

The reset signal on the base of T_4 is transmitted, via 1.5 nsec delay, to the base of T_7 . This will turn on this transistor, and a positive current pulse is added to the disappearing original positive excursion at the collector of T_6 (D_{35} has been reset). The duration of this second pulse covers the dead-time (= reset loop propagation delay) of the trigger circuit, thus covering the period during which T_4 holds down D_{35} , which means that the maximum obtainable pulse duty cycle in the collector of T_6 has become 100% (see Fig. 4); the resolving time of the trigger circuit has not, however, been affected.

The signal at the collector of the T_6 drives the output fan-out²²⁾, consisting of buffer emitter follower T_9 and three transistor-diode-current switches (T_{10} - D_{42} , T_{11} - D_{46} , T_{12} - D_{50}), and one transistor-diode-transistor current switch (T_{13} - D_{58} - T_{14}). The diodes D_{39} , D_{40} , D_{41} (and others in identical positions) are output protection and clamping diodes.

3. PERFORMANCE

The performance of the instrument is summarized by the specifications as outlined in Fig. 7.

The operation is illustrated by the waveforms shown in Fig. 8. Two channels are switched on. The inputs to the two channels have a slightly different frequency, so that periodically an overlap occurs.

Details of the standardized output signal (\overline{OUT} and \overline{OUT}) at a low frequency are shown in Fig. 9. The width of this signal has been chosen to be 9.0 nsec in the design. Other widths can be obtained by inserting different lengths of the "timing" and "delay" cables (see Fig. 3). The signal is independent of the number of activated inputs and their overlap. The output signal at the maximum "pulse rate" (see Fig. 7) is given in Fig. 10a (77 MHz for this unit). In Fig. 10b the unit is operating at a frequency corresponding to the maximum duty cycle (110 MHz for this unit; the baseline of the oscilloscope is at one division from the top for Fig. 10b).

The overlap output (LIN) is shown in Fig. 11 for a single input and for a double coincidence. The width, basically equal to the input width or overlap time, decreases somewhat with the number of inputs (see Specs. Fig. 7). The rise-time, the fall-time, and the amplitude (provided the overlap is ≥ 2.0 nsec) are independent of the number of inputs. The operation at the maximum repetition rate (≥ 200 MHz) is shown in Fig. 12.

The minimum resolving-time for a double coincidence via the overlap output is demonstrated by Fig. 13, which is 1.25 nsec for this unit (specified ≤ 2.0 nsec).

Timing curves obtained in a recent experiment²⁴⁾, using the set-up of Fig. 14, are shown in Fig. 15. The curves exhibit flat tops and steep skirt slopes. The slopes change very little with the number of coincident inputs, thus proving the good operation of the system. The steepness of these slopes is determined by the scintillator and photomultiplier time dispersion, the time slewing in the shapers, and the noise in the photomultiplier, the shaper, and the coincidence unit.

The instrument has been designed to operate over the ambient temperature range 0-60°C.

The results of an extensive series of tests on two randomly selected production units are described elsewhere²⁵⁾.

* * *

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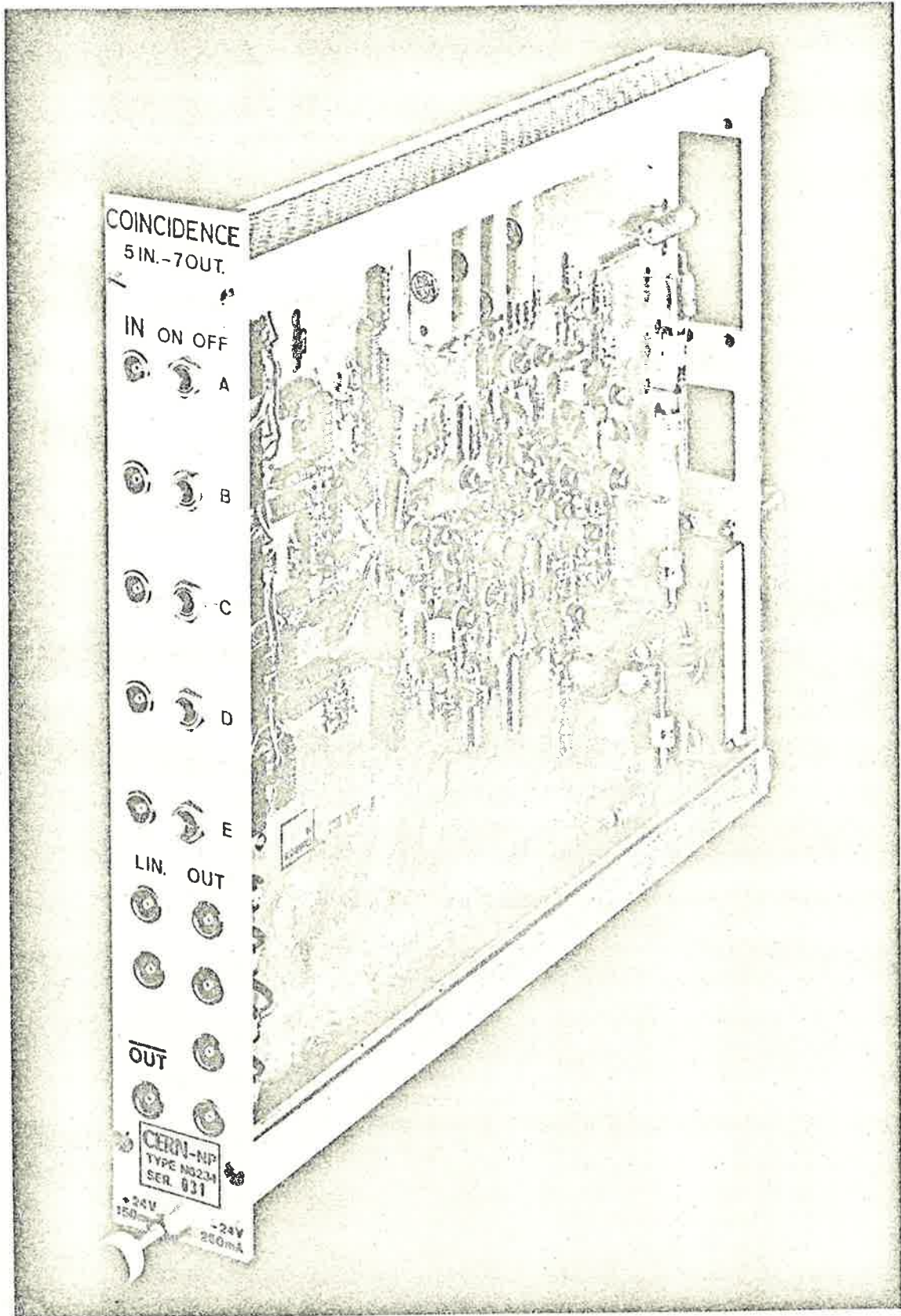


Fig. 1 : View of the front panel and of the inside

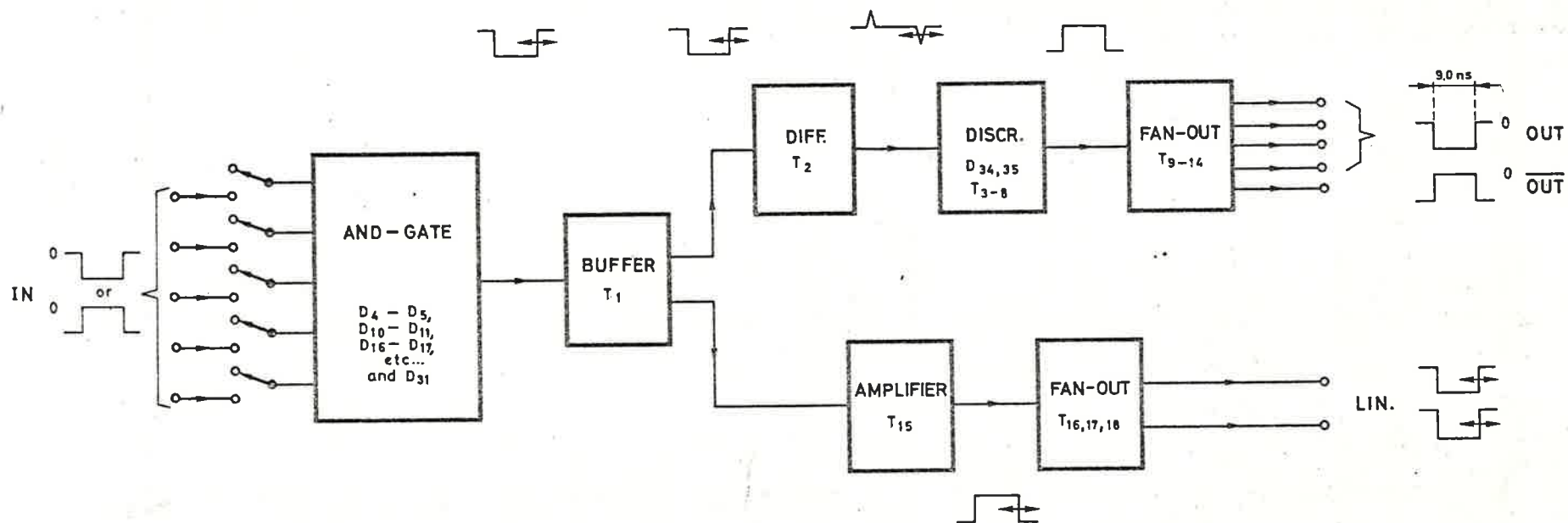
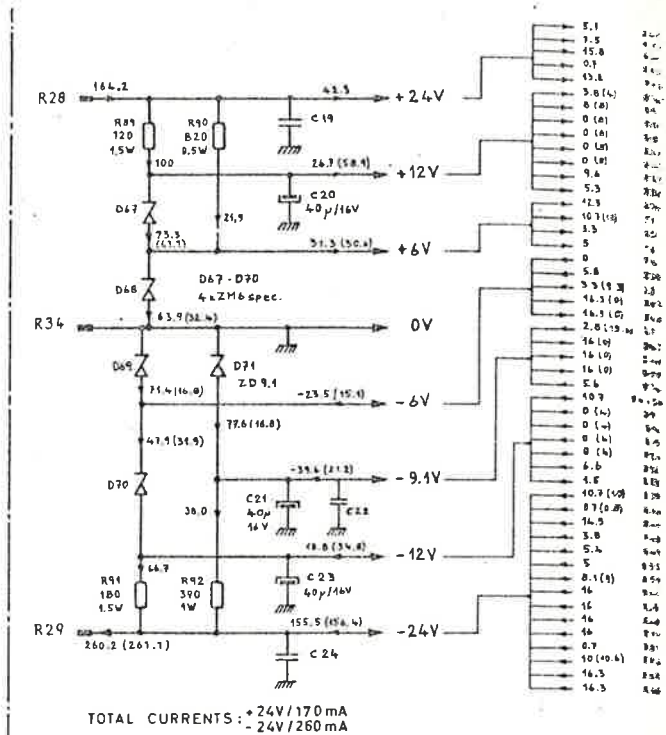
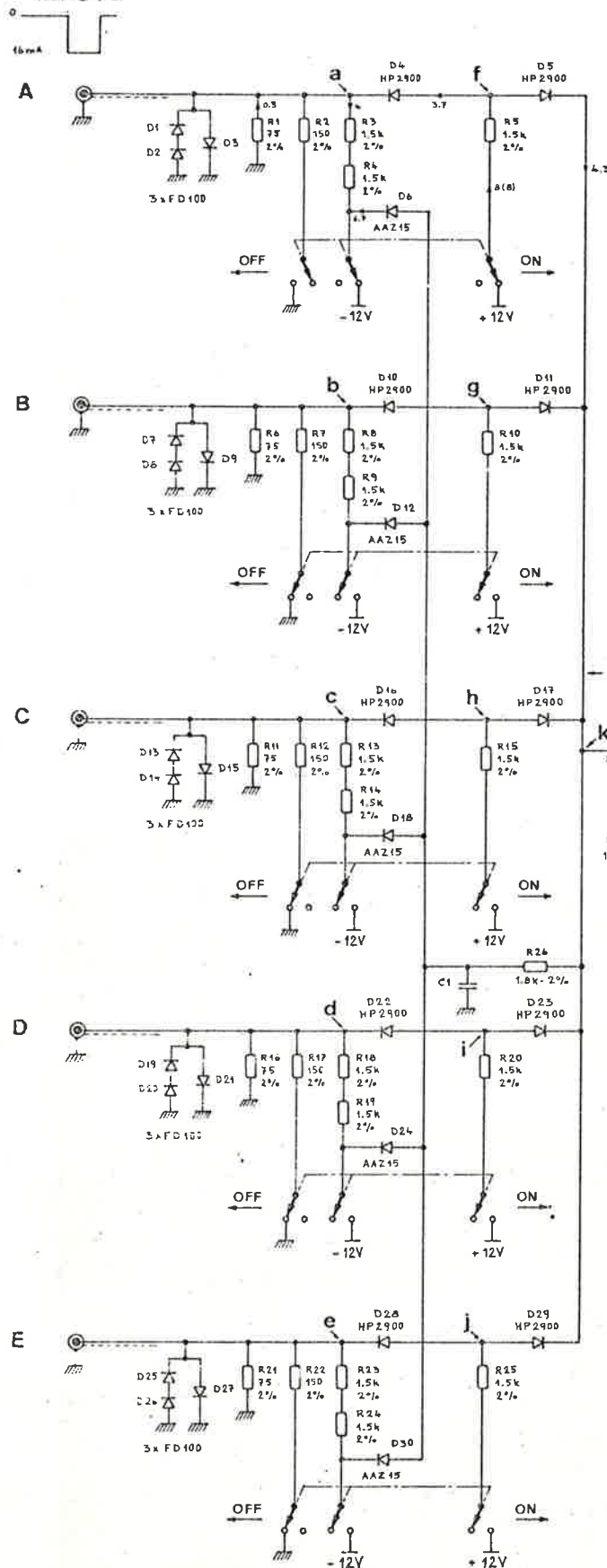
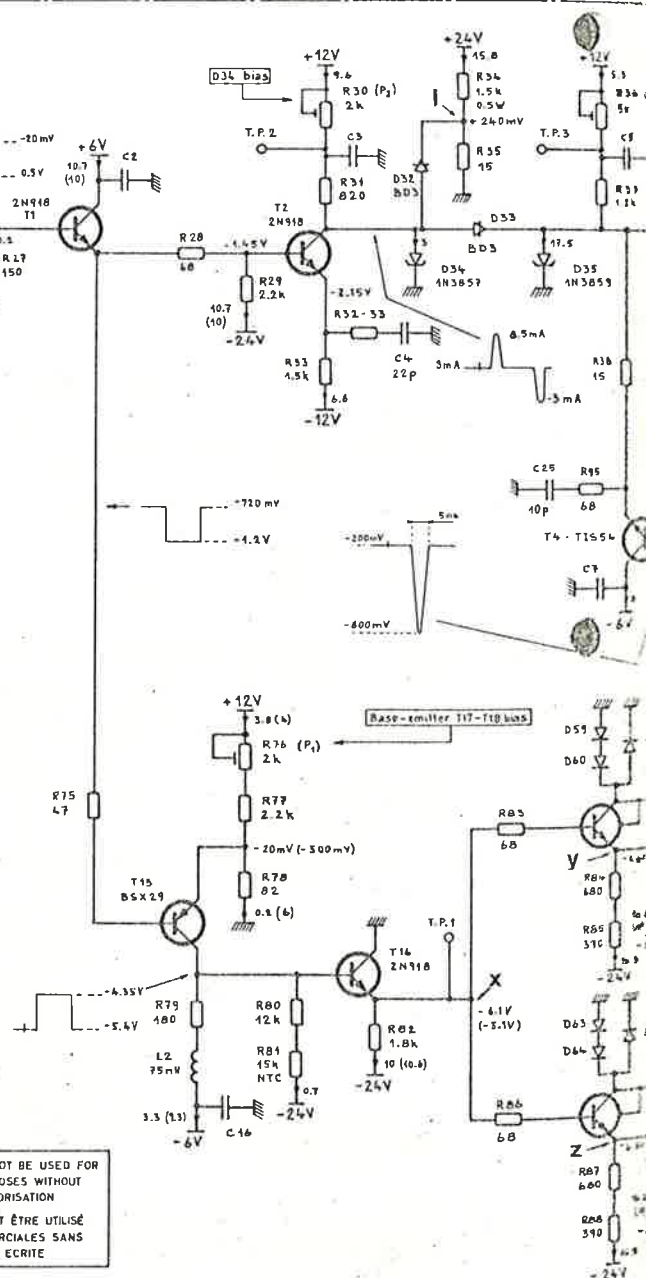


Fig. 2 : Functional block diagram

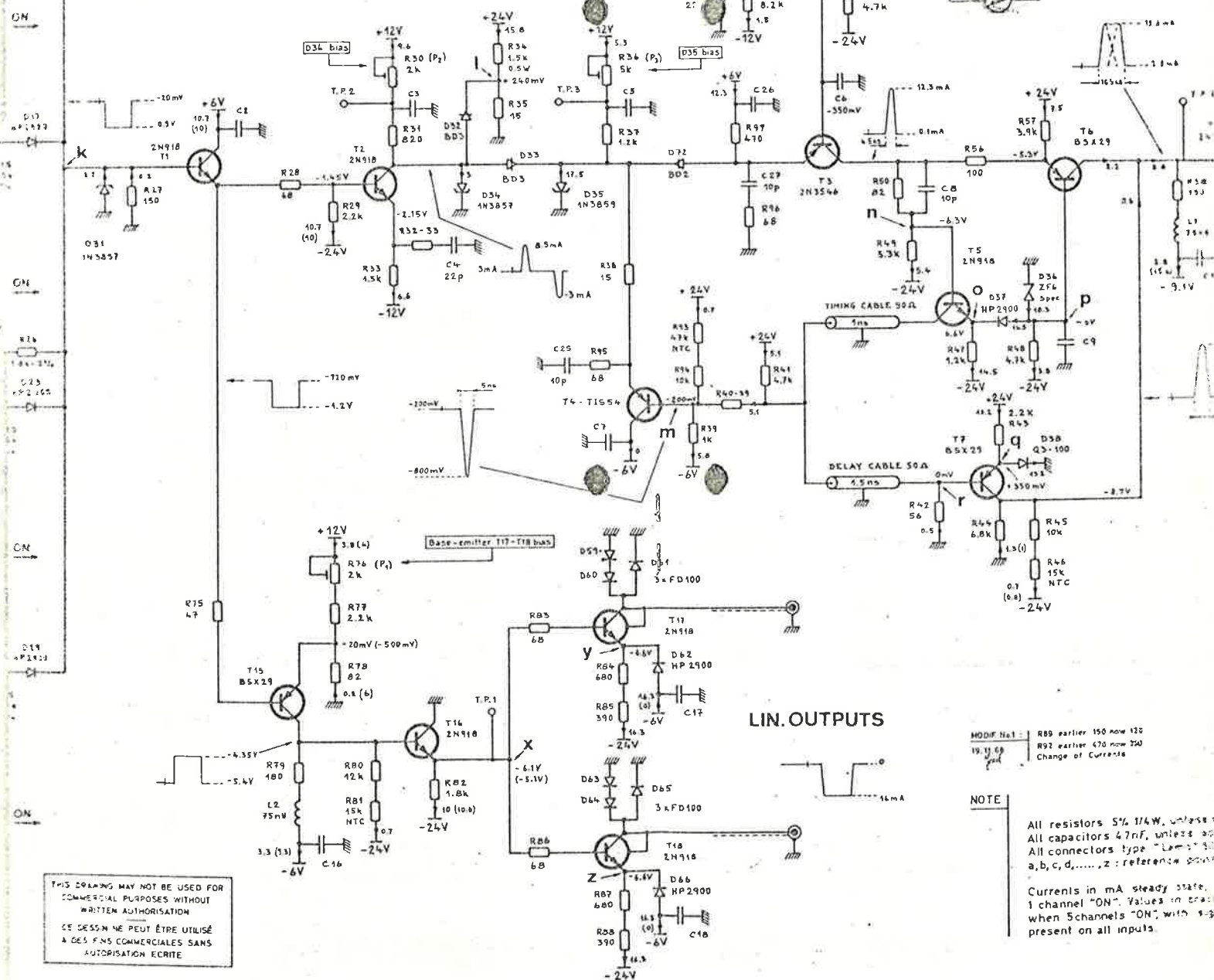
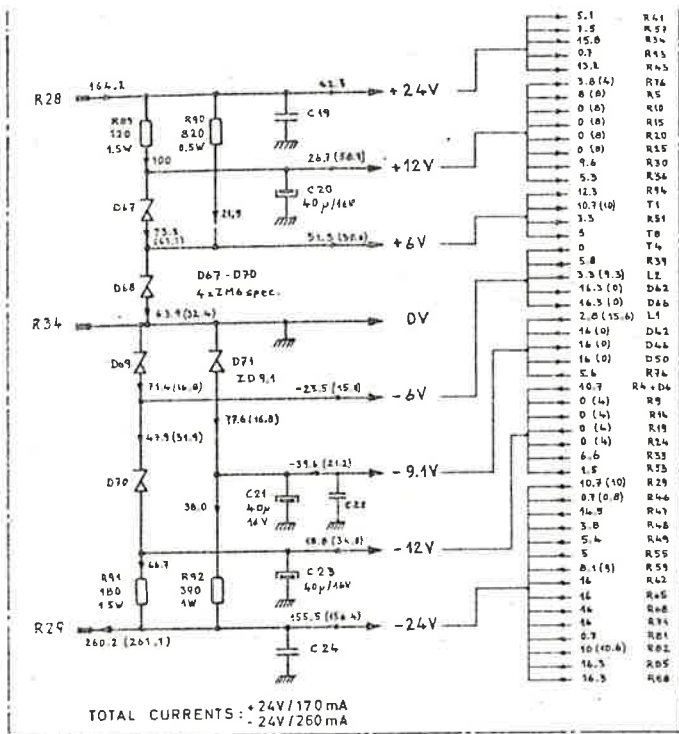
INPUTS



TOTAL CURRENTS: +24V/170mA
-24V/260mA



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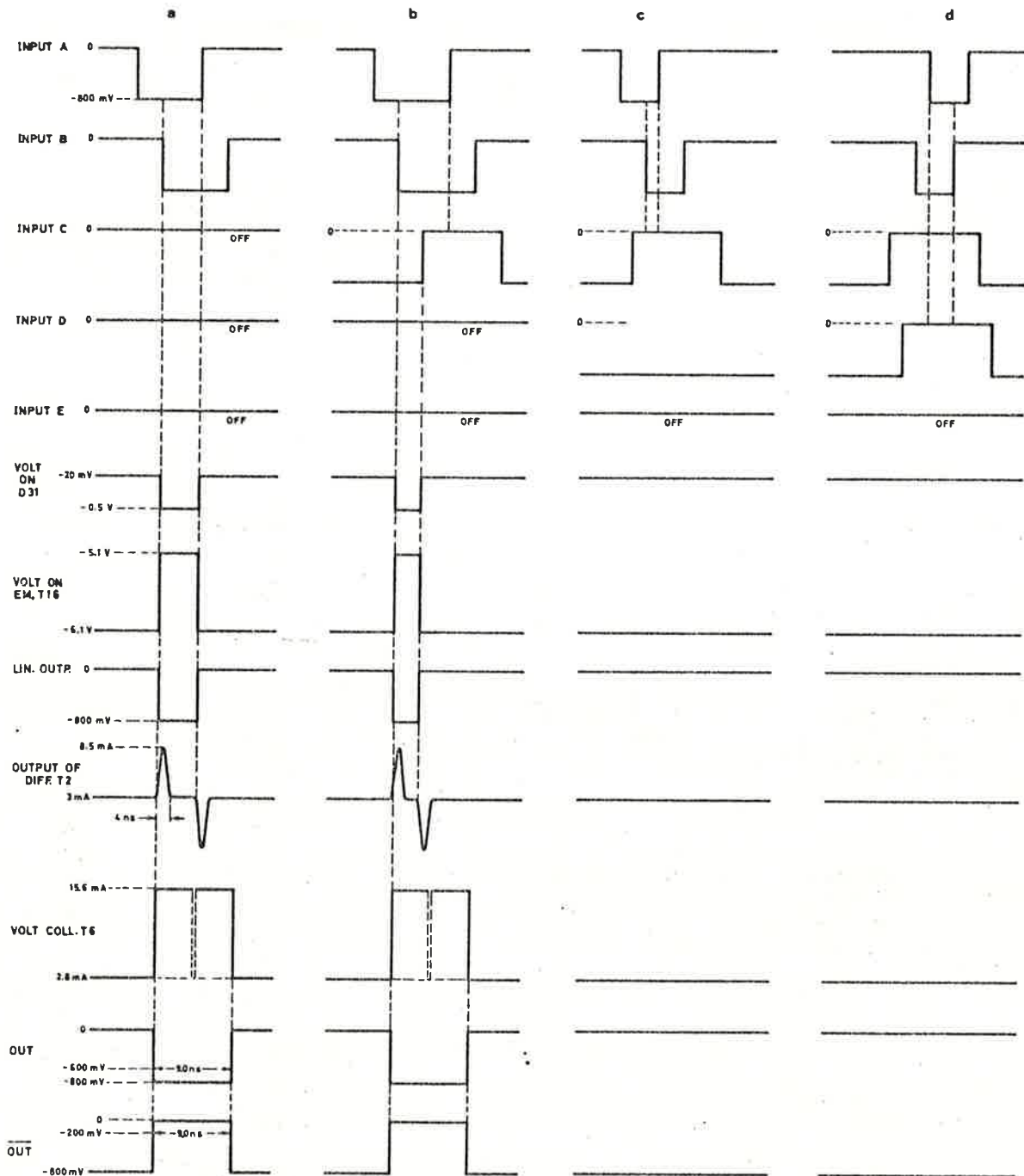


Fig. 4 : Waveforms in various points of the circuit for some input conditions:

- a) two logic inputs;
- b) two logic and one complementary logic input (anti);
- c) two logic and two complementary logic inputs, of which only one has a pulse overlapping the logic inputs;
- d) inputs as (c) but now both complementary logic inputs have pulses overlapping the logic inputs

- Loadline when only one channel is "ON"
- Loadline when two channels are "ON"
- Loadline when three channels are "ON"
- Loadline when four channels are "ON"
- Loadline when five channels are "ON"
- High-state loadline

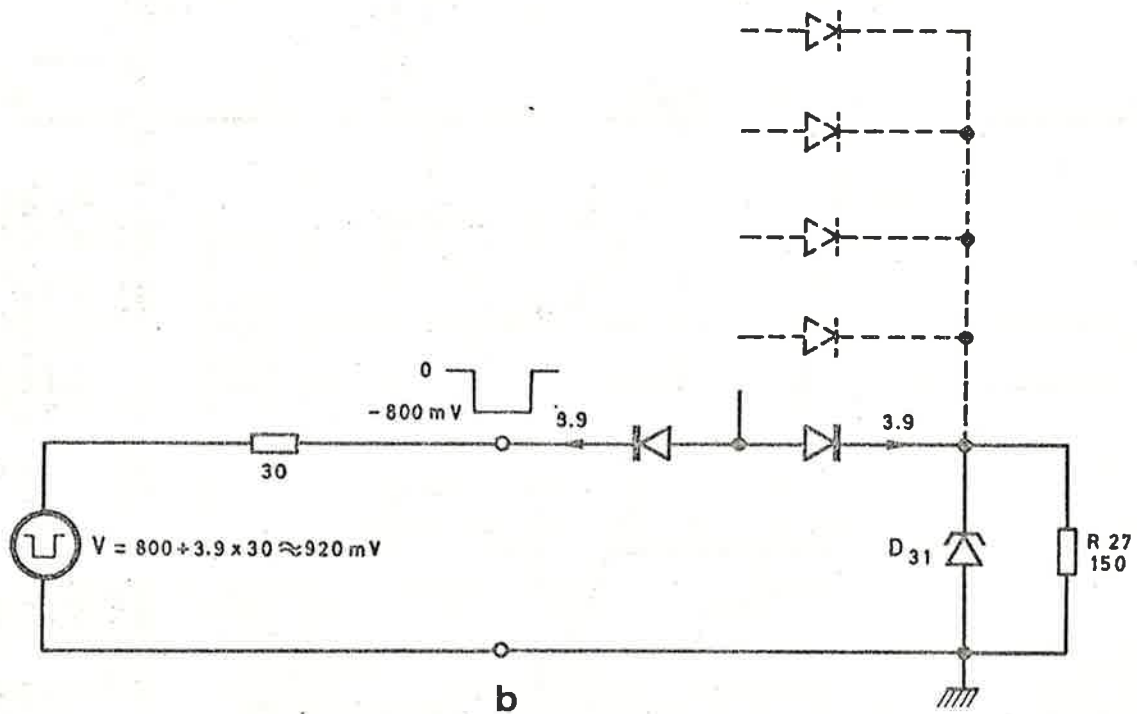
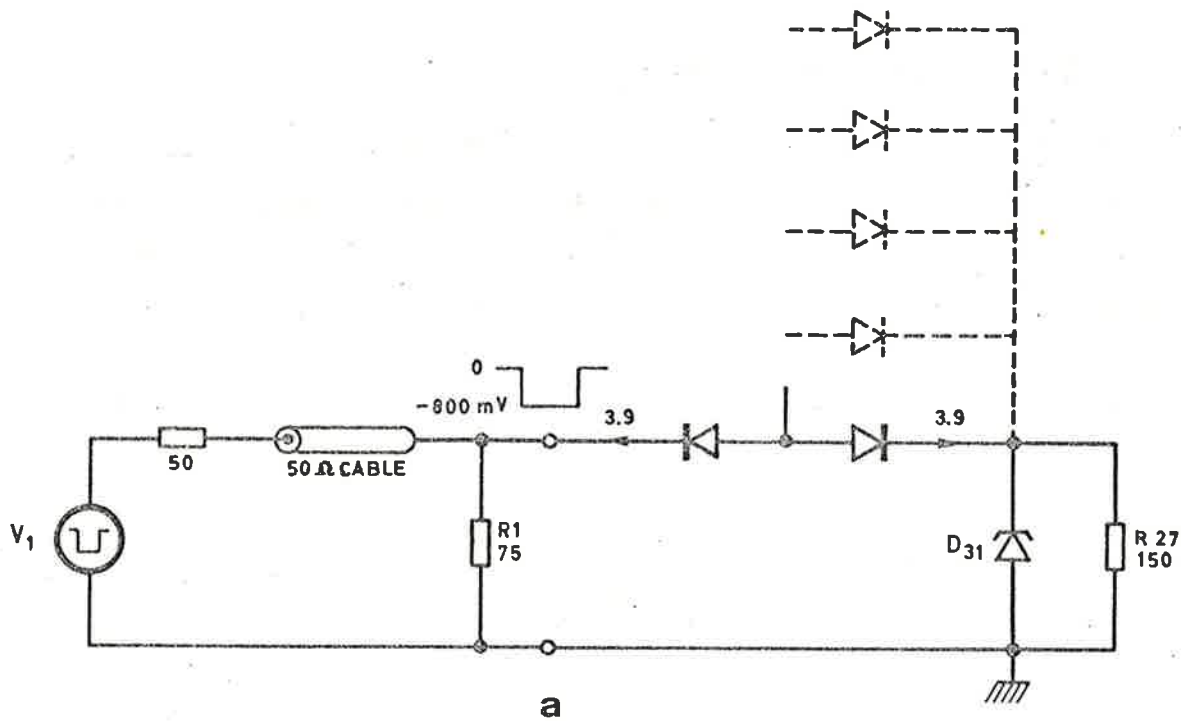


Fig. 6 : Equivalent circuits used for the calculation of the loadlines:

- a) Complete
- b) Reduced

INPUT

Number: 5
Impedance: 50 Ω
Reflections: In "On" State: < 20% (capacitive)
 In "Off" State: < 15% (inductive)
Voltage: Logic, -800 mV for coincidence.
 Complementary logic for anticoincidence.
Width: Minimum width or overlap (at minimum input "1" level = -12 mA) to produce outputs.
LIN: For singles ≤ 2.0 nsec
 For 5-fold ≤ 2.0 nsec
OUT and $\overline{\text{OUT}}$: For singles ≤ 1.5 nsec
 For 5-fold ≤ 1.25 nsec
Maximum Rate: Determined by output specifications.

OUTPUT

LIN: (Overlap Output)
Number: 2 logic
Impedance: High, current source, unused outputs need not be terminated.
Rise-time: $t_{01} \leq 1.8$ nsec
and
Fall-time: $t_{10} \leq 2.0$ nsec
Width: Equal to input width or overlap at min input "1" level (-12 mA)
 $+ \leq 1.0$ nsec for singles
 $- \leq 1.0$ nsec for 5-fold
Maximum Rate: ≥ 200 MHz
Propagation
delay: 6.2 ± 0.75 nsec (between min. input and output "1"), for singles. For 5-fold it decreases by ≤ 0.5 nsec.
Feedthrough: for n-1, $\leq |\pm 50|$ mV
OUT AND $\overline{\text{OUT}}$: (Standardized output)
Number: 4 logic
 1 complementary
Impedance: High, current source, unused outputs need not be terminated.
Rise-time: Logic: $t_{01} \leq 1.5$ nsec Complementary: $t_{10} \leq 2.0$ nsec
and
Fall-time: $t_{10} \leq 2.2$ nsec $t_{01} \leq 2.2$ nsec
Width: Logic, 9.0 ± 1 nsec at min input "1" level (-12 mA)
 Complementary, 9.0 ± 1 nsec at max input "0" level (-4 mA).
Maximum Rate: Up to a frequency of ≥ 70 MHz the output consists of pulses, i.e. the level between pulses comes down inside the output "0" band. At a frequency of ≥ 100 MHz the output has become d.c.; when exceeding this rate it turns into pulses again but counts will be lost.
Propagation
delay: $9.5 \text{ nsec} \pm 1.2 \text{ nsec}$ (between min input and output "1"), for singles. For 5-fold it decreases by ≤ 0.5 nsec.

POWER CONSUMPTION

-24 V ≤ 260 mA
 +24 V ≤ 170 mA

- N.B.
- 1) Rise- (t_{01}) and fall-times (t_{10}) are measured between maximum output "0" (-100 mV) and minimum output "1" (-700 mV).
 - 2) All parameters have been determined with input signals having rise- and fall-times of 0.7 nsec.

Fig. 7 : Specifications

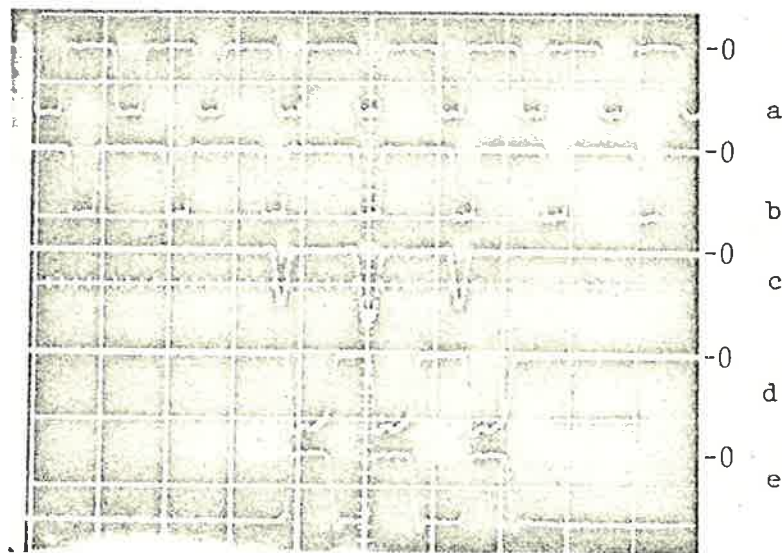


Fig. 8 : Coincidence operation:

- a) Input to one channel
- b) Input to another channel
- c) Overlap output (LIN)
- d) Discriminator, logic output (OUT)
- e) Discriminator, complementary logic output ($\overline{\text{OUT}}$)

Scale: Hor. 16 nsec/div. Vert. 800 mV/div.

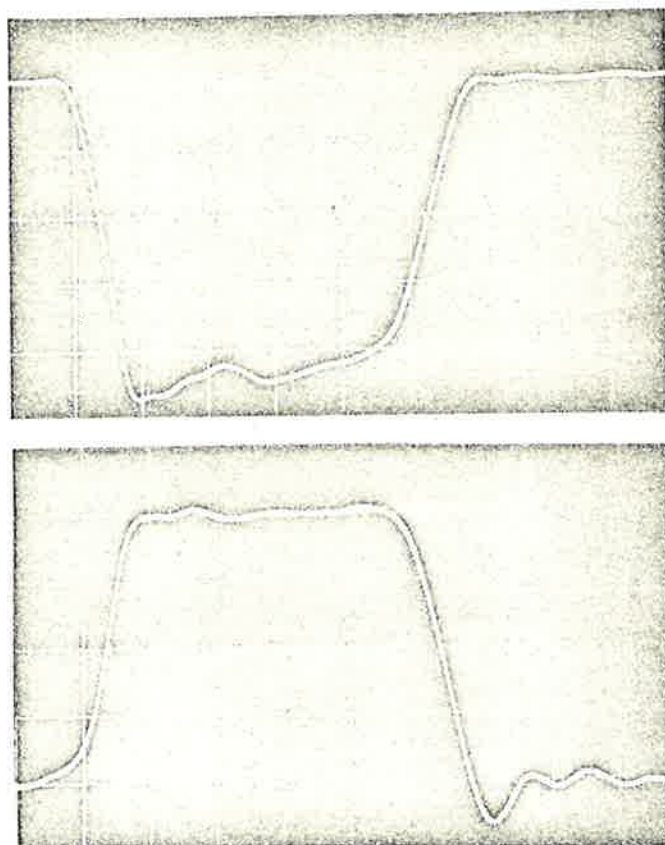


Fig. 9 : Discriminator output:

a) Logic (OUT)

b) Complementary logic ($\overline{\text{OUT}}$)

Scale: Hor. 2 nsec/div. Vert. 200 mV/div.

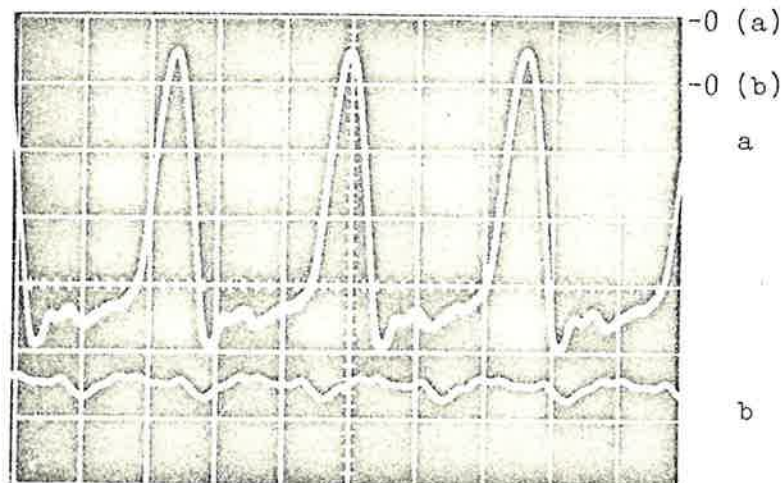


Fig. 10 : Operation of the discriminator channel at high repetition rates:

- a) Output (OUT) at maximum pulse rate
- b) Output (OUT) at maximum duty cycle

Scale: Hor. 5 nsec/div. Vert. 200 mV/div.

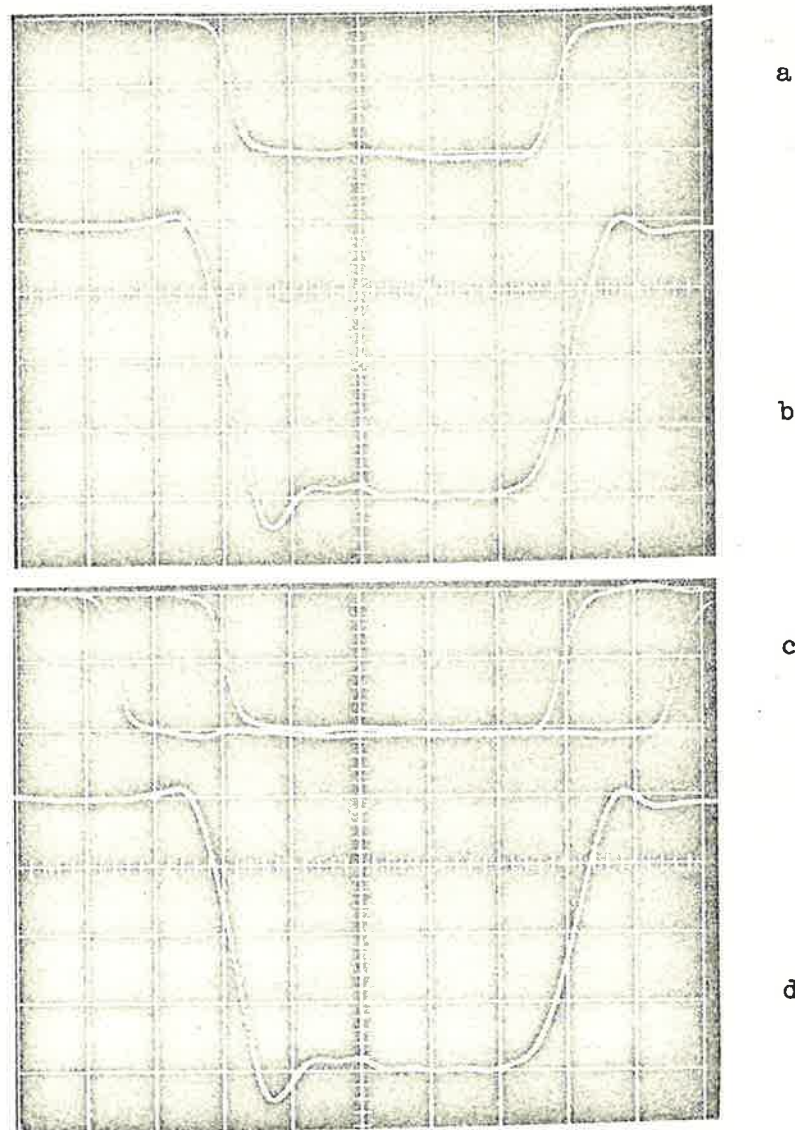


Fig. 11 : Overlap output

- a) Single input
- b) Output (LIN)
- c) Two overlapping inputs
- d) Output (LIN)

Scale: Hor. 2 nsec/div. Vert. a and c 400 mV/div.
b and d 200 mV/div.

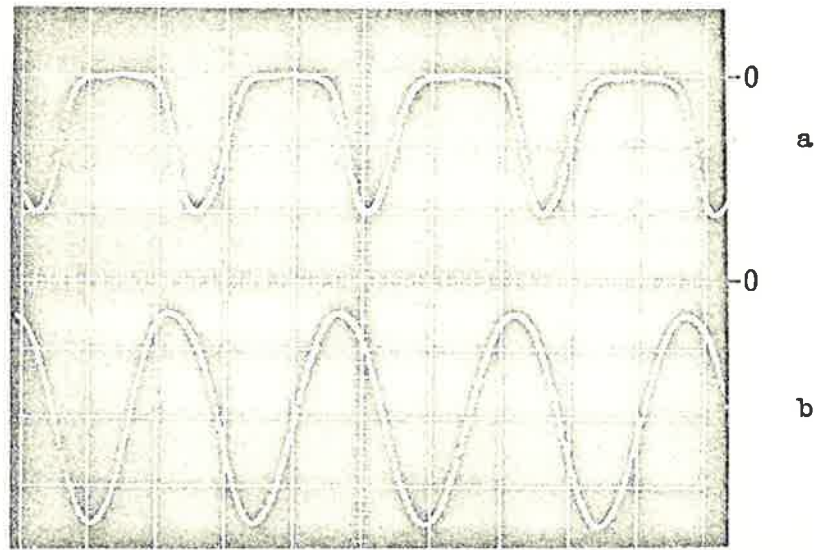


Fig. 12 : Operation of the overlap channel at high repetition rates:

a) Input

b) Output (LIN) at maximum repetition rate (≥ 200 MHz)

Scale: Hor. 2 nsec/div. Vert. a) 400 mV/div

b) 200 mV/div.

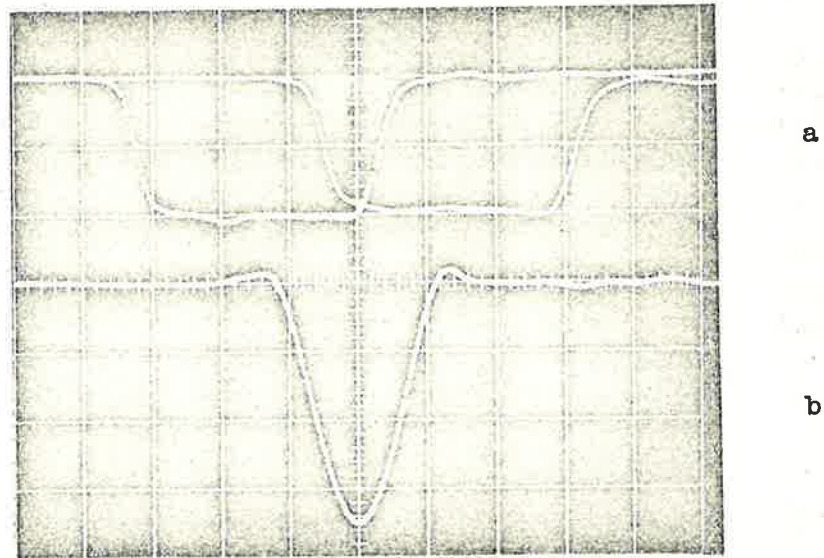


Fig. 13 : Minimum double coincidence resolving-time:
a) Two inputs with minimum overlap
b) Output (LIN)
Scale: Hor. 2 nsec/div. Vert. a) 400 mV/div.
b) 200 mV/div.

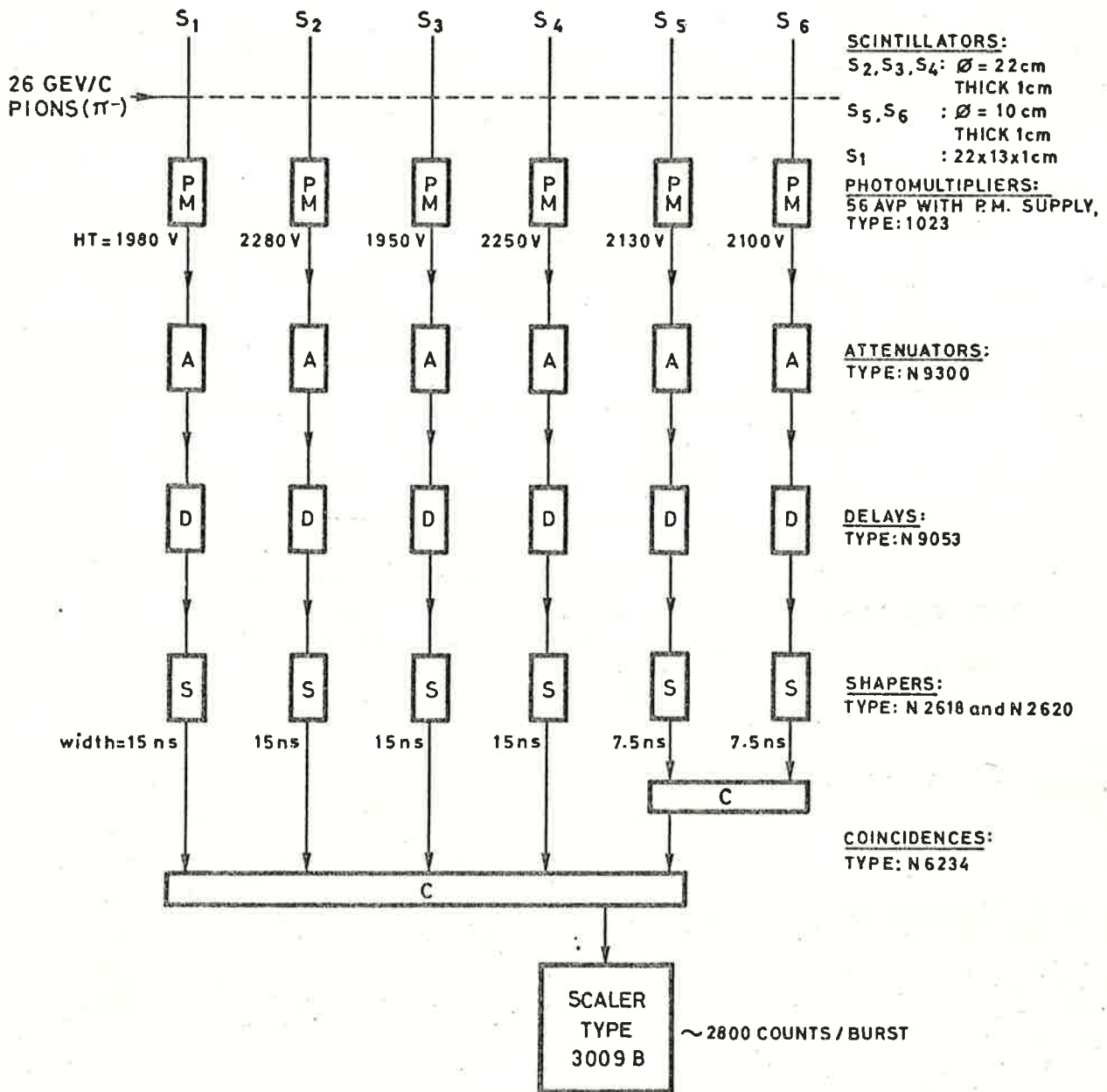


Fig. 14 : Counter arrangement as used in a recent CERN experiment
 (information kindly provided by J.V. Allaby et al.)

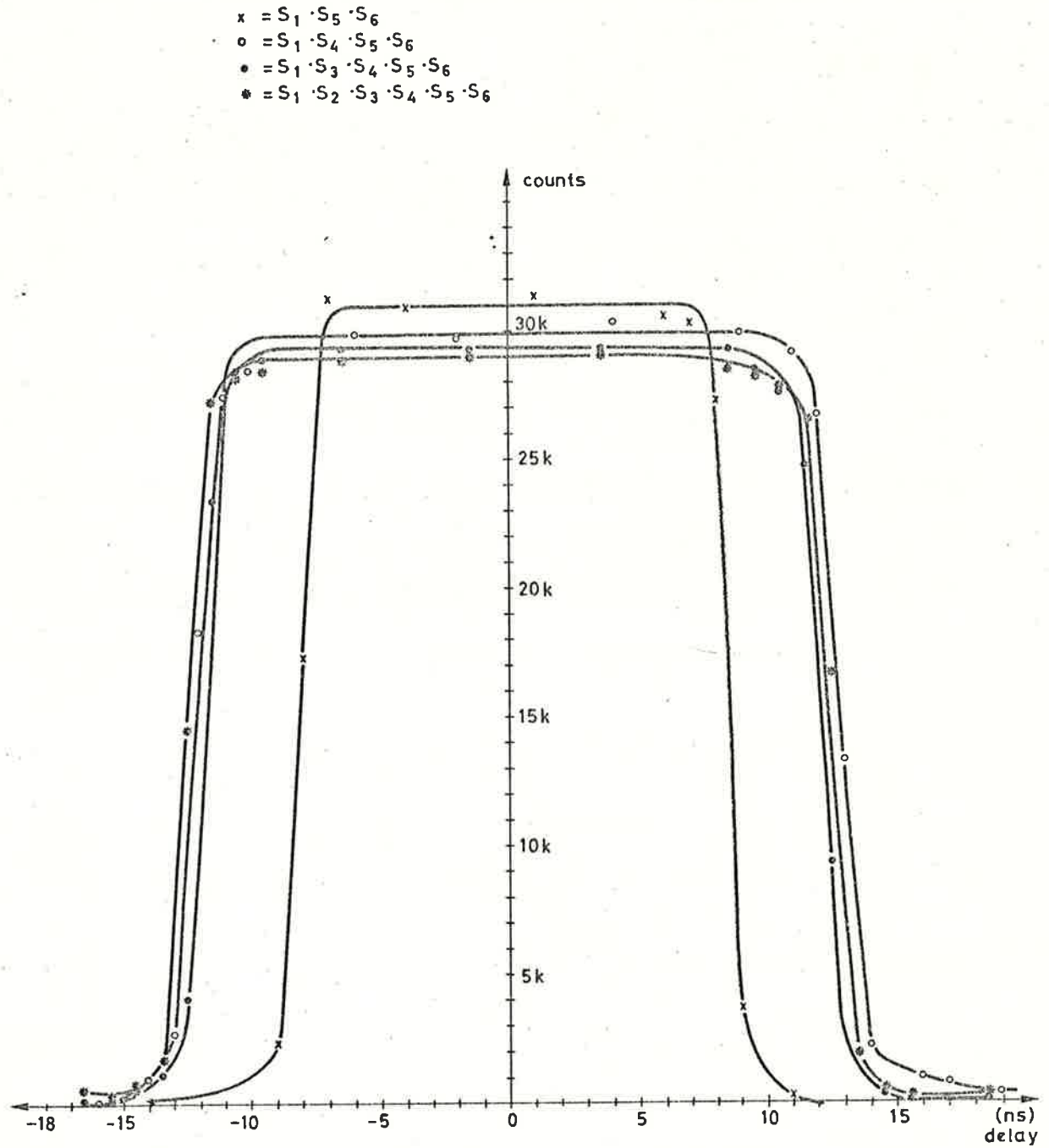


Fig. 15 : Timing curves measured with the experimental set-up as shown in Fig. 14.