Invited Paper

Data Output Interface for Holographic Memory

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ABSTRACT

The issue of interfacing holographic memory with an electronic processor is discussed. The high speed and parallel access of two dimensional, page formatted optical data from holographic memory can be utilized to reconfigure an electronic processor at a rate much faster than traditionally available. This new technique could be the stepping stone to a new class of high performance device for a variety of image/signal processing tasks.

We will first give a review of the holographic memory activity at Holoplex, in particular, our research on holographic optical disk as a read-only memory device. We will then discuss the optical architecture for interfacing an optical ROM with a programmable gate array processor.

Keywords: optical memory, holographic ROM, parallel access, reconfigurable computing.

1. HOLOGRAPHIC ROM (HROM)

We have implemented a holographic optical disk for high-capacity, digital data storage application. The holographic disk utilizes the Bragg-selectivity of the volume hologram to achieve a storage density much higher than conventional means. Figure 1 illustrates the holographic disc system where the holograms are arranged on concentric tracks. Each spot contains a number of multiplexed holograms that can be read out in separate steps by steering the reference beam to different angles

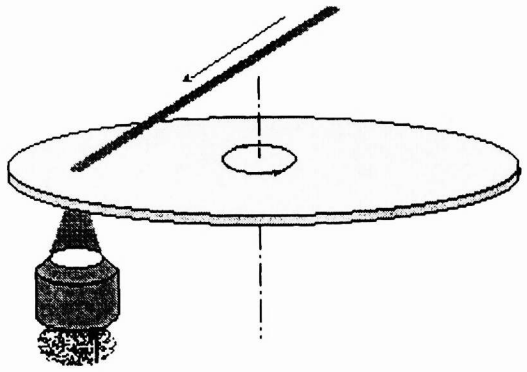

Figure 1. Conceptual Diagram of the Holographic Optical Disk

The imaging optics and the performance of the imaging system are shown in figures 2 and 3. The pixels on the SLM are imaged and one-to-one matched to the detector array, for the entire field of view. The SNR of the transmitted image varies from 10.5 in the center to 7.5 at the edge. The performance of the imaging optics is sufficient for the target specifications.

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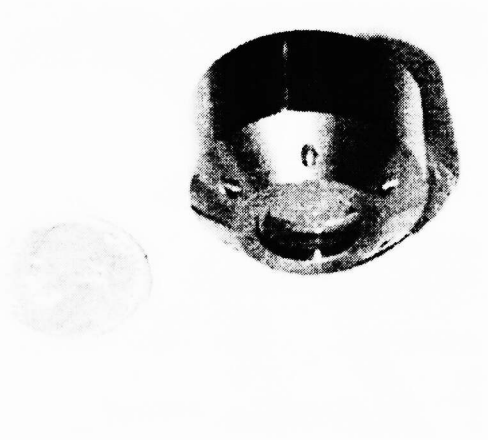

Fig.2. Imaging optics for holographic disk.

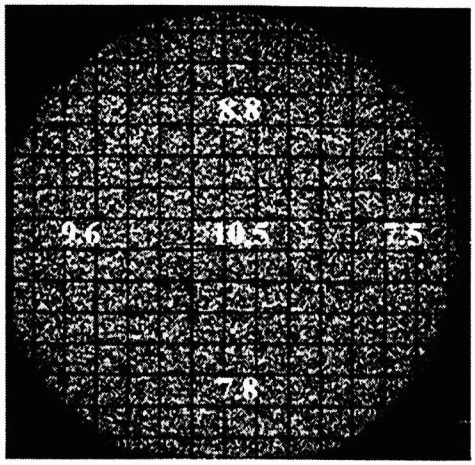

Fig.3. SNR of the imaging system

In our system, each hologram contains 180,000 pixels, and the entire page is stored in an area of roughly 0.6 mm in diameter. This gives us a storage density of 0.5 bits/μm^2/hologram. We multiplex 80 holograms over each spot to achieve a density of 40 bits/ μm^2. During readout, the 12 cm disc is spun continuously at 600 r.p.m., and pixel-matched holographic data is readout from the disc in real-time.

When the holographic image is readout from the spinning disc, the reconstructed images could be shifted, distorted, or defocused. These may be caused by disc wobble, disc decentration, and by mechanical deformation in the disc substrate. When these happen, the readout holographic image is degraded and the bit error rate becomes exceedingly high. In order to maintain image alignment and good pixel registration, we have designed a servo system that detects the readout error in the hologram and automatically compensates for the disc error in real time. Figure 4 is the schematic of our holographic disc system. The laser beam (from the top) passes through the modulator and enters the scanner. The scanner can change the laser beam propagation direction along two orthogonal axes in space. The laser beam is directed to the disc and the stored images are read out. Alongside the main readout image, there are two separate pixels in each hologram which we call control pixels. The control pixels are directed to two quadrant photodetectors, respectively. If the disc were at still and at correct position, the control pixels would be focused at the center of each quadrant detector. Since the disc spins continuously, the control pixels actually sweep across the detector, as does the main reconstructed image. We pulse the laser to readout a stationary image onto the detector array. The laser pulse timing is slaved on the gap-crossing of the left control pixel. As the laser fires, the holographic image is registered, and the signals from the quadrant photodetectors are sampled. A controller derives the appropriate error signals from the quadrant detector, and drives the scanner to compensate for image shift and rotation in real time.

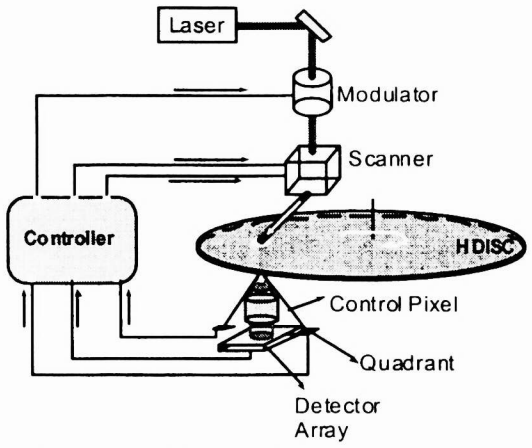

Fig. 4. Schematic of the holographic disc.

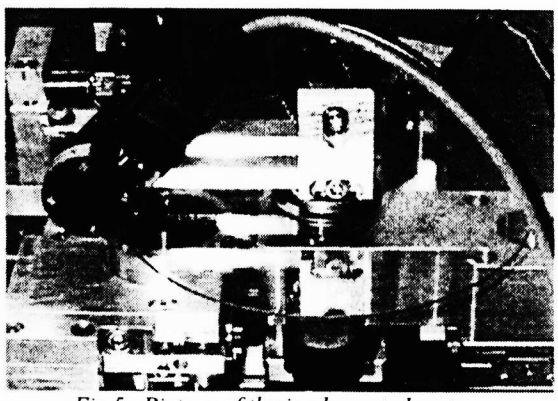

Fig.5. Picture of the implemented system.

Figure.5 is a picture of the disc system that we have implemented. We use frequency doubled YAG laser as the light source. The disc is fabricated by laminating a layer of holographic photopolymer onto a glass substrate. We have achieved one-to-one matched detection of optical pixels and real-time readout of the underlying digital data while the disc is continuously spinning.

2. OPTICALLY PROGRAMMABLE GATE ARRAY (OPGA)

The OPGA is a device that uses the high-speed optical data from an HROM to actively control the function of a programmable gate array device (FPGA). The HROM in the OPGA is simpler and much more compact than the disk-based system presented in previous section, but the underlying technology remains the same. The OPGA module consists of 3 major components: The silicon chip that contains the FPGA circuitry and light detectors, a hologram containing the reconfiguration data, and a VCSEL array that acts as a light source and multiplexing mechanism selecting the reconfiguration templates from the hologram and transferring them to the Si chip.

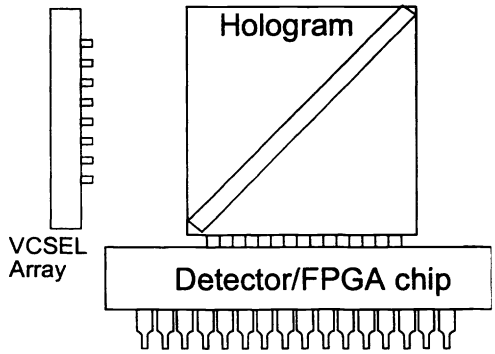

Figure 6. The OPGA Module

Figure 6 shows an optically programmable gate array module. It integrates an optically addressable FPGA chip with a compact holographic memory. Holographically stored information is read by a VCSEL array and detector elements on the FPGA chip. The entire FPGA can be reconfigured in a single shot. The rapid reconfiguration capability of the module introduces a new computational paradigm. Complex problems can be solved employing relatively little silicon real estate without any sacrifice of speed. Overhead costs associated with moving information between processors and memories can be greatly reduced. General purpose computing can be achieved at a speed that rivals that of customized electronics. In summary, the OPGA presents an opportunity for implementing digital algorithms at high speed and low cost.

The holographic template can be recorded in a photopolymer material using the shift-multiplexing technique. The Du Pont photopolymer has many desirable properties that are suitable for this application. The material is sensitive at laser diode wavelengths, and it has very good MTF allowing high resolution images to be recorded and reconstructed. Recorded

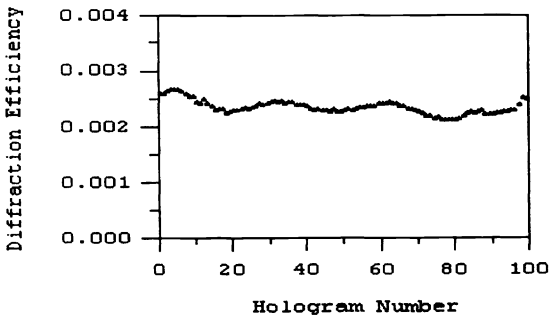

Figure 7. Photopolymer characteristics.

holograms can be fixed by UV curing. The material is a film about 100 μm thick. The photopolymer also has a large dynamic range, with an M/# of about 5. Figure 7 shows the equalized diffraction efficiency of 100 holograms recorded in photopolymer.

Laser diode array

The light source for holographic readout in the OPGA is a VCSEL array. The performance of this device has direct impact on the overall performance of the system. Honeywell has succeeded in fabricating red laser diodes that operates in single spatial and longitudinal mode, having 1mW output power at 660nm, and with good room temperature lifetime. These devices can also be switched on/off at speeds much faster than the one microsecond required here. Figure 8 shows a 4X4 VCSEL array that we are currently testing. With the existing power of 1mW and an M/# of 5 from the polymer, we could

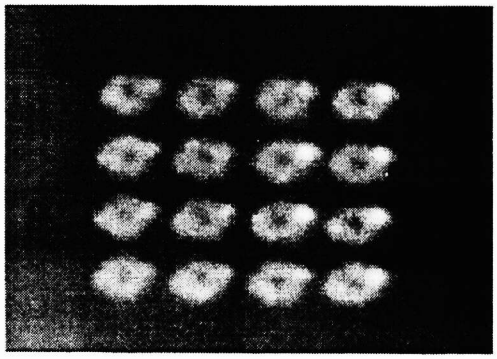

Figure 8 The VCSEL array

store 100 templates of 10,000 pixels each and readout the page within one microsecond. The long term stability of the VCSEL array, especially power and wavelength stability, is a key issue for the laser diode array. Fluctuations in power causes changes in reconstructed power, and affecting the integration time and speed of operation. Fluctuations in wavelength causes the reconstructed image to change position and in size. The holographic data bits can be mis-registered, and the SNR degraded. We are presently investigating these issues.

Silicon circuit: FPGA

Figure 9 shows the conceptual layout of the silicon OPGA chip. The chip consists of an array of I/O blocks and configurable logic blocks (CLB). An array of light detectors is implemented on the same chip in a way illustrated by figure. The light detectors receive and convert the holographic data bits into electrical signals that are used to control the FPGA functionality. Figure 10 shows the typical circuit for a CMOS active pixel detector cell. It consists of a silicon photodiode, a capacitor, and a few transistors that control the biasing and operation of the photodiode. The data bits from the holographic template is used

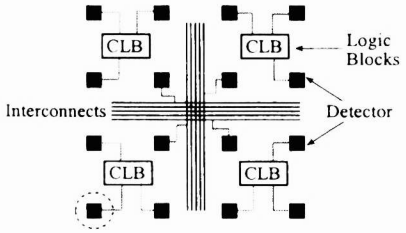

Figure 9

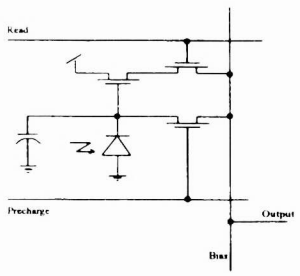

Figure 10

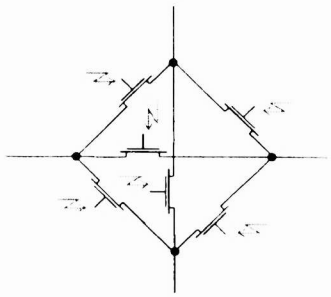

Figure 11

to configure the FPGA chip in two possible ways. The logic function implemented by each individual logic block can be reconfigured. The interconnect pathway between any two logic blocks can also be optically programmed. Figure 11 shows the configuration of one interconnect node by means of optical illumination. This interconnect node is attached to four lines, and has six possible interconnect patterns. By optically activating the gate of a particular transistor, we can control the direction of routing for this node. In FPGA, the logic function of each logic block is implemented by an SRAM look up table. Rewriting the SRAM with the holographic data bits reconfigure the logic function. Conventional FPGAs usually take milliseconds to seconds to reconfigure. The OPGA shown in figure 6 is able to reconfigure itself on the order of a microsecond. This is achieved through the high I/O bandwidth of holographic memory, and the silicon design that integrates the detector array within the FPGA chip.

3. REFERENCES

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