Holographic memory design for a petaflop superconducting computer architecture

Ernest Chuang, Wenhai Liu, and Demetri Psaltis
California Institute of Technology, Mail-Stop 136-93, Pasadena, CA 91125
Tel: (626) 395-4843, Fax: (626) 568-8437

SUMMARY

We will describe the role of holographic memory in a current research effort[1] that seeks to combine various advanced technologies to achieve petaflops scale computing within the next decade. In addition to holographic memory, the petaflop architecture combines superconductor Rapid Single Flux Quantum (RSFQ) logic, which can operate at 100 GHz within a cryogenic environment with power consumption less than 50 watts, a packet-switching optical network with a multi-level structure capable of providing interconnection among tens of thousands of ports with latencies of only 10 to 30 nanoseconds, Processor-In-Memory (PIM) technology, and a multithreaded hierarchical structure (see Figure 1) to allow the processors to access a high capacity memory while compensating for the latency problem inherent in such a system.

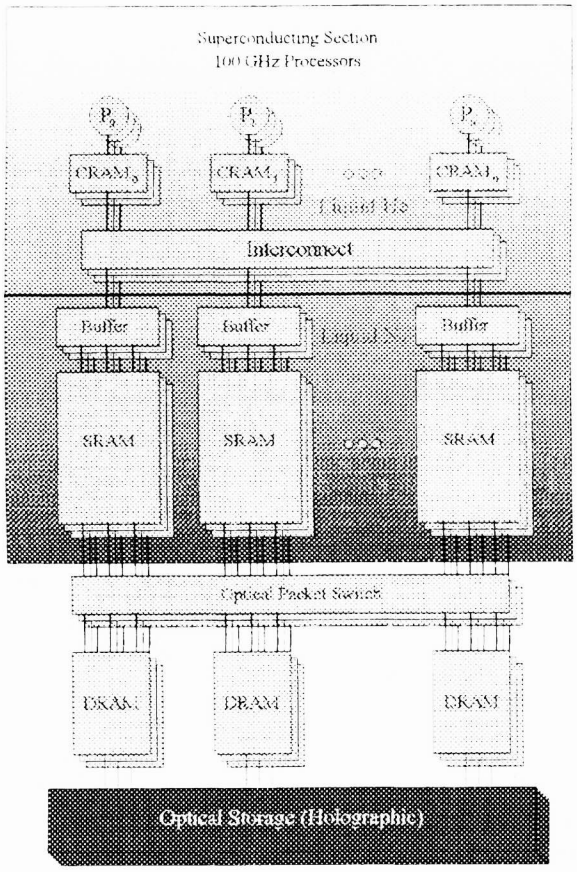

Figure 1. Schematic for the Hybrid Technology Multi-Threaded (HTMT) petaflop architecture

A Holographic Random Access Memory (HRAM) was chosen as the mass memory for its ability to offer both high-density storage as well as high bandwidth. The design specifications for this system are:

Total Capacity	100 terabytes
Access Time	10 microseconds
Total Bandwidth	100 terabytes/sec

The architecture that we have designed for the holographic memory uses a modular approach, with the basic unit module diagrammed in Figure 2. This system stores angularly multiplexed holograms in a photorefractive crystal in the 90-degree geometry, with data pages input by a Spatial Light Modulator (SLM) and read out with a detector array. We use conjugate readout to eliminate the need for imaging optics between the SLM and detector array, thus maintaining a compact size for the system. An alternative to using separate SLM and detector devices is to use a smart-pixel array that combines the functionality of these two components. We have demonstrated such a device experimentally.[2] With this design we can create a very compact high-density holographic memory module a few centimeters on a side, as shown in Figure 3.

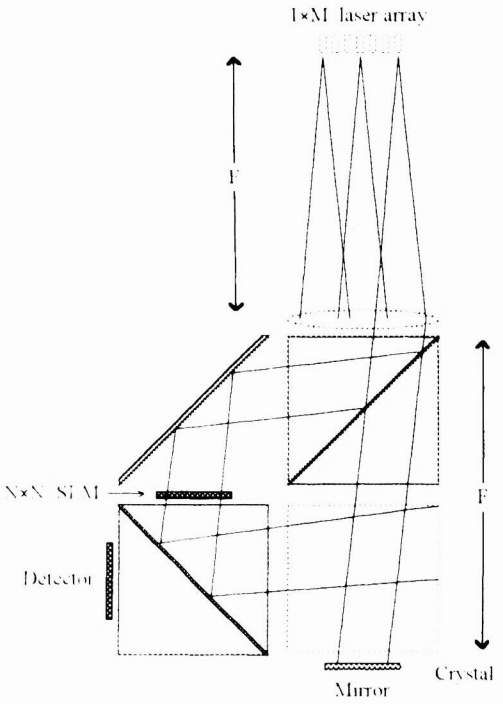

Figure 2. Schematic diagram of the compact holographic memory module with separate SLM and detector array components.

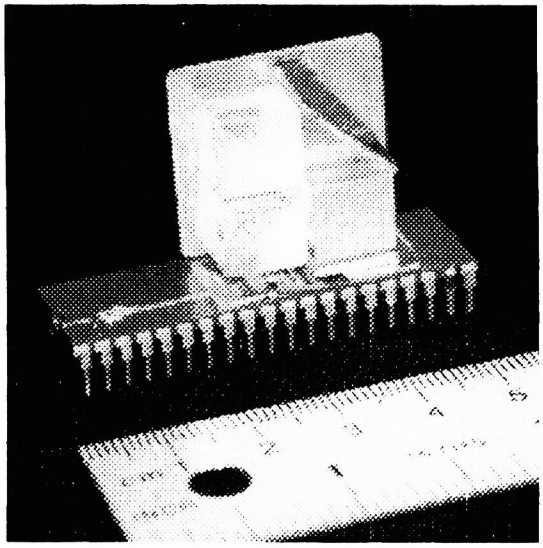

Figure 3. Model of the compact architecture using the smart-pixel array. (The laser array is not shown.)

To meet the 10μs access time target for the petaflops architecture, we are using a Vertical Cavity Surface Emitting Laser (VCSEL) array in combination with a Fourier transforming lens to produce the necessary range of multiplexing angles for the reference beam while allowing rapid random access. Each module has a capacity for on the order of one gigabit of storage. We can increase the storage capacity by assembling these modules together in an array. For example, an array of approximately 32 × 32 modules assembled on a board yields one terabit of data storage. The bandwidth requirements are met through both the inherent parallelism of the holographic storage as well as the parallel operation of the array.

In order to be a viable solution for the mass storage of the petaflop computer, the holographic architecture must not only meet the performance requirements of the system design, but it must also be cost effective. This is attainable through cost savings in silicon area gained by multiplexing data pages in the holographic memory, as illustrated in Figure 4, which compares the cost per bit stored in the HRAM with a comparable memory fabricated entirely in DRAM. We will present the cost projection of the HRAM and compare it to DRAM.

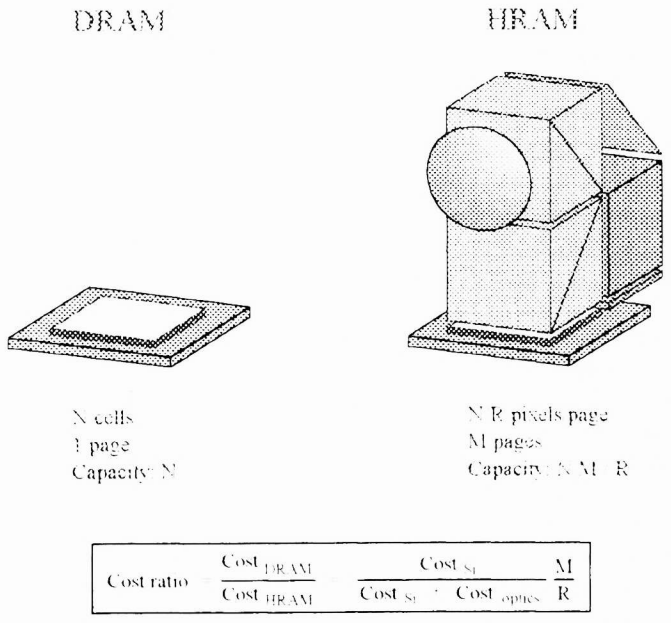

Figure 4. Cost comparison between DRAM and HRAM

REFERENCES

1. Thomas Sterling et al., "A hybrid technology multithreaded computer architecture for petaflops computing." Grant proposal submitted to DARPA in response to announcement BAA-97-03, March 1997

2. J-J. Drolet, E. Chuang, G. Barbastathis, D. Psaltis, "Compact, integrated dynamic holographic memory with refreshed holograms," *Optics Letters*, Vol. 22, No. 8, April 1997.