Optically Programmable Gate Array (OPGA)

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Field Programmable Gate Arrays (FPGAs) are very versatile devices. A typical FPGA consists of an array of configurable logic blocks and a mesh of interconnections fully programmable by the user to perform a given application. By just changing its internal connectivity, the FPGAs can implement a totally different new function. This concept of programmable hardware makes the FPGA be faster when compared to a general-purpose processor, but at the same time more flexible than a specific circuit (ASIC).

However in most of the applications, the FPGA is configured only once and used as coprocessor to carry out some highly complex or time-consuming computation. The reason for such limitation is the small communication bandwith between the FPGA chip and the external memory, usually ROM, where the configuration data is stored. A typical FPGA requires about 1Mbit of configuration data, which results in reconfiguration times of hundreds of milliseconds.

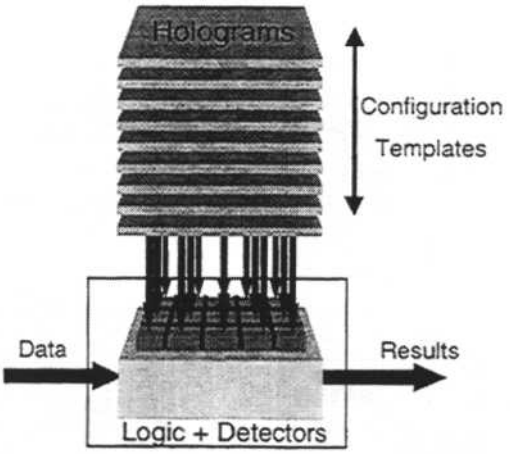

Figure 1: Interface between optical memory and FPGA.

To overcome this bandwidth limitation, we use an FPGA that can be very rapidly configured by transferring the configuration data from an optical memory (figure 1). The optical memory can store a very large set of configuration pages in the form of holograms, which can be transferred at once to the FPGA since the readout is page oriented. Therefore, this Optically Programmable Gate Array (OPGA) makes it possible to dynamically reconfigure the FPGA and use more efficiently its logic resources by time and space multiplexing them.

The OPGA module, as depicted in figure 2, consists of three major components. The silicon chip that contains the FPGA logic and the array of photodetectors, a holographic memory that stores the configuration templates, and an array of VCSELs that act as light source s and multiplexing mechanism selecting the reconfiguration templates and transferring them to the chip. The reconfiguration time for the OPGA is limited by the integration time of the photodetectors, which can be made to be of just hundreds of microseconds.

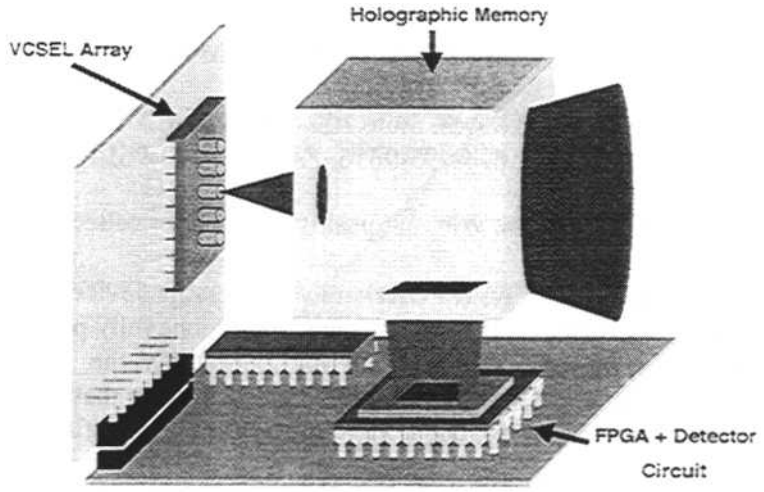

Figure 2: Optically Reconfigurable Gate Array module.

To multiplex the configuration templates in the optical memory, the shift multiplexing technique is used. To avoid crosstalk among holograms the shift selectivity of the material, a 100μm thick layer of red sensitive Du Pont photopolymer, is matched to the spacing between the VCSELs in the array.

Another approach to reduce the reconfiguration time consis ts of adding some built-in cache memory to the FPGA chip to locally store a few fast access configurations. However, this approach results in higher power dissipation and lower logic density. The performance, in terms of density of logic elements for a fixed die area, has been studied for both architectures: the cache based FPGA and the OPGA (figure 3), analyzing the trade-off between area dedicated to logic and area for either banks of memory or photodectors.

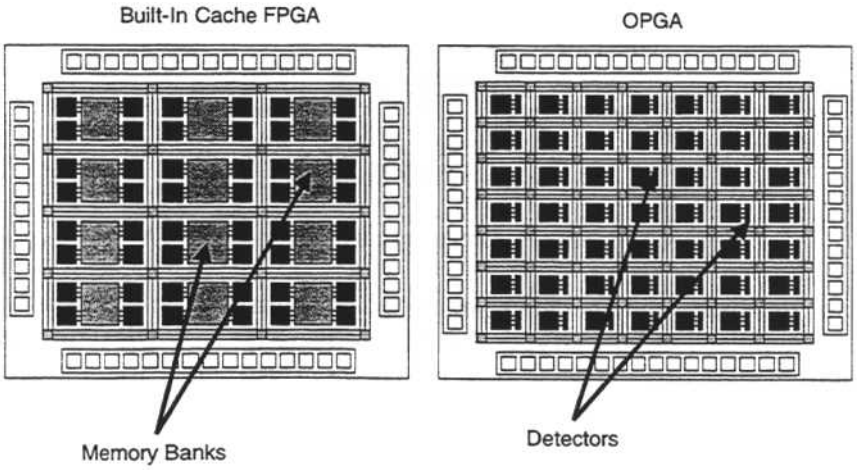

Figure 3: Area trade-off for both architectures.

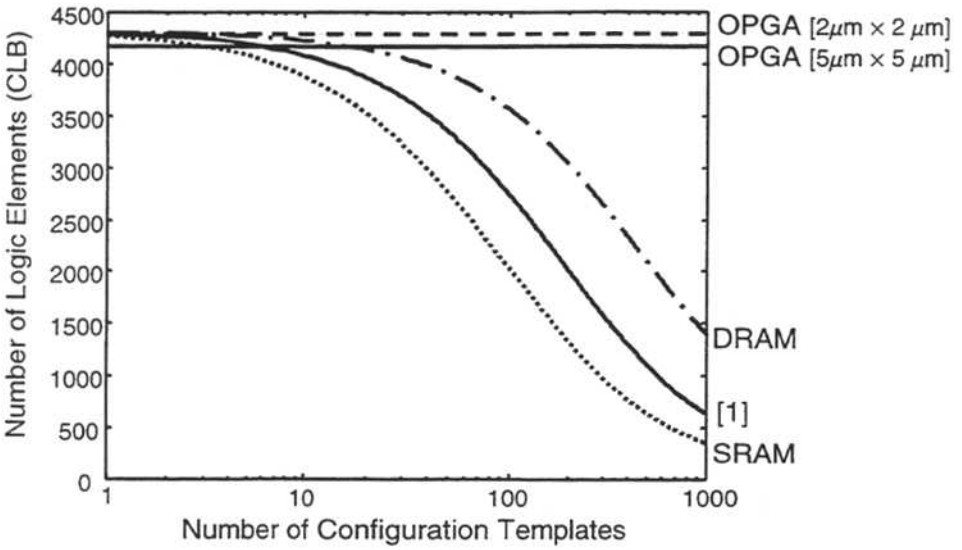

Figure 4: Performance comparison between OPGA and cache memory FPGA.

As shown in figure 4, for small number of contexts the performance of both architectures is about the same, but the logic density of the cache-based FPGA degrades as the context depth of the cache increases, while for the OPGA it is independent of the number of templates. The comparison is made with DRAM and SRAM, the latter is more fair due to the non-volatility of the optical memory.

The experimental OPGA is shown in figure 5a. A 4x4 array of red VCSELs (figure 5b) working at 680nm has been used to study the suitability of VCSELs for this application. Holograms have been recorded and readout with the VCSELs and the reconstruction has been pixel matched to the detector (figure 5c).

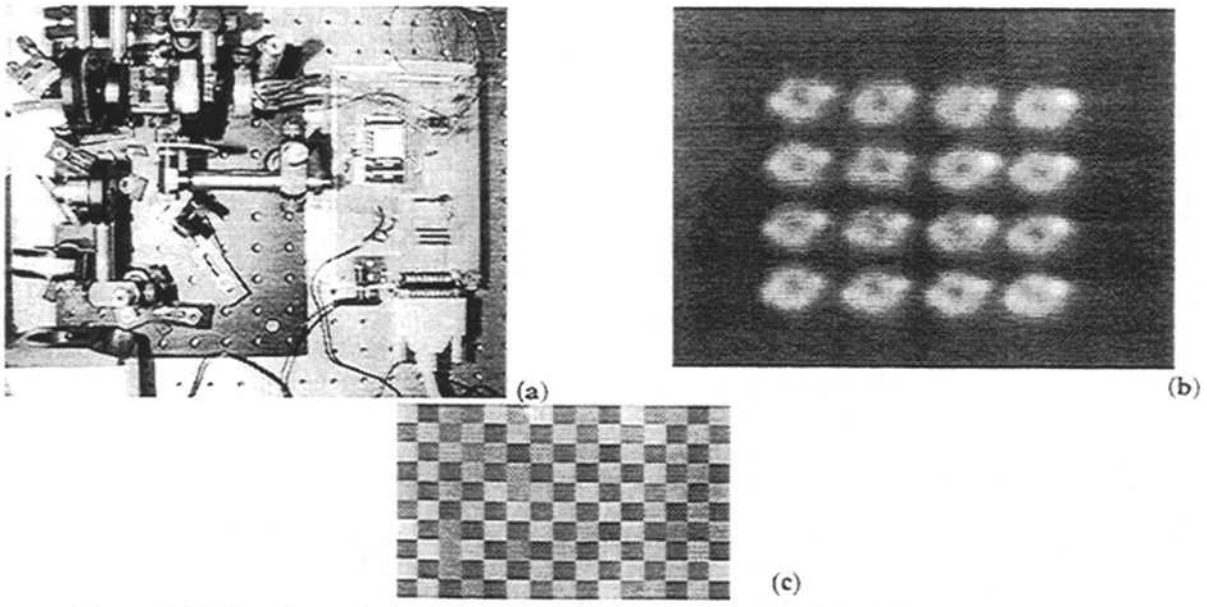

Figure 5: (a) Experimental setup. (b) 4x4 VCSEL array. (c) Detail of the hologram reconstructed.

Reference: [1] M. Motomura, Y. Aimoto, A. Shibayama, Y. Yabe, M. Yamashina, "An Embedded DRAM-FPGA Chip with Instantaneous Logic Reconfiguration", NEC Corporation, JAPAN