High-Responsivity Optical FET's Fabricated on a FET-SEED Structure

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Abstract— **Optical detectors with responsivity of 1000 A/W and response time of 10 μs at 50 nW optical input power were fabricated using the AT&T FET-SEED process.**

I. Introduction

THE integration of GaAs–AlGaAs field-effect transistors and self-electrooptic effect devices (FET-SEED's) in a batch fabrication process [1] has been applied to the fabrication of optoelectronic smart pixels [2]–[4] and other applications [5]. In this paper we consider the use of this process to fabricate optical neuron arrays. A high-density neuron array requires optical detectors with high gain [6]. To the knowledge of the authors, such high gain detectors using the FET-SEED process have not been reported before. In this paper, we report the successful demonstration of using the FET's by AT&T FET-SEED process as a high gain optical detector suitable for neuron array applications. These detectors have an actual responsivity as high as 10000 A/W and a fall time on the order of 10 μs. The dark current is controlled by bias gate voltages and can be below 1 nA.

II. Structure and Fabrication

The FET structure is schematically shown in Fig. 1. Detailed description was given by T. K. Woodward *et al.* [2]. The channel consists of a 100 Å n-doped GaAs conducting layer and a 900 Å AlGaAs undoped spacer located between the gate electrode and the channel. The source and drain contacts are made to the channel through ohmic contacts which penetrate from the top n+ GaAs layer to the n-channel layer. Under the channel, there are a multiple-quantum-well (MQW) region and a p+ conducting layer. The p+ layer is electrically addressable by Be ion implantation, which acts as a backgate to the FET. As we will see later, this backgate plays a very important role in the operation of the FET as an optical detector. The FET has a gate width of 10 μm and a length of 1 μm, with a spacing of 2 μm between the gate and the ohmic contacts. These devices were fabricated by AT&T Bell Laboratories and made available through the FET-SEED workshop organized by the Consortium for Optical and Optoelectronic Technologies for Computing (CO-OP).[1]

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[1]More information on CO-OP and the FET-SEED workshop can be obtained from Dr. Ravi Athale at the ECE Department, George Mason University, Fairfax, VA 22030 USA.

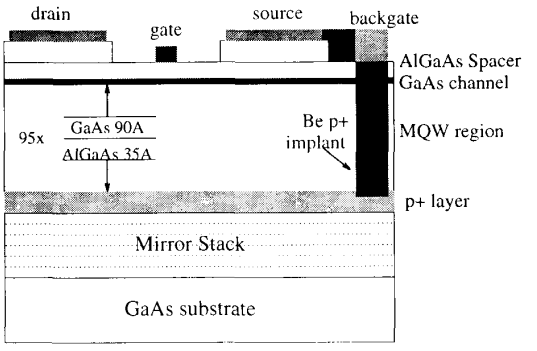

Fig. 1. Cross section of the FET. The MQW region under the n+ channel is designed for modulator/SEED, and can be used as the absorption layer for optical detectors.

III. Results

The FET's are depletion-mode transistors, where the threshold voltage is typically −1.2 V. Their source-drain conductance can be controlled electrically by applying a voltage to either the gate or backgate. In order to use this FET as an optical detector, we biased either the gate or the backgate to the subthreshold regime so that the dark current is low, typically below 1 nA. By shining light on the FET gate region, we observed a dramatic increase in the channel current, as shown in Fig. 2.

From this I–V curve, we calculated the responsivity of the FET detector by simply dividing the photocurrent by the optical input power. For 21 nW optical input, we measure a photocurrent of more than 21 μA at $V_{ds} = 2.5$ V, which gives us a gain of over 1000 A/W. The focused light spot is much larger than the gate region—the focused spot is estimated to have a diameter of 30–40 μm while the gate opening is only 4×10 μm^2—and therefore most of the light is wasted outside the gate region. Thus, the actual detector gain can be about an order of magnitude higher if the illuminating light is focused to a small spot. This can be achieved by using better light source and focus optics or increasing the gate opening area using interdigital gate geometry as we previously demonstrated with GaAs Optical FET fabricated through MOSIS [7].

Fig. 3 shows the responsivity result under different gate bias voltages with the backgate contact floating. We get a high gain when the optical input power is low, typically in the order of 1000 A/W for input power lower than 50 nW.

Since the conducting layer of the FET is so thin (only 100 Å) it is basically transparent to the optical input signal. Therefore, the absorption must happen in the MQW region underneath. We verified this by measuring the spectral responses of the

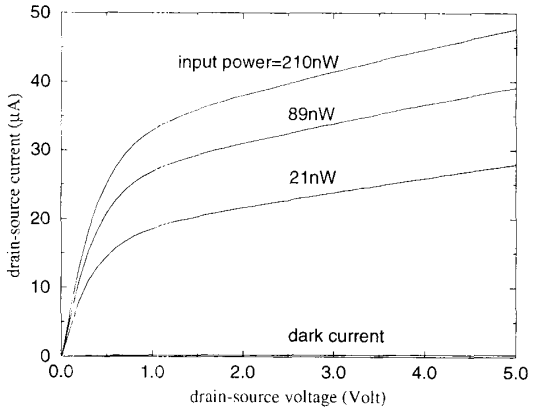

Fig. 2. IV characteristics of the optical FET. Gate voltage is fixed at -1.5 V, while the backgate is floating. The dark current is 0.20 μA at $V_{ds} = 2.5$ V.

optical FET and the MQW photodiode. The two spectral responses have almost identical exciton peak and absorption edge.

When light is absorbed in the MQW region, electron-hole pairs are generated. Under the built-in electric field, holes are swept into the backgate layer while electrons go to n-channel. In the case where the gate voltage is fixed and the backgate is floating, the accumulation of holes in the backgate region charges up its voltage just as a p-i-n photodiode. As a result, the positive voltage that builds up on the backgate contact increases the conductance of the FET dramatically. The measured photo-induced positive voltage on the backgate is very similar to that of a typical photodiode. When the input power is low, we observe a sharp increase in the backgate voltage, which gives very high responsivity. As P_{in} becomes stronger, the backgate voltage grows logarithmically. In return, the responsivity decreases to below 500 A/W. Based on the photo-induced backgate voltage measurement and the measured backgate transconductance, we calculated the expected photocurrent. The result agreed with our experimental measurement.

We measured the time response of the optical FET by illuminating the gate region with a square-wave optical signal. This signal changes from zero input to variable high levels. We observed asymmetric rise and fall responses: the rise time is faster than the fall time. The exact reason for this behavior is yet not clear. Fig. 4 shows the measured result as a function of signal high level. We can estimate the expected rise time as

$$\Delta t \simeq \frac{C\Delta V}{I}$$

where C is the capacitance of the i-MQW region, ΔV is the voltage swing on the backgate, and I is the photogenerated charging current. For 215 nW optical input power, if we use 30 μm as the diometer of the focus spot, only 12.2 nW power is absorbed in the MQW region through the 4×10 μm^2 window on the surface, which gives us a charging current of 4.88 nA assuming the efficiency of the MQW photodiode is 0.4 A/W. The total area under the FET is 16×10 μm^2, giving us a capacitance of 16.2 fF. From our measurement, the generated voltage swing is 0.56 V for $P_{\text{in}} = 215$ nW. Based on these

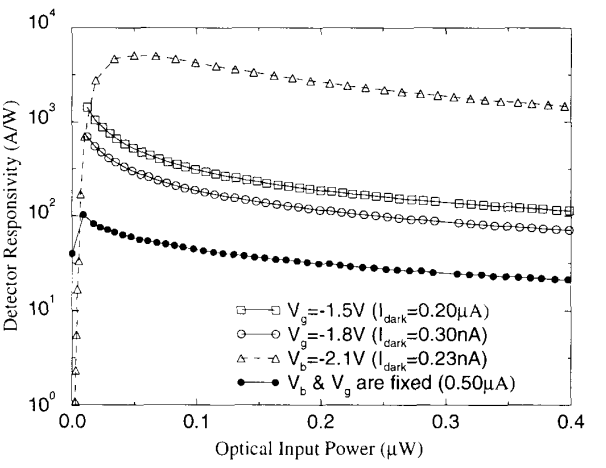

Fig. 3. Responsivity of the optical FET with the backgate or the gate floating. Solid curves are plotted for different gate voltages with the backgate floating. The dashed curve is with the gate floating. In comparison is the filled curve when both gate and backgate voltages are fixed.

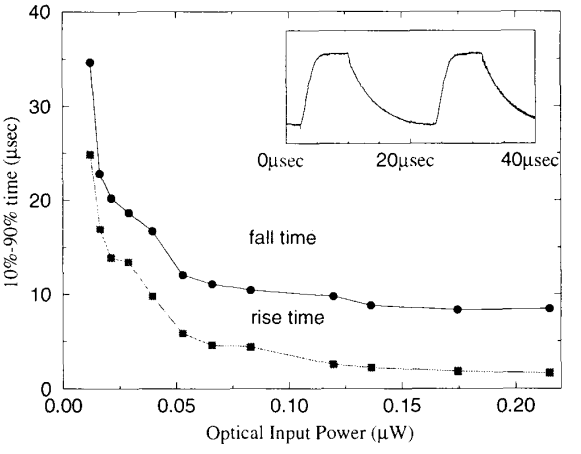

Fig. 4. Time response of the optical FET with the backgate floating. Gate voltage is fixed at -1.8 V, which gives a dark current of 0.30 nA.

numbers, we can calculate the rise time to be 1.87 μs, which is very close to our measured 1.65 μs result.

This optical FET can also be operated with the gate floating while the dark current is controlled by backgate bias. The mechanism is slightly different. Since the backgate is now electrically connected, photo-generated holes will be swept away while electrons are trapped at the n-channel. In order to maintain charge neutrality, we believe positive charges are generated at the gate contact through surface states. As a result, the gate-voltage increases and huge photocurrent is observed. Fig. 3 also shows the measured result for this operation mode. Again, the FET detector has high gain but with different behavior. We observe a peak in the responsivity curve that is attributed to the peak of FET transconductance when plotted as a function of gate voltage [3]. Measuring the photo-induced gate voltage, we calculated the expected photocurrent and it agreed well with experiment measurement. The optical FET shows longer response time, in the order of 100 μs, most likely

because surface states are involved when operating in this mode. If both the gate and the backgate voltages are fixed, this photo-induced gate/backgate voltage mechanism is no longer valid, and the detector gain is low as we can see from Fig. 3.

IV. Conclusion

We were able to use the FET of the AT&T FET-SEED process as a high responsivity detector. It can be operated in two modes: backgate floating or gate floating. The dark current can be controlled by the electric bias and can be as low as 0.30 nA. For the backgate floating case, responsivities as high as 1000 A/W is achievable and the response time is in the order of 10 μs. Considering the large size of the illuminating optical beam relative to the size of the gate opening area, we believe the actual FET responsivity is in the order of 10 000 A/W.

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