# Monolithic Optoelectronic Circuit Design and Fabrication by Epitaxial Growth on Commercial VLSI GaAs MESFET's

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***Abstract*— A technique for realizing large-scale monolithic OEIC's, which involves epitaxially growing GaAs-based heterostructures on fully metallized commercial VLSI GaAs MESFET integrated circuits, has recently been reported. In the initial work the circuits and LED's occupied distinct halves of a chip, the dielectric growth window was wet-etched after circuit fabrication, and the LED's required both n and p ohmic contacts to be formed after epitaxial growth. In this letter we report the use of standard foundry process etches to open dielectric growth windows intermixed with circuitry and the growth of n-side-down LED's on a source/drain ion-implanted $n^+$ region serving as the n ohmic contact. A winner-take-all neural circuit is demonstrated using these advances, which are important steps toward realizing higher levels of circuit integration.**

IT HAS RECENTLY been reported that fully processed, commercially available (Vitesse Semiconductor Corp. through MOSIS) VLSI GaAs MESFET integrated circuits are electrically stable after thermal cycles of up to 3 h at 500 °C with minimal shifts after 5 min at 600 °C followed by 5 h at 530 °C [1]–[5], [8] (in [8], an extensive experimental and modeling study of Vitesse HGaAs3 device and circuit time-temperature stability; upper-level interconnect and ohmic-contact metallurgical reactions are detailed). A novel optoelectronic integration technique was proposed based on this circuit stability and consequently the monolithic integration of LED's and GaAs circuits by molecular beam epitaxial (MBE) growth, to form an optoelectronic thresholding circuit, was demonstrated [1], [4]–[5]. In the initial work the circuits and LED's occupied distinct halves of the chip, one large dielectric growth window was wet etched after circuit fabrication and the LED's required both n and p ohmic contacts to be formed after growth. Advances in these areas are required to achieve higher levels of integration and thus to take full advantage of the highly uniform VLSI circuitry inherent to this and other optoelectronic integration techniques [6]–[7]. In this letter we describe the design and fabrication of LED's grown in dielectric growth windows intermixed with circuits, the use of standard MOSIS/Vitesse process etches to open the dielectric growth windows, and the n-side down LED growth on a source/drain (S/D) ion-implanted $n^+$ region, serving as the $n$ ohmic contact, to form a three-unit winner-take-all (WTA) neural circuit.

The electronic portion of the WTA circuit was designed using standard Vitesse HGaAs3 design rules. The regions of the chip slated for LED growth were represented in the layout by specifying a dielectric growth window and a S/D $n^+$ implant. Dielectric growth windows, which are the regions on the chip where the dielectric stack is to be etched away to expose the underlying GaAs substrate, which serves as the seed crystal for subsequent epitaxial growth, are specified by stacking two standard etch mask layers: the passivation etch layer which cuts through the top overglass and the street-clear etch layer which cuts through interlevel-metal dielectric layers. To produce a vertical dielectric sidewall with $CHF_3/CF_4$/He reactive-ion etching (RIE), these layers were identically sized and aligned. The S/D $n^+$ implanted region (typically 200 $\Omega/\square$) beneath the dielectric growth window region together with a standard ohmic contact (typically 0.3 Ω–mm) forms the bottom-side $n$ ohmic contact. The design was fabricated at the foundry and returned unpackaged. For post-foundry processing ease the chips are typically 3 mm × 3 mm (present case) or larger. Fig. 1(a) is an artist's perspective of the chip as received from the foundry.

In preparation for growth, the S/D $n^+$ implanted GaAs at the bottom of the dielectric growth windows was cleaned. $CF_4/O_2$ RIE and an ultrasonic bath of buffered oxide etchant removed the residual material (a Teflon-like film) and dielectric at the bottom of the well. The chips were degreased and mounted with indium on a molybdenum block around the perimeter of a quarter wafer of bulk $n^+$ GaAs which served as a pyrometer source, RHEED crystal, and control sample. The block temperature was ramped at 15 °C/min up to 600 °C until the native oxide on the bulk GaAs desorbed. Five minutes later the native oxide in the dielectric growth windows on the chips was assumed to be desorbed. This is short enough to not significantly effect the MESFET's but it may impact the tungsten-plated aluminum interconnect metallization [8]. Thus low-temperature hydrogen-plasma native oxide removal

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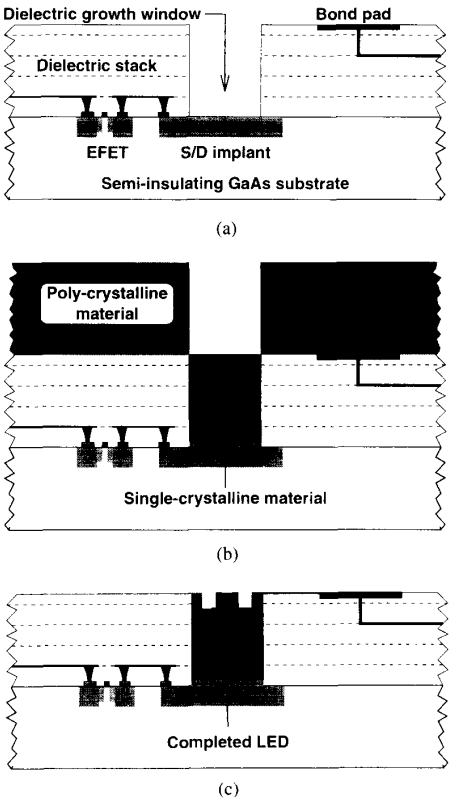


Fig. 1. Artist's perspective of the three stages of optoelectronic circuit fabrication: (a) Custom designed chip with dielectric growth window as received from the foundry. (b) Single-crystal material grows in the dielectric growth window and polycrystalline material deposits on the top overglass and bond pads. (c) Planarizing polycrystalline etch, current-confining mesa etch, $Si_3N_4$ chemical vapor deposition, and AuZn–Au p-ohmic contact evaporation completes the fabrication sequence.

would be prefered [9]. The $n^+$ GaAs growth was initiated and the temperature was ramped to 530 °C where the LED heterostructure was grown with a reduced As flux. The total growth thickness was 4.2 $\mu$m (4.5 h) and approximately aligns the top surface of the single-crystalline GaAs with the top of the dielectric sidewalls. The heterostructure consisted of a 15 period $n^+$ $Al_{0.3}Ga_{0.7}As$(5 nm)–GaAs(5 nm) superlattice, 2.5 $\mu$m $n^+$ GaAs buffer, 0.3 $\mu$m n $Al_{0.3}Ga_{0.7}As$ barrier, 0.6 $\mu$m $p^-$ GaAs active region, 0.7 $\mu$m p $Al_{0.3}Ga_{0.7}As$ barrier, and a 0.1-$\mu$m $p^+$ GaAs contact. Single-crystalline material grows in the windows and polycrystalline material deposits on the top overglass and bond pads as illustrated in Fig. 1(b).

After the chips were unloaded and the backside indium was stripped, the growth windows were photolithographically protected with photoresist (with a 5-$\mu$m overhang around the perimeter) and the polycrystalline material was wet etched with 1:1:5 $H_3PO_4$:$H_2O_2$:$H_2O$ to expose the overglass and bond pads. The photoresist was then stripped resulting in a planar surface suitable for standard GaAs processing, including high-resolution contact lithography [10]. Current-confining mesas were formed by phosphoric acid based wet-etch, electrically insulating $Si_3N_4$ was chemical vapor deposited (CVD) in 3 min at 610°C (lower-temperature plasma enhanced CVD would be prefered), and AuZn–Au p-ohmic contacts were evaporated. See Fig. 1(c). A proton implanted annular ring, resulting in high-resistivity material at the periphery of the epitaxial well, would make the current-confining etch and dielectric deposition unnecessary thereby simplifying processing and maintaining superior planarity. To study the completed LED growth region, a cross-sectional scanning electron micrograph was taken. The top of the dielectric sidewall and the top of the LED are in approximate alignment, the polycrystalline material has been successfully removed from the dielectric stack, and an approximately 5-$\mu$m-wide transition region exists between the dielectric sidewall and good quality epitaxy.

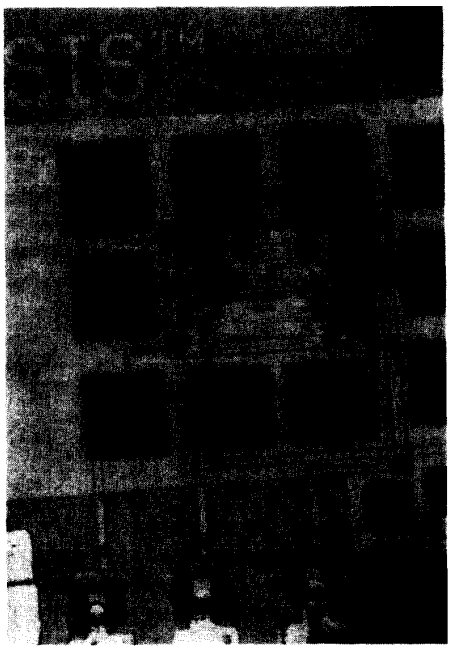

Fig. 2. Optical picture of the three-unit WTA circuit with three 40 $\mu$m × 1 $\mu$m optical E-MESFET's surrounded by bond pads at the top and the three 50 $\mu$m × 50 $\mu$m epitaxial wells with grown LED's at the bottom.

Fig. 2 is an optical picture of the three-unit WTA circuit showing the three 40 $\mu$m × 1 $\mu$m optical enhancement-mode MESFET's (OPFET's) surrounded by bond pads at the top, numerous MESFET's and three 50 $\mu$m × 50 $\mu$m epitaxial wells with LED's at the bottom of the picture. Dozens of such optoelectronic circuits are also on this chip and surround the WTA circuit. All electrical devices on the chip function, but with some degradation (i.e., saturation current reduced by 10%) caused by long periods at temperatures in excess of 500 °C. While no such shifts would be present for growth temperatures below 500 °C, which is very desirable, these changes are predictable and can be offset by proper design scaling (e.g., 10% gate width increase) [2], [8]. This is not possible for growth temperatures exceeding 530 °C. I-V and L-I curves from LED's fabricated in the epitaxial wells and in the bulk control wafer show no discernible differences ($V_{TH}$ typically 1.2 V), as reported for previous LED integrations

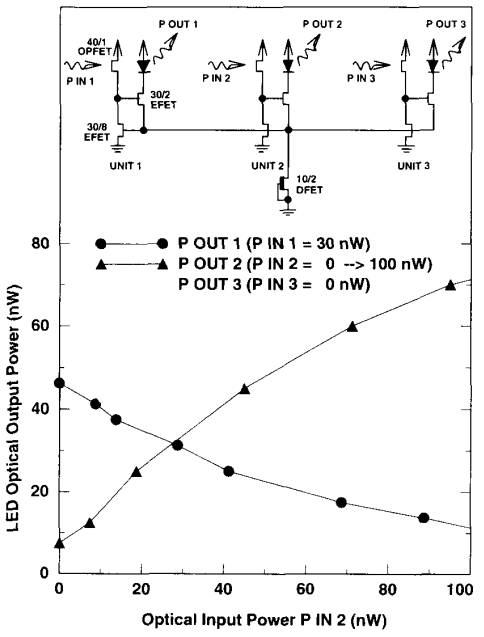


Fig. 3. Plot of the WTA cross-over characteristics where 30 nW of optical power was applied to the first unit, the optical power was swept from 0–100 nW on the second unit, and no optical power was applied to the third unit. The winning unit LED output power is greater than the other branches for input powers greater than 30 nW, thus demonstrating the correct optoelectronic winner-take-all circuit functionality. Schematic inset: Each unit of the three-unit optoelectronic winner-take-all circuit consists of an OPFET photodetector, an epitaxially grown LED emitter and two EFET's which compare signal intensities (dimensions in W [$\mu$m]/L[$\mu$m]). A single depletion-mode MESFET serves a current sink.

[5]. The efficiencies are also indistinguishable and are low (typically 0.01% at 100-$\mu$A and 0.03% at 1 mA) due to poor current confinement. Similar LED's grown at 700 °C and identically processed had equally low efficiencies confirming that the low efficiencies are inherent in the structure, not in the integration.

Each unit of an optoelectronic WTA circuit consists of a photodetector, an emitter or modulator and analog circuitry. The unit which receives the largest optical input should be the only unit to emit or modulate light. In the present design a high-gain OPFET [5] with a floating gate and 10 $\mu$m source-to-gate and 10 $\mu$m drain-to-gate separation serves as the photodetector, an epitaxially grown LED serve as the emitter and two EFET's per unit compare signal intensities as shown in the schematic inset of Fig. 3. Specific WTA circuit design and performance issues will be the subject of another publication. Fig. 3 is a plot of the WTA cross-over characteristics where 30 nW of optical power was applied to the first unit, the optical power was swept from 0–100 nW on the second unit and no optical power was applied to the third unit. The winning unit LED output power (P OUT 2) is greater than the other branches for input powers (P IN 2) greater than 30 nW, thus demonstrating the correct optoelectronic WTA circuit functionality [11]. All possible input combinations functioned properly and measured characteristics agreed quite well with simulations.

By epitaxially growing LED's on custom designed commercial VLSI GaAs E/D MESFET integrated circuits with S/D $n^+$ regions beneath foundry etched dielectric growth windows, a three-unit optoelectronic winner-take-all circuit has been successfully demonstrated. With these integration advances, large-scale high-density optoelectronic circuits [12], [13] and systems [14] fabricated by epitaxially growing heterostructures lattice-matched to GaAs on VLSI GaAs circuits should now be possible.

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