lon or plastic partitions, or on tips of glass pipettes. However, unsatisfactory stability and reproducibility of these BLMs not only hampered the research in ion channel characterization but also prevented the realization of a practical BLM-based biosensor for routine applications [1]. It is known that the shape and physical dimensions of the aperture effect the stability of the BLM [2]. In this work, silicon micromachining is used to fabricate reproducible miniature apertures over photosensitive polyimide (PPI) layers (septa), with highly controllable dimensions. PPI, having a high level of planarization, chemical inertness, a low dielectric constant and good mechanical strength, is a very suitable material to be used as BLM septa. Apertures, of ~ 5 μm thickness and ~ 40 μm diameter in PPI septa suspended over thick silicon rims were realized. Fabrication process includes double-side oxide growth on the wafer, spin-coating the PPI and its patterning, back surface anisotropic window etching, and a final cleaning step. Apertures with high circular symmetry were fabricated using the above process. BLM is formed by dropping a small amount of phospholipid-alkane solution over the PPI aperture. Initially few μms thick membrane, spontaneously thins down to an ~ 50 Å thick BLM. Specific capacitance measurements of these BLM's revealed stability of upto 50 hours. Successful incorporation of Alamethicin channel and AChR activities into these membranes, further proves their bilayer nature. To our knowledge, this is the first study of its kind that reports a very stable BLM formation on a silicon-based device and subsequent ion channel incorporation. Since the process presented here is totally compatible with a standard CMOS technology, PPI septa can be used in a future class of miniature BLM-based biosensor with on-chip measurement and processing circuitry.

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[1] U. J. Krull, and M. Thompson, "The lipid membrane as a chemical transducer," *IEEE Trans. Elect. Dev.*, vol. 32, pp. 1180-1184, 1985.

[2] S. H. White, "Analysis of the torus surrounding planar lipid bilayer membranes," *Biophys. J.*, vol. 12, pp. 432-445, 1972.

VIA-3 MBE Regrowth of LED's on VLSI GaAs MESFET's

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We demonstrate for the first time the regrowth and monolithic integration of heterostructure LED's on fully processed VLSI GaAs MESFETs. Commercially available, self-aligned VLSI GaAs MESFET's, with tungsten-based refractory-metal Schottky gates, nickel-based refractory-metal ohmic contacts, and aluminum interconnection metallization, have been shown to be stable after 3 h at 525°C ± 10°C[4,5]. Thus, it is now possible to regrow optical sources on fully processed MESFET circuitry with lowered-temperature molecular beam epitaxy (MBE). This allows one to build high density, complex electronic circuitry with optical inputs and optical outputs. Such optoelectronic circuits are useful for high speed optical communications, optical computing, or smart pixels.

Our specific circuit application is for optoelectronic neuron arrays in optical neural networks. Each neuron circuit has two photodetectors to receive the optical inputs, electronic circuits to perform a nonlinear thresholding function on the photocurrent and a LED to transmit the output of the neuron. A typical optical neural network has neuron densities of 1×10^4 neurons/cm^2. This puts stringent requirements on the power dissipation and uniformity of the circuit, but these requirements can be met with an industrial fabrication process [6].

Each branch of the circuit accepts two optical inputs, I_1 and I_2. If I_1 equals I_2 then the gate voltages of both MESFETs are $V_d/2$ which turns both transistors off. The current sinking transistor draws its current entirely from the LED. If I_1 or I_2 are not equal, then the gate voltage on one of the two MESFET's will be high (V_d) turning the transistor on and thus shorting the LED. Therefore, the LED is only turned on when $I_1 \approx I_2$. The photodetectors are enhancement mode MESFET's with the gate connected to the source. These optical FETs provide the nonlinear IV characteristics required.

The electronic circuit was designed and fabricated through MOSIS using Vitesse Semiconductor Corporation's HGaAs2 process. Half of the chip was left blank for the LED regrowth. The fabricated chip was electrically tested and then the dielectric stack covering the blank area was removed using HF. A superlattice was grown to impede the propagation of defects from the semi-insulating substrate. The LED structure consists of double heterostructure nAlGaAs/iGaAs/pAlGas layers. The total growth time was nearly 4 h at the lowered growth temperature of 530°C. The polycrystalline GaAs that covers the portion of the chip where the circuits are, was removed by masking off the crystalline GaAs with photoresist and then etching with a phosphoric etchant. The LED was fabricated and connected to the circuit after the regrowth.

The circuits were tested electrically after the growth and their performance was compared to the original circuit. The DFET saturation voltage is the same, whereas the saturation current has decreased by approximately 10%, and the source-to-drain resistance has increased by 40%. The peak photoluminescence (PL) of the epitaxial material was 10% less than the PL of a control blank wafer that was grown at the same time. LEDs fabricated on the chip and the control wafer had comparable efficiencies and the desired nonlinear optoelectronic thresholding function has been achieved. Thus, we have demonstrated for the first time an extremely attractive regrowth technology for

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high density optoelectronic circuits which takes full advantage of commercial VLSI GaAs MESFETs.

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Krishna V. Shenoy was supported by a National Science Foundation Graduate Fellowship and a Fannie and John Hertz Foundation Graduate Fellowship.

Annette C. Grot was supported by a National Science Foundation Graduate Fellowship.

[1] K. V. Shenoy, C. G. Fonstad, Jr., *et al.*, *LEOS '92 Conf. Proc.*, Boston, MA, Nov. 16-19, 1991, pp. 594-595.
[2] K. V. Shenoy, C. G. Fonstad, Jr., and J. M. Mikkelson, submitted to *IEEE Electron Device Lett.*, Dec. 1992.
[3] S. Lin, A. Grot, J. Luo, and D. Psaltis, to be published in *Appl. Opt.*, 1993.

VIA-4 Characterization and High-Speed Digital Application of GaAs MESFET's on Substrates—S. Onozawa, N. Yamamoto, T. Kimura, Y. Sano, and M. Akiyama, Oki Electric Industry Co., Ltd., 550-5 Higashiasakawa-cho, Hachioji, Tokyo 193, Japan Tel. 0426-63-1111.

Crystallinity of GaAs epilayers on Si has shown a great improvement owing to the 2-step growth technique [1] and many devices fabricated on the GaAs/Si substrates have been reported. However, there still exist several problems due to the nature of the substrate for submicron devices. The most serious is a strong residual stress of about 10^9 dyn/cm^2 between GaAs and Si, which induces piezoelectric charges and causes a large shift of threshold voltage of a few hundred mV for submicron gate GaAs MESFET's. We have solved this problem by introducing p-layer (C^+: 140 keV) burried under the n-type channel (Si^+: 20 keV) in the n^+ self-alignment technique with refractory W-Al gate [2]. The device fabricated with a 0.3 μm-gate showed good saturation characteristics and high transconductance of 498 mS/mm, of which value is only 4% smaller than that of a control device on a GaAs substrate. These results indicates that the crystallinity of the GaAs epilayer such as the electron mobility is good enough for the high speed device application.

Then, uniformity becomes the next requirement for the large scale integration. We evaluated, for the first time, the microscopic uniformity of the device on GaAs/Si using 60 μm $\times$ 60 μm-pitch FET arrays, and found that it is remarkably improved by introducing the p-layer. The standard deviation of the threshold voltage for 900 FET's (with p-layer) within an area of 3.6 $\times$ 0.9 mm^2 was as small as 20.3 mV, which is about a half of that for the control device (without p-layer).

Finally, to evaluate the dynamic characteristics, we fabricated a direct-coupled FET logic (DCFL) ring oscillator using the 0.3 μm-gate MESFET on the GaAs/Si substrate. As a result, the propagation delay was as small as 19.9 ps/gate at a supply voltage of 2 V. We also fabricated an 1/2 frequency divider. The circuit, designed by the memory-cell type flip-flop (MCFF) [3], showed a stable operation up to 10 GHz, which is the highest speed ever reported for GaAs/Si devices.

In summary, we optimized the device structure to suppress the short channel effect due to the residual stress in GaAs/Si substrates and improved the microscopic uniformity, then successfully fabricated a high speed digital circuit. From the results obtained we have proved that the technology of GaAs/Si can provide large and high-quality substrates for high speed large scale integration.

[1] M. Akiyama *et al.*, *J. Cryst. Growth*, vol. 77, p. 490, 1986.
[2] M. Tsunotani *et al.*, *IEDM Tech. Digest*, pp. 700-703, 1988.
[3] M. Shikata *et al.*, *GaAs IC Symp. Tech. Digest*, pp. 67-70, 1985.

VIA-5 Demonstration of Monolithic Co-Fabrication of $Y_1Ba_2Cu_3O_{7-\delta}$ and CMOS Devices on the Same Sapphire Substrate—P. R. de la Houssaye, M. J. Burns,* W. J. Ruby,* S. D. Russell, S. R. Clayaton, G. A. Garcia, L. P. Lee,* NCCOSC RDTE DIV (NRaD) 553, 49375 Ashburn Rd., Room 2, San Diego, CA 92152-7633.

We report the first fabrication of active semiconductor and high temperature superconducting (HTS) devices on the same substrate. Complementary Metal-Oxide-Semiconductor (CMOS) transistors were fabricated on the same sapphire substrate as either YBCO flux-flow transistors (FFT's) or YBCO superconducting quantum interference devices (SQUID's). All devices functioned as expected at 77 K without degradation, demonstrating that a compatible process has been found to monolithically integrate adjacent CMOS and HTS devices.

In the seven years since the discovery of high-temperature superconductivity, the field of superconductive electronics has undergone explosive development. Due to difficulties in growing films directly on silicon, copper and oxygen contamination of the silicon layers during growth, and the high temperature environments seen in HTS growth, it has not been fully integrated with semiconductor based technology. Research has been focused on the use of superconducting interconnects between integrated circuits, which could lower chip power dissipation, reduce necessary interconnect width and pitch, and reduce dispersive loss. Several attempts have been made to fabricate HTS circuits or devices directly on Si or other semiconductor surfaces [1], [2]; these layers were of low quality and were stress limited, and no devices were fabricated in the layers.

CMOS thin-film silicon on sapphire (SOS) devices utilizing improved silicon films have achieved performance equal to or better than bulk CMOS devices [3]. For low temperature, low power operation, CMOS SOS has a number of advantages over other silicon technologies [4]. Additionally, one of the best substrates for growth of YBCO layers for superconducting devices is sapphire.

Fabrication of the thin-film SOS CMOS on sapphire was performed first. Further details relating to the CMOS pro-

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