Optically Reconfigurable Gate Array

Jose Mumbru, George Panotopoulos, Demetri Psaltis
Department of Electrical Engineering
California Institute of Technology

Xin An, Gan Zhou, Fai Mok
Holoplex Inc.

Abstract

Reconfigurable processors, like the Field Programmable Gate Arrays (FPGA's), open new computational paradigms where the processor is able to tailor its internal structure to better implement a given application. A typical FPGA consists of an array of configurable logic blocks and a mesh of interconnections fully programmable by the user to perform a given application. By just changing its internal connectivity, the FPGA can implement a totally different new function. However in most of the applications, the FPGA is configured only once and used as coprocessor to carry out some highly complex or time-consuming computation. The reason for such limitation is the small communication bandwidth between the FPGA chip and the external memory, usually ROM, where the configuration data is stored.

The Optically Programmable Gate Array (OPGA)[1], **figure 1**, an enhanced version of a conventional FPGA, can overcome this problem. The OPGA utilizes a holographic memory accessed by an array of VCSELs to program its logic. The on-chip logic has been complemented with an array of photodetectors to detect the configuration template recorded in the memory. Combining spatial and shift multiplexing to store the configuration pages in the memory, the OPGA module is very compact and has extremely short configuration time allowing for dynamic reconfiguration. The reconfiguration capability of the OPGA can be applied to solve more efficiently problems in pattern recognition and database searches.

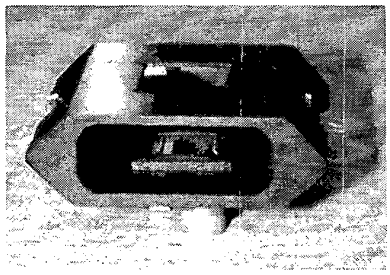

Figure 1. OPGA module package

Reference:

[1] "Optically Reconfigurable Proccessors", J. Mumbru, G. Zhou, S. Ay, X. An, G. Panotopoulos, F. Mok, and D. Psaltis, SPIE Critical Review, 1999 Euro-American Workshop on Optoelectronic Information Processing, Vol. 74, pp. 265-288, Colmar, France, June, 1999.

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