Grayscale topography engineering for 2D nanoelectronics

Master thesis / Semester project

(Section: Microengineering – Electrical Engineering - Materials Science)

While nanolithography has historically focused on downscaling, there is now a growing interest in grayscale nanolithography for introducing or enhancing functionality in micro-nanodevices applied for optics and fluidics. **Grayscale thermal scanning probe lithography** (t-SPL) achieves single-digit nanometer spatial resolution and sub-nanometer depth control, but it has limited scalability. We combine t-SPL with **nanoimprint lithography** to replicate high-resolution grayscale nanostructures on large surfaces by step-and-repeat process [1, 2]. For the next generation of nanoelectronics, we use these deterministic grayscale topographies for **strain engineering of 2D materials** as they hold the potential to replace silicon in transistors with sub-10 nm channel lengths.

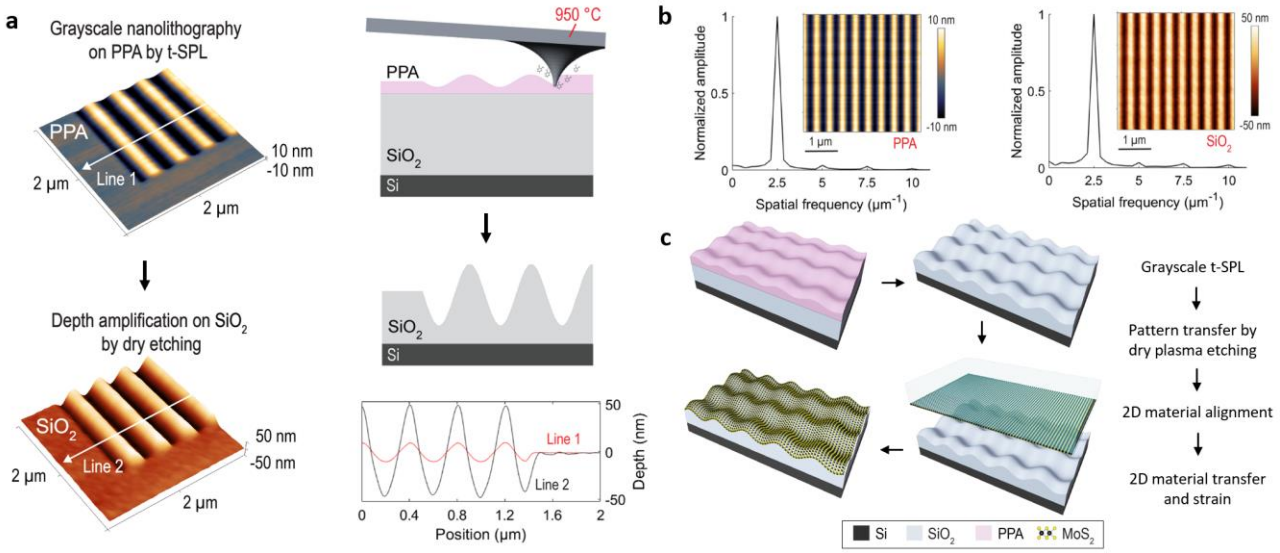

Figure 1: a AFM images and amplitude comparison of a sinusoidal pattern before (Line 1) and after (Line 2) dry etch transfer. **b** Fourier transforms of the measured topographies after t-SPL on PPA and transferred into SiO_2. **c** Fabrication process flow of grayscale dielectric nanostructures for 2D materials strain.

The main tasks in the project will be:

- Grayscale stamp fabrication by combining t-SPL and dry etching
- Nanoimprint lithography and metrology characterization
- 2D material strain characterization

Desired Skills:

- Autonomy
- Knowledge in cleanroom processes is a plus

References:

[1] Howell, Samuel Tobias, et al. "Thermal scanning probe lithography—A review." *Microsystems & nanoengineering* 6.1 (2020): 1-24.

[2] Erbas, Berke, et al. " Combining thermal scanning probe lithography and dry etching for grayscale nanopattern amplification." ChemRxiv (2023)

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