2.5D nanofabrication for silicon-based quantum computing

Semester project / Master project

(Section: Microengineering – Electrical Engineering – Materials Science – Physics)

LMIS1 takes on a new challenging project on the fabrication of quantum computing hardware. Solid-state quantum bit (qubit) and silicon-based hardware are promising ways to fabricate scalable quantum devices [1-4]. To do this, we aim at integrating industrialized metal-oxide-semiconductor fabrication processes with thermal scanning probe lithography (t-SPL). T-SPL is a non-conventional nanolithography technique to create 2.5D (grayscale) shapes with sub-2 nm vertical precision.

![Figure I](image)

**Figure I** (a) SEM image and (b) Cross-sectional TEM image of the area shown with a white dashed line in (a). L1 and L2 are the source and drain reservoirs. G1, G2, and G3 are three nanoscale gates [1]. (c) Heated scanning probe tip for nanoscale patterning. (d) Grayscale nanopatterning of Rolex Learning Center by t-SPL.

The main tasks in the project will be:
- Literature review of existing quantum computing hardware (25% of the time)
- One (or two) of the following tasks: (75% of the time)
  - Single dopant based quantum hardware design and process flow preparation for fabrication
  - Ion implantation simulation by using SRIM (Stopping and Range of Ions in Matter) software
  - Nanoscale mask fabrication with t-SPL patterning and dry etching for deterministic ion implantation

Desired Skills:
- Autonomy
- Knowledge in cleanroom processes and/or quantum computation is a plus

References:

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