# FPGA 2023 Chairs' Welcome

We are delighted to welcome you to the 31st ACM International Symposium on Field-Programmable Gate Arrays (FPGA 2023). We are particularly thrilled to welcome you back to the beautiful Monterey, as this edition marks the first time since February 2020 that we will meet in person after two virtual editions of the symposium. We hope you will be inspired by the spectacular coastline of the Monterey Bay to renew connections with long-time friends you may have only met online for too long and to make new acquaintances. We invite you to take maximum advantage of live presentations, interactions with authors and fellow researchers during coffee breaks and poster sessions, and all the social opportunities offered by an in-person conference.

The ACM International Symposium on Field-Programmable Gate Arrays is the premier forum for the presentation of new and exciting research on all aspects of FPGA technology. This year, the program committee received 82 papers that met submission guidelines and were reviewed. Overall, 28% of reviewed papers were accepted for presentation. This year's program extends over three days: on Sunday, we have 7 invited tutorials and workshops; the main symposium takes place Monday and Tuesday, comprising 17 full research papers (10 pages) and 6 short research papers (6 pages), as well as 2 invited keynotes. The keynotes have extended abstracts published in the proceedings. In addition, we have 24 submissions presented as posters that appear in these proceedings as an abstract.

As now customary, badges have been awarded for artifacts associated with accepted papers. Artifact evaluation is an opt-in process and accepted papers have an evaluator assigned who works with the authors to check the artifacts. The evaluator attempts to reproduce the results. Awarding of badges follows the ACM guidelines: https://www.acm.org/publications/policies/artifact-review-and-badging-current. Badges are published with the papers and highlighted in the program. Artifact evaluation promotes reproducibility and encourages reusable open source code from our community that meets high standards. A total of 7 papers were awarded 20 badges this year. We are grateful to this year's evaluators for their hard work and efforts in helping to make this a successful initiative.

We would like to thank the members of the Program Committee and the secondary reviewers, whose names appear on the following pages, for devoting considerable time and effort evaluating the submissions and providing thoughtful feedback to the authors. We would like to thank all of our session chairs for their help during the conference. Special thanks to the indispensable Joanne and John Lateulere for logistical support, to our fellow organizing committee team members, and to our sponsors for making FPGA 2023 possible.

Welcome to Monterey and to FPGA 2023!

**Paolo Ienne**
*General Chair*
EPFL, Switzerland

**Zhiru Zhang**
*Program Chair*
Cornell University, USA