Introduction to the Special Section on FPGA 2022

PAOLO IENNE, École Polytechnique Fédérale de Lausanne (EPFL), Switzerland

ACM Reference format:
Paolo Ienne. 2023. Introduction to the Special Section on FPGA 2022. *ACM Trans. Reconfig. Technol. Syst.* 16, 4, Article 56 (December 2023), 2 pages.
https://doi.org/10.1145/3618114

Field-Programmable Gate Arrays (FPGAs) are unique devices that achieve versatility not through software programming but via circuit reconfiguration; they are the prime example of commercial reconfigurable technology. Industrially, FPGAs have primarily excelled in implementing glue logic, in hardware system prototyping, and for low-volume, high-performance products. Increasingly, they are also recognized as general computational devices with untapped capabilities, and they are now employed in data centers to accelerate a broad variety of applications with the same reconfigurable hardware component, thus complementing traditional programmable computing engines. The ACM International Symposium on Field-Programmable Gate Arrays stands as the premier venue for presenting and discussing advancements in this exciting technology. This special section comprises extended versions of three papers presented at the 2022 ACM International Symposium on Field-Programmable Gate Arrays (FPGA 2022), which was held virtually due to the COVID-19 pandemic.

The first article, "A Reconfigurable Architecture for Real-time Event-based Multi-Object Tracking," by Gao et al., showcases FPGAs as embedded computing devices. The authors introduce *REMOT*, a reconfigurable event-based tracking hardware-software system designed for real-time multiobject tracking using an event camera input. Compared to a software baseline, REMOT achieves up to a 44-fold higher throughput and 35.4-fold higher power efficiency, illustrating the benefits of circuit configuration over software programmability.

The second article, "Logic Shrinkage: Learned Connectivity Sparsification for LUT-based Neural Networks," by Wang et al., extends previous work by some of the same authors, focusing on binary neural networks that naturally leverage FPGA resources. In this article, the authors propose *logic shrinkage*, an automated search for LUT-based neural network inference accelerators in which LUT sizes and inputs are learned during training. This work demonstrates how FPGAs' flexibility can be harnessed in innovative ways distinct from traditional digital circuit design.

The final article is "RapidStream 2.0: Automated Parallel Implementation of Latency Insensitive FPGA Designs through Partial Reconfiguration," by Guo et al. This article addresses a critical FPGA issue—the lengthy compilation cycle—particularly problematic in certain contexts. It presents an enhanced version of *RapidStream*, a compilation framework that takes a latency-insensitive C/C++

Author's address: P. Ienne, Ecole Polytechnique Fédérale de Lausanne (EPFL), School of Computer and Communication Sciences, 1015, Lausanne, Switzerland; e-mail: paolo.ienne@epfl.ch.

1936-7406/2023/12-ART56
https://doi.org/10.1145/3618114

program, partitions the design for parallel placement and routing, and then integrates the partitions to generate a fully placed and routed implementation in significantly less time than a monolithic placement and routing would need. RapidStream highlights how progress can still be made on crucial FPGA design automation challenges.

I extend gratitude to the authors for their high-quality submissions and to the anonymous reviewers for their insightful guidance throughout the review process. I also acknowledge the support of Michael Adler (FPGA 2022 General Chair) during the conference paper selection and the contributions of Deming Chen, Angelique Ly, and Jeffery Goeders in preparing this special section. I trust you will find this collection enjoyable to read.