Improved analytical modeling of polysilicon depletion in MOSFETs for circuit simulation

Jean-Michel Sallese [a,*], Matthias Bucher [a], Christophe Lallement [b]

[a] *Swiss Federal Institute of Technology, Lausanne (EPFL), Electronics Laboratory, ELB-Ecublens, CH-1015 Lausanne, Switzerland*
[b] *ERM-PHASE, Ecole Nationale Supérieure de Physique de Strasbourg, Boulevard Sébastien Brant, F-67400 Illkirch, France*

Abstract

Polysilicon gate depletion is an important effect that degrades the circuit performance of deep submicron standard CMOS technologies. A new approach to analytically modeling the polysilicon depletion effect on drain current and transconductances as well as node charges and transcapacitances is presented. The model is based on a clear physical analysis of the charges in the MOS transistor structure. Using the modeling framework and the fundamental variables of the EKV MOS transistor model formalism and that of the related charges models, a continuous model is achieved that is valid in all operating regions from weak inversion to strong inversion and from non-saturation to saturation. The asymptotic behavior of the transcapacitances is improved with respect to former model formulations. Only the doping concentration in the polygate is used in addition to the other physical device model parameters. The model shows excellent results in comparison with a surface potential based numerical model and 2D numerical device simulation. The model is efficient for circuit simulation and is further practical for analog circuit design. © 2000 Elsevier Science Ltd. All rights reserved.

1. Introduction

The continuing increase of the channel doping concentration when scaling deep submicron CMOS technology using dual polysilicon gates accentuates the impact of the polysilicon depletion effect [1,2] on all device characteristics. Modeling the effects of polysilicon depletion (or simply polydepletion) on drain current, transconductances, charges and transcapacitances in a unified and coherent way is a challenge. The correct asymptotic behavior of transcapacitances is difficult to achieve particularly when polydepletion is considered. The surface potential based approaches require numerical iteration to find the surface potential [2]. This may require special attention so as not to worsen the computational burden of the numerical iteration [3]. [1] An analytical polysilicon depletion model [4,5] was intro-

duced in the PCIM model [6] and subsequently implemented in BSIM3v3 of University of California, Berkeley [7]. This model conserves the essence of the polydepletion effect in strong inversion but uses an empirical extension to model charges in moderate and weak inversion. Other analytical circuit simulation models may not include polydepletion, such as MM9 of Philips [8]. In contrast to other analytical approaches, the models based on the EKV model [9] formalism, namely the models of [10,13] and the EPFL-EKV v2.6 model [11,12], use unified charges expressions, valid in all inversion regions and from non-saturation to saturation [14]. However, they do not include polydepletion either. In the present approach, a new charge based analytical model is formulated that includes polydepletion. The model uses the basic model variables of the initial EKV model [9] and can be viewed as a generalization of the charge based models [10–13]. Basic assumptions such as a uniform doping concentration both in the gate and the substrate, and depletion approximation in the gate are used similarly to [4,5]. Since the model formulation is tightly linked with the underlying analytical framework, the model derivation is specific to this family

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[*] Corresponding author. Tel.: +41-21-693-3975; fax: +41-21-693-3640.

E-mail address: jean-michel.sallese@epfl.ch (J.-M. Sallese).

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of models and is not intended to be used in a conventional source-referred MOSFET models.

The derivation of the new analytical model considering polysilicon depletion is provided in Section 2. The essential features of the new model is discussed in comparison with the previous model formulations [10–13]. The new analytical model is compared in Section 3 with the exact charges expressions where the surface potential is obtained by numerical iteration, considering different ratios of doping concentration for the substrate and the polysilicon. In Section 4, the formulation of the integral node charges, transcapacitances, and drain current are discussed. Comparison with the characteristics obtained from a two-dimensional numerical device simulator is made, for transcapacitances and drain current under various bias conditions.

2. Model formulation

The analytical model described here will use the same basic variables according to the modeling approach in Ref. [9], namely the pinch-off voltage V_P, the slope factor n, the current normalizing factor I_S called specific current, and the normalized forward and reverse currents i_f and i_r, as well as a substrate reference for all voltages. New expressions for the pinch-off voltage and the slope factor, considering now the effect of polydepletion, will be derived. The linearization of inversion charge versus surface potential considered in Ref. [10] has been the basis for the charge-based models either using charges [10] or the normalized currents [11–13] as principal variables. Here, a modified linearization scheme will be introduced and will later be shown to be essential to the accuracy of the new model especially for the transcapacitances.

The potential balance equation [14] in the MOS structure, including here the surface potential in the polysilicon gate, can be written as

$$V_G = \phi_{MS} + \Psi_{ox} + \Psi_s + \Psi_p, \tag{1}$$

where ϕ_{MS}, Ψ_{ox}, Ψ_s and Ψ_p are the workfunction difference between the polysilicon gate and the semiconductor, the potential across the gate oxide, the surface potential and the polysilicon gate surface potential, respectively. The charge neutrality is written as

$$Q'_G + Q'_0 + Q'_I + Q'_B = 0, \tag{2}$$

where Q'_G, Q'_0, Q'_I and Q'_B are the gate charge, fixed charge in the oxide, channel inversion and depletion charges, respectively, which are all expressed per unit area.

The gate charge and the potential across the oxide are related by

$$Q'_G = C'_{ox} \Psi_{ox}, \tag{3}$$

where C'_{ox} is the gate capacitance per unit area.

For simplicity, the doping profile in the polysilicon gate, as well as in the substrate, will be considered as uniform. The polysilicon is assumed to be well described by considering it as if it were crystalline silicon with the same doping concentration. Further, it is assumed that the region in the gate near the oxide interface will be entirely depleted. The depletion approximations for both the substrate and the gate lead, for an n-channel device, to the expressions for bulk and gate charges,

$$Q'_B = -C'_{ox}\gamma_s\sqrt{\Psi_s}, \tag{4}$$

$$Q'_G = C'_{ox}\gamma_p\sqrt{\Psi_p}, \tag{5}$$

where $\gamma_s = \sqrt{2q\varepsilon_s N_s}/C'_{ox}$ and $\gamma_p = \sqrt{2q\varepsilon_p N_p}/C'_{ox}$ are the substrate and polysilicon body effect coefficients, depending on the doping concentrations N_s, N_p and the dielectric constants $\varepsilon_s, \varepsilon_p$ for the substrate and polysilicon, respectively.

Using the standard definition of the flat-band voltage,

$$V_{FB} = \phi_{MS} - \frac{Q'_0}{C'_{ox}} \tag{6}$$

and combining Eqs. (1)–(5), a relationship between gate voltage, inversion and depletion charges and the channel surface potential is obtained in the form,

$$V_G = V_{FB} + \Psi_s - \frac{Q'_I + Q'_B}{C'_{ox}} + \frac{1}{\gamma_p^2}\left[\frac{Q'_I + Q'_B + Q'_0}{C'_{ox}}\right]^2. \tag{7}$$

At this point, it is suggested that the oxide fixed charges be neglected in the last term of Eq. (7). Under this assumption, Eq. (7) can be inverted so that the inversion charge can be written in terms of the other variables, as

$$Q'_I = C'_{ox}\left[\gamma_s\sqrt{\Psi_s} + \frac{\gamma_p^2}{2}\left(1 - \sqrt{1 + 4\frac{V_G - V_{FB} - \Psi_s}{\gamma_p^2}}\right)\right]. \tag{8}$$

The above assumption can be justified since the fixed charges are negligible with respect to inversion and depletion charges in strong inversion, where polysilicon depletion has the most notable impact. Conversely, in weak inversion, polydepletion has little effect on the charges.

In the following, definitions of pinch-off voltage and threshold voltage are given including them for polydepletion; however, note that the derivation made here is more straightforward than in Ref. [9] even without polydepletion.

Assuming that the MOS transistor is strongly inverted, the surface potential in the substrate can be approximated by a nearly constant value, which is fairly well described by Refs. [14,9],

$$\Psi_s \cong \phi_0 + V_{ch} \tag{9}$$

where $\phi_0 \cong 2\phi_F +$ several U_T and where V_{ch} is the channel Fermi potential Ref. [14].

Defining the threshold voltage V_{TO} as the gate voltage corresponding to a vanishing inversion charge density Q_I' under the above strong inversion assumption, and the condition $V_{ch} = 0$, i.e. with the channel in equilibrium Ref. [9], the threshold voltage is obtained from Eqs. (8) and (9) as

$$V_{TO} = V_{FB} + \gamma_s \sqrt{\phi_0} + \phi_0 \left[1 + \frac{\gamma_s^2}{\gamma_p^2} \right] \tag{10}$$

differing from its usual definition [9] but by the non-unity value of the term in parentheses that can similarly be found from Ref. [5].

Defining the pinch-off voltage V_P as the channel voltage such that the inversion charge density vanishes under the same strong inversion assumption similarly as in Ref. [9], the new pinch-off voltage expression accounting now for polydepletion is obtained as,

$$V_P = \left[\frac{1}{2} \left(\frac{\gamma_p}{\gamma_p^2 + \gamma_s^2} \right) \left[\gamma_s \gamma_p \right. \right.$$
$$\left. \left. - \sqrt{4(V_G - V_{FB})(\gamma_p^2 + \gamma_s^2) + (\gamma_p^2 \gamma_s^2)} \right] \right]^2 - \phi_0. \tag{11}$$

Note that without polydepletion, that is if $\gamma_p^2/\gamma_s^2 \gg 1$ or equivalently $N_p/N_s \gg 1$, the above definitions of V_P and V_{TO} revert to their basic counterparts defined in Ref. [9].

The inversion charge density Q_I' can be well approximated by a linearization in terms of either channel potential V_{ch} Ref. [9] or surface potential Ψ_s Ref. [10], in strong inversion, where (9) holds. The linearization is performed at $Q_I' \cong 0$, where $V_{ch} = V_P$ or $\Psi_s = \phi_0 + V_P$ hold under the above strong inversion assumption. Evaluating the slope of the Q_I' versus Ψ_s characteristic at this point allows us to define the slope factor, in the absence of polydepletion, as Ref. [10]

$$n = \frac{\partial}{\partial \Psi_s} \left(\frac{Q_I'}{C_{ox}'} \right) \Bigg|_{Q_I' \cong 0, \Psi_s = \phi_0 + V_P}$$
$$= 1 + \frac{\gamma_s}{2\sqrt{\phi_0 + V_P}}, \tag{12}$$

which coincides with the expression obtained in Ref. [9]. This approximation gives rise to the simple but accurate analytical charges model expressions used in Refs. [10–13] across the whole inversion region. In the present work, the inversion charge will still be linearized at the same point (i.e. $\Psi_s = \phi_0 + V_P$). However, the proposition is made here that the slope itself should be evaluated at a point $\Psi_s \cong \phi_0 + kV_P$, where k can take positive values

inferior (or equal to) one. The slope of inversion charge density is therefore evaluated at a higher level of inversion, allowing for a better estimation of inversion charge particularly when polydepletion is present, and leading to a new expression for the slope factor. The value for k can be chosen more or less arbitrarily; lower values of k shift the point where the slope is evaluated more towards strong inversion. In particular, the value $k = 0.5$ will be considered here, which represents a good compromise between simplicity and accuracy for the resulting transcapacitances.

Fig. 1 illustrates the dependence of the inversion charge density on surface potential for a given gate voltage, with and without polydepletion. The inset shows the derivative of the inversion charges versus the surface potential for both cases. When polydepletion is negligible (i.e. $\gamma_p^2/\gamma_s^2 \gg 1$), an almost linear relationship is observed, corresponding to an almost constant derivative over a large range of surface potential. The linearizations according to Ref. [10] and the proposed scheme both coincide with the theoretical characteristic in the absence of polydepletion. In the presence of polydepletion however the dependence of inversion charge density versus surface potential is less linear, as can be seen in Fig. 1. Note that the slope is significantly reduced and shows a rather important variation (see inset in Fig. 1); polydepletion in this example has been chosen to be rather strong on purpose. Linearizing the inversion charge as before leads to an important error in the estimation of charges. Conversely, the new linearization as presented here, greatly improves the accuracy
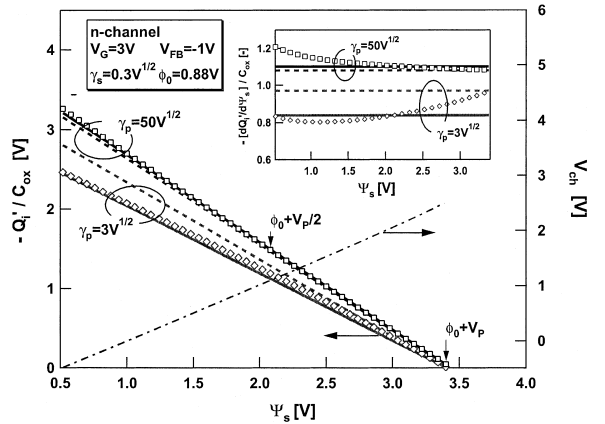

Fig. 1. Inversion charge density versus surface potential for a given gate voltage, without and with polydepletion. Surface potential based numerical model (markers) and linear approximations used in the analytical model, where the slope is evaluated at $\Psi_s = \phi_0 + 0.5V_P$ (lines) and at $\Psi_s = \phi_0 + V_P$ (dotted). The channel potential V_{ch} (dashed-dotted) remains almost unaffected by polydepletion. Inset: corresponding partial derivatives of inversion charge (markers), and the constant slopes of the linearizations (lines).

of the charges estimation. This improvement will be particularly clear on the calculated gate capacitance discussed in the following section. Further, Fig. 1 also shows the dependence of the channel potential V_{ch} with Ψ_s, for both values of polysilicon doping concentration. As is evidenced in the figure, V_{ch} is practically unaffected by polydepletion.

According to the new linearization scheme, the new definition of the slope factor will read,

$$n_Q = \frac{\partial}{\partial \Psi_s}\left(\frac{Q'_1}{C'_{ox}}\right)\Bigg|_{Q'_1 \cong 0, \Psi_s = \phi_0 + \frac{V_P}{2}}$$
$$= \frac{\gamma_s}{2\sqrt{\phi_0 + \frac{V_P}{2}}} + \frac{\gamma_p^2}{\sqrt{[\gamma_p^2 + 2\gamma_s\sqrt{\phi_0 + V_P}]^2 + 2\gamma_p^2 V_P}} \quad (13)$$

and has been given the subscript Q to underline that it is obtained from the linearization of inversion charge. Note that the expression for n_Q only depends on the gate voltage through V_P, and further depends only on the parameters γ_s, γ_p and ϕ_0.

The alternative definition of the slope factor, obtained as the derivative of the gate voltage with respect to the pinch-off voltage [9], will be modified as

$$n_v = \frac{dV_G}{dV_P} = 1 + \frac{\gamma_s}{2\sqrt{\phi_0 + V_P}} + \frac{\gamma_s^2}{\gamma_p^2} \quad (14)$$

and has been given the subscript v, differing from its original in Ref. [9] but by the last term. Similarly as before [9], the pinch-off voltage itself can be conveniently approximated in terms of the slope factor n_v as

$$V_P \cong \frac{V_G - V_{TO}}{n_v}. \quad (15)$$

The term n_v is therefore useful for hand-calculation estimates but is not directly used in the equations for the circuit simulation model. Since both V_{TO} and n_v increase with increased polydepletion effect, V_P can be seen to decrease. The slope factors n_Q and n_v differ significantly; their roles are not the same anymore. They would coincide in the absence of polydepletion, if the slope factor n_Q were evaluated at $\Psi_s \cong \phi_0 + V_P$ in Eq. (13). A further analysis in Appendix A illustrates the role of n_v relating the gate and source transconductances.

In Fig. 2, the two slope factors are compared for two cases, with and without polydepletion. n_v is greater or equal to one per definition and has an increased value in the presence of polydepletion. Conversely, n_Q can be seen to decrease significantly when polydepletion is present, and to attain values even lower than one. The pinch-off voltage itself, shown in the inset, can be seen to be slightly affected by polydepletion.

The roles of either of the slope factors need to be clearly distinguished. n_Q will in particular be used in the normalizing factors for the inversion charge and drain
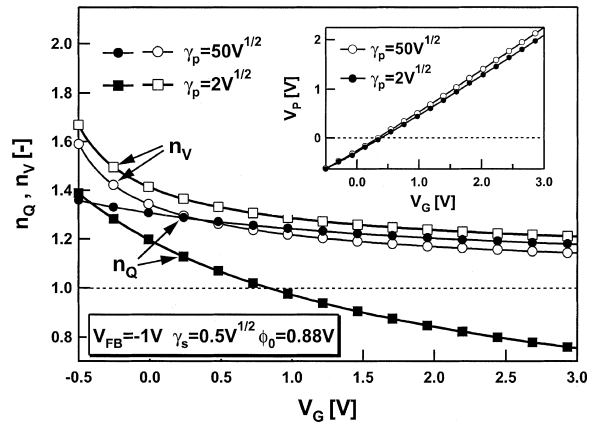

Fig. 2. Effect of polysilicon depletion on slope factors n_Q and n_v versus gate voltage, with and without polydepletion. Inset: corresponding pinch-off voltages.

current, as will be discussed later. Since n_Q is reduced when polydepletion is more severe, charges and current are reduced. Therefore, the transcapacitances and transconductances are also similarly reduced in the presence of polydepletion. On the other hand, the increased value of n_v when polydepletion is present has a comparable effect to that of a higher substrate doping concentration in the absence of polydepletion.

3. Comparison to surface potential based model

In this Section, the new analytical model will be compared to the surface potential based numerical model. Note that both the model formulations are valid only locally at a given point in the channel of the MOS transistor, or in the whole channel only when $V_{ch} = V_D = V_S$. The expressions of the local charge densities for the new analytical model are given in Appendix A. Transcapacitances are defined as partial derivatives of the charge densities with respect to the gate, channel and substrate potentials.

Fig. 3 shows the total gate capacitance from depletion to strong inversion, as obtained from the new analytical model, compared with the surface potential based model. The level of polysilicon doping concentration is varied over a large range; the first case with highest N_p shows almost no polydepletion effect, while the case with lowest N_p corresponds to an extreme case of polydepletion. The analytical model uses exactly the same physical parameters as the numerical model. The new analytical model shows an excellent match for all cases of polysilicon doping concentration, throughout the whole range of gate voltage. The onset of strong inversion is shifted with decreasing doping concentrations in the gate, corresponding to a change in the
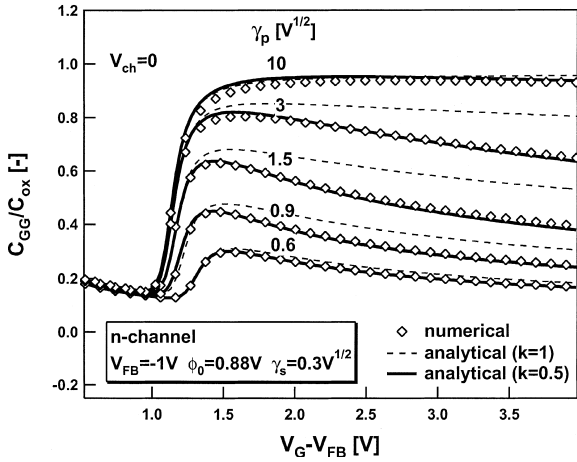
Fig. 3. Normalized gate capacitance versus gate voltage, for different polysilicon doping concentrations. The new analytical model (lines) is compared to the numerical model (markers). The conventional inversion charge linearization (dotted) results in serious errors. The analytical model uses the same physical parameters as the numerical reference model. For a value of $t_{ox} = 5$ nm, the values of γ_s and γ_p correspond to $N_s \cong 1.3 \times 10^{17}$ cm^{-3}, and $N_p \cong 2.1 \times 10^{21}$, 1.3×10^{19}, 3.2×10^{18}, 1.1×10^{18}, 5.1×10^{17} cm^{-3}, respectively.

threshold voltage which is accurately predicted. The gate capacitance attenuation is accurately matched for the whole regime of inversion. The quality of the match is underlined by the fact that no fitting parameter is used, which confirms the excellent physical basis of this model. In comparison, the results of the analytical model using the conventional linearization is shown to result in a much degraded match of gate capacitance attenuation.

4. Comparison to 2D device simulation

In this section, the new model will be compared to the characteristics obtained from a 2D numerical device simulator, for transcapacitances as well as drain current. For the latter, mobility reduction will also be considered.

The obtention of the analytical charges model in an integral form is outlined in the following so as to make the model valid also at non-equilibrium conditions (i.e. $V_D \neq V_S$). The local charge densities are integrated along the channel. The integration of the inversion charge, in terms of the normalized current, is straightforward. Ward's linear scheme is used to part the inversion charge into drain and source sides. The depletion charge as described by (A.4) is not integrable in its local form; therefore, a Taylor series expansion of (A.4) in terms of the inversion charge is required. While in the absence of polydepletion a first-order development is sufficient [9],

this is not the case anymore when polydepletion is present. The choice has been made here to use a third-order development, which is sufficient for practical cases of polydepletion. The integral node charges expressions will not be described in detail here. The full transcapacitances for the MOS transistor are then obtained by derivating the node charges versus terminal voltages [14,15] for all bias conditions from weak to strong inversion and from non-saturation to saturation.

The structure underlying the 2D numerical device simulation has been obtained from a 2D process simulation, where process characteristics correspond to a sub-quarter micron technology. All usual processing steps except channel implant are performed, resulting in a low channel doping but rather uniform doping profile with channel depth. The gate oxide thickness corresponds to $t_{ox} = 4.5$ nm, the substrate doping level is estimated as $N_s \cong 4 \times 10^{16}$ cm^{-3}, and the polysilicon doping level $N_p \cong 1 \times 10^{19}$ cm^{-3}, with approximately uniform profiles. In the present work, the modelling of non-uniform channel doping will not be discussed; an approach to non-uniform doping modelling can be found in Ref. [16]. Note that the low substrate doping level also alleviates the influence of quantum effects, which are beyond the scope of this article, and have therefore not been included in the numerical device simulation. Further, a channel length of $L = 10$ μm has been chosen to exclude short-channel effects such as velocity saturation and overlap and fringing capacitances. Model extensions for these effects will be considered elsewhere [17].

In Fig. 4(a)–(c), the normalized transcapacitances versus gate voltage are shown at various drain-to-source voltages, namely $V_D = 0$, 0.5, 1 V and $V_S = 0$ V. The new analytical model is compared with the numerical device simulation, and shows an excellent match for all bias conditions for all transcapacitances, C_{GG}, C_{DG}, C_{SG}, and C_{BG}. A single set of parameters is used in the analytical model for all bias conditions. The flat-band voltage has been adapted to match the measurement, and all other parameters match those underlying the 2D device simulation to within a few percent, i.e. to about the accuracy of the estimate of the doping concentrations in the gate and the substrate. The agreement at $V_D = V_S = 0$ V is excellent, $C_{DG} = C_{SG}$ is correctly predicted, and the value of $C_{DG} = C_{SG} = C_{GG}/2$ is correctly reached in strong inversion. At non-equilibrium conditions, the agreement is slightly degraded in the transition regions from saturation to non-saturation. Nonetheless, the overall qualitative behavior for an analytical model using only physical parameters remains excellent. Similar results have also been found with different levels of substrate and gate doping concentrations. Correct asymptotic behavior is found for all transcapacitances, including the ones not shown here, and is found to be further improved with respect to the previous
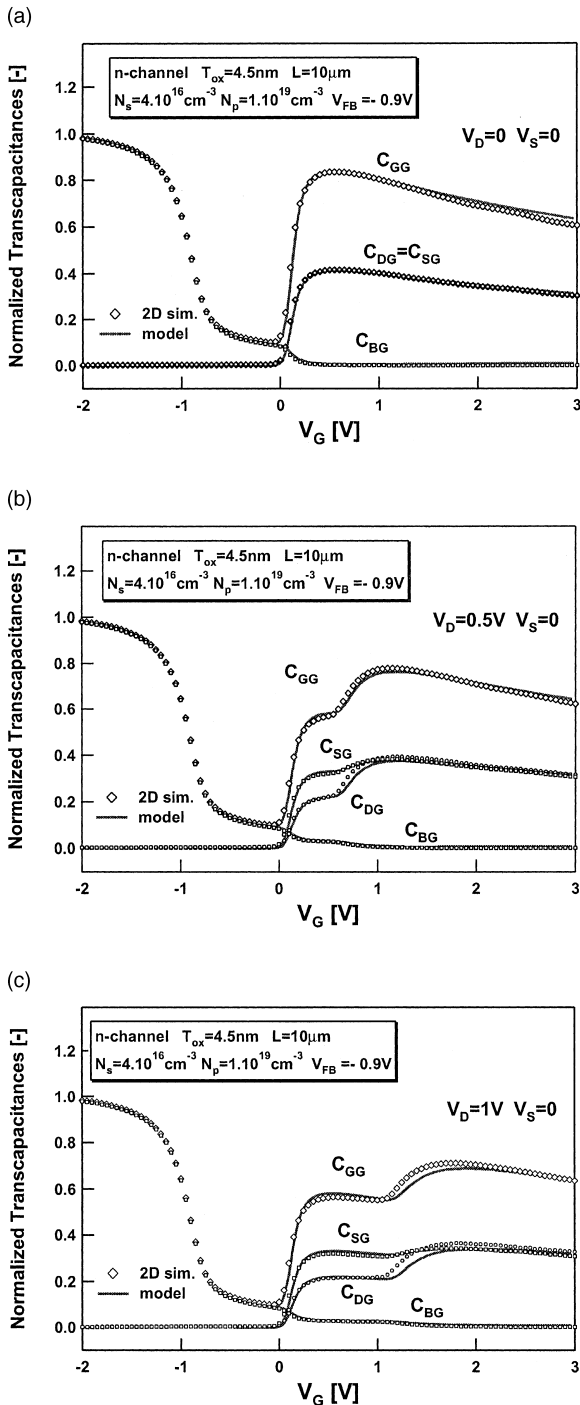
(a)

(b)

(c)

Fig. 4. Normalized transcapacitances versus gate voltage for an n-channel device showing polysilicon depletion: (a) $V_D = 0$ V, (b) $V_D = 0.5$ V, (c) $V_D = 1$ V, at $V_S = 0$ V. The new analytical model (lines) is compared to 2D numerical devices simulation (markers). The values of N_s and N_p correspond to $\gamma_s \cong 0.15\sqrt{V}$, and $\gamma_p \cong 2.38\sqrt{V}$, respectively.

linearization. Note that e.g. the correct behavior of $C_{BG} \rightarrow 0$ in strong inversion non-saturation, is due to the higher-order development of the bulk charge used, while its first-order counterpart would indeed lead to an incorrect asymptotic behavior of C_{BG}.

The new drain current expression (18) is given in Appendix A. The effect that polydepletion has on the drain current will shortly be discussed here. The pre-factor of the drain current, called specific current I_S [9], is written in terms of the slope factor n_Q,

$$I_S = 2n_Q\mu_{eff}C'_{ox}U_T^2\frac{W}{L}. \tag{16}$$

The effective mobility μ_{eff} can be written, considering the effect of the mobility reduction due to vertical field to first order [6,11] as

$$\mu_{eff} \cong \frac{\mu_0}{1 + \Theta E_{eff}} \tag{17}$$

where μ_0 is the low-field mobility, and Θ (in m/V), the mobility reduction parameter. The effective vertical field is expressed as $E_{eff} = |Q'_B + \eta Q'_I|/\varepsilon_{si}$, where η is a weighting factor Refs. [6,18]. Note that the charges expressions for the effective field, affecting the mobility reduction, are themselves affected by polydepletion.

In summary, the drain current is affected in three ways by polydepletion: first, through the new expression of the pinch-off voltage, essentially equivalent to a change in threshold voltage and body effect, affecting the normalized forward and reverse currents; second, through the modified slope factor n_Q in the specific current, and finally through the mobility model using effective field. Among the three effects, the one on the slope factor n_Q is found to be the most important. Note that in the other analytical models, no equivalent effect to that of n_Q has been described.

The effect of polydepletion on drain current versus gate voltage characteristics is shown in Fig. 5, for two values of drain voltage, $V_D = 0.5$ V and $V_D = 1$ V corresponding to the same cases as in Fig. 4(b) and (c). Two cases of polysilicon doping concentrations are shown, $N_p = 1 \times 10^{19}$ cm^{-3} corresponding to the same devices as used in Fig. 4, and $N_p = 9.1 \times 10^{20}$ cm^{-3} showing no polydepletion as a result. The same parameter set is used for the analytical model in both cases, except for the change in polysilicon doping concentration and a slight change in the flat-band voltage, due to a changed workfunction difference between the polygate and the substrate. The mobility model parameters have been chosen to match the case with polydepletion. As can be seen, the case without polydepletion is reasonably well matched without adapting model parameters further, confirming the coherence of the model. The slight difference observed may also stem from different processing circumstances for each cases.
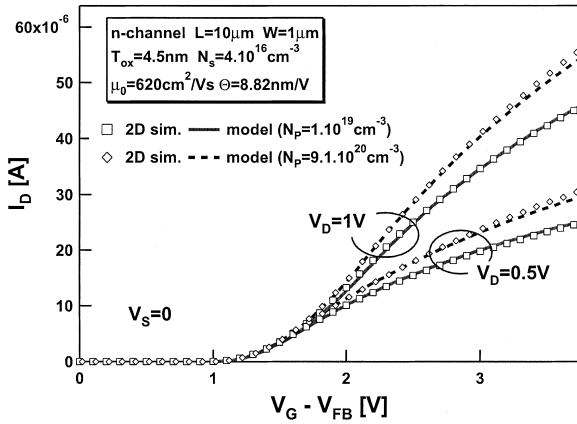
Fig. 5. Drain current versus gate voltage, for two drain voltages, $V_D = 0.5$ V, 1 V, $V_S = 0$ V, for two cases of polysilicon doping concentrations. 2D simulation (markers) and analytical model (lines). The model uses one set of parameters in all conditions except for changed gate doping concentration.

Further, mobility effects and short-channel effects will be introduced for a more complete model [11,12,17], that will again affect both charges and drain current in a coherent way, maintaining the essential feature of the present model.

5. Conclusions

A new analytical approach to modelling polysilicon gate depletion for MOS transistor circuit simulation has been presented. The analytical model uses only physical parameters and shows excellent behavior compared to a surface potential based numerical approach and to 2D numerical device simulation. A coherent charge and drain current model has been formulated based on the model formalism of the EKV model and related charges models, which is valid in all operating regions from weak to strong inversion and from non-saturation to saturation. The model shows improved qualitative and quantitative behavior with respect to formerly available model formulations, which either do not include polydepletion, or do not present unified charges expressions valid at all inversion levels, or both. The model is based on a new linearization scheme for inversion charge versus surface potential. The essential characteristics of the new model are contained in the modified expressions for the pinch-off voltage and the slope factor. The impact of polydepletion on these expressions, which are useful to analog circuit design, has been pointed out. Other expressions of the analytical charges model formulation remain essentially the same as in the preceding models underlying the present approach. The new model for the transcapacitances shows good qualitative and quantitative behavior, in particular for asymptotic cor-

rectness. Comparisons of CV and IV characteristics over a large range of physical device parameters and bias conditions, corresponding to present deep submicron CMOS technology, have shown excellent overall behavior considering that no empirical fitting parameters are used. The model uses a minimal number of physical device parameters. This model formulation is therefore a sound basis for a more complete model, including in particular short-channel effects, for deep submicron circuit design and simulation.

Appendix A

The drain current can be written as [9]

$$I_D = 2n_Q \mu_{eff} C'_{ox} U_T^2 \frac{W}{L} (i_f - i_r), \quad (A.1)$$

where the current prefactor, called specific current in Ref. [9], now uses the new definition of the slope factor n_Q according to Eq. (13). The normalized currents $i_{f(r)}$ [9] are evaluated according to Refs. [11,12],

$$i_{f(r)} = F\left[\frac{V_P - V_{S(D)}}{U_T}\right]. \quad (A.2)$$

Note that the origin of the function F is due to Ref. [10]. The pinch-off voltage V_P is now used according to its new definition (11).

The expressions of local charge densities for the new analytical model, in terms of the position x and the currents $i_{f(r)}$, are given by

$$Q'_I(x) = -2n_Q U_T C'_{ox}\left[\sqrt{\frac{1}{4} + i_f - \frac{x}{L}(i_f - i_r)} - \frac{1}{2}\right], \quad (A.3)$$

$$\frac{Q'_B(x)}{C'_{ox}} = \frac{\gamma_s^2 \gamma_p^2}{\gamma_s^2 + \gamma_p^2}\left[\frac{1}{2} - \frac{Q'_I(x)}{\gamma_p^2 C'_{ox}}\right.$$
$$\left. - \sqrt{\frac{1}{4} + \left(\frac{1}{\gamma_s^2} + \frac{1}{\gamma_p^2}\right)(V_G - V_{FB}) + \frac{Q'_I(x)}{\gamma_s^2 C'_{ox}}\left(1 - \frac{Q'_I(x)}{\gamma_p^2 C'_{ox}}\right)}\right], \quad (A.4)$$

$$Q'_G(x) = -[Q'_I(x) + Q'_B(x) + Q'_0]. \quad (A.5)$$

Note that n_Q is also used in the prefactor of the inversion charge density, replacing the formerly used expression of the slope factor [9–13].

The slope factor n_v can be shown to relate the gate and source transconductances. The gate transconductance g_{mg} [14,9] is defined as

$$g_{mg} \equiv \frac{\partial I_D}{\partial V_G}\bigg|_{V_S,V_D} = \frac{\partial}{\partial V_P}[I_S(i_f - i_r)]\frac{dV_P}{dV_G} \\ = \frac{\partial}{\partial V_P}[I_S(i_f - i_r)]\frac{1}{n_v}. \tag{A.6}$$

The source transconductance g_{ms} [9,14] is defined as,

$$g_{ms} \equiv -\frac{\partial I_D}{\partial V_S}\bigg|_{V_G,V_D} = -\frac{\partial}{\partial V_S}[I_S(i_f - i_r)]. \tag{A.7}$$

If the gate voltage dependence of n_Q in the specific current I_S is neglected (an approximation which is less valid in the presence of polydepletion), the relationship between the gate and source transconductances in saturation ($i_f \gg i_r$) is approximately given by

$$g_{ms} \cong n_v g_{mg}, \tag{A.8}$$

which corresponds to the relationship in Ref. [9] with n_v replacing n, showing that the source transconductance is n_v times higher than the gate transconductance in saturation.

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