

EKV MOS Transistor Modelling & RF Application

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- ⇒ Part I: Charge-based DC, AC and Noise Modelling
- ⇒ Part II: RF Application

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PART I: Charge-based DC, AC and Noise Modelling

- ⇒ ***Introduction: EKV v2.6***
- ⇒ ***Charge-based Static Model***
- ⇒ ***Quasi-static Charge & Transcapacitances Model***
- ⇒ ***NQS Model***
- ⇒ ***Noise Model***
- ⇒ ***Mobility Model & Short-Channel Effects***

Introduction: EKV v2.6 MOS Transistor (MOST) Model

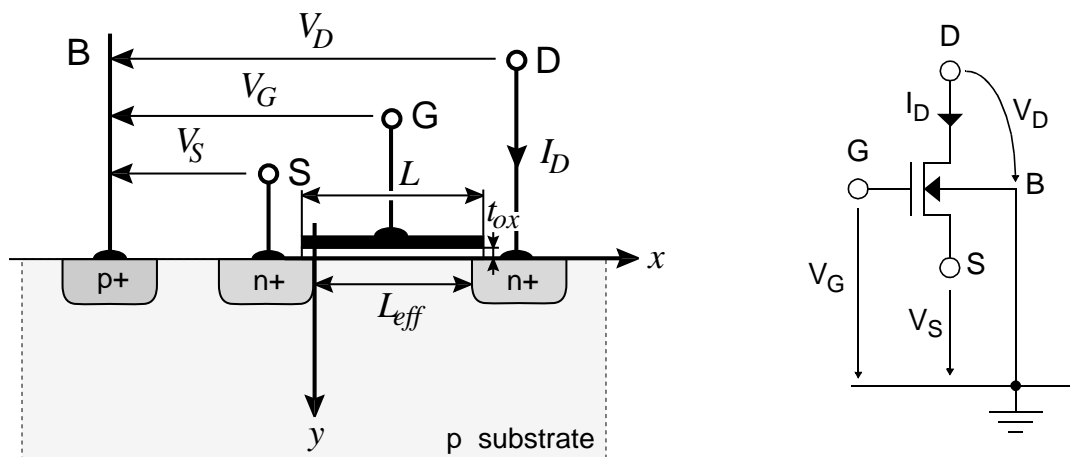
☞ Motivation:

- ✓ RF circuit design requires **complete MOST model from DC to RF**, including noise.
- ✓ All current levels need to be well modelled, in particular also **moderate inversion**.

☞ EKV v2.6 in summary:

- ✓ A **physics-based compact MOST model in the public domain**.
- ✓ Dedicated to **analog circuit simulation** for submicron CMOS.
- ✓ Includes **weak-moderate-strong inversion modelling**, doping & mobility effects, short-channel effects, geometry- and bias-dependent matching.
- ✓ Small number of intrinsic model parameters:
EKV v2.6: < 20, BSIM3v3: > 65, MM9: > 55

Charge-based Static Model

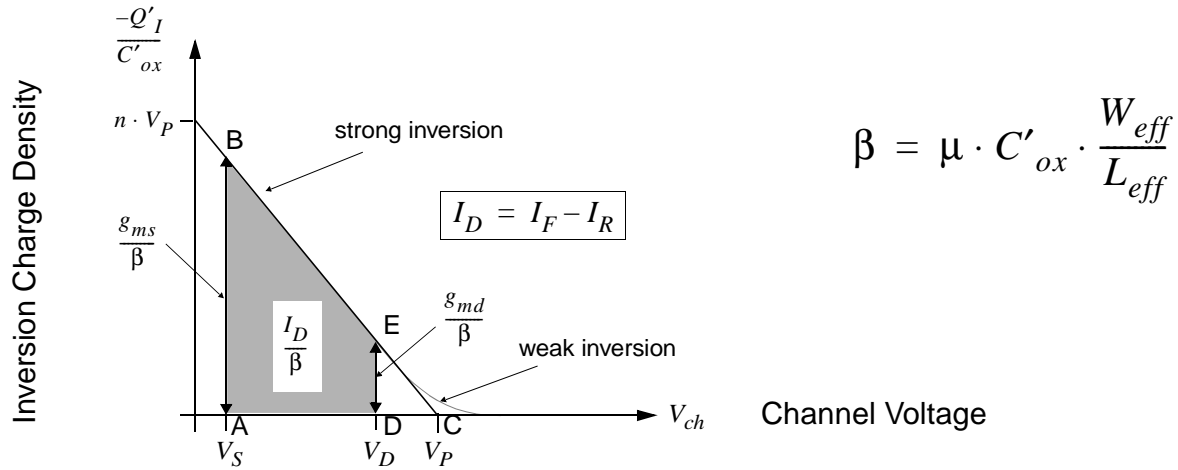


☞ Bulk-reference, symmetric model structure.

☞ Drain current expression including drift and diffusion:

$$I_D = W \cdot \mu \cdot (-Q'_l) \cdot \frac{dV_{ch}}{dx} \quad (1)$$

Charge-based Static Model



⇒ Integration of Q'_I from source to drain:

$$I_D = \beta \int_{V_S}^{V_D} \left(\frac{-Q'_I}{C'_{ox}} \right) \cdot dV_{ch} = \underbrace{\beta \int_{V_S}^{\infty} \left(\frac{-Q'_I}{C'_{ox}} \right) \cdot dV_{ch}}_{I_F(V_P - V_S)} - \underbrace{\beta \int_{\infty}^{V_D} \left(\frac{-Q'_I}{C'_{ox}} \right) \cdot dV_{ch}}_{I_R(V_P - V_D)} \quad (2)$$

Drain Current Normalization and Pinch-off Voltage

⇒ Current normalization using the **Specific current** I_S :

$$I_D = I_F - I_R = I_S \cdot (i_f - i_r) = 2n\beta U_T^2 \cdot (i_f - i_r) \quad (3)$$

⇒ **Pinch-off voltage** V_P accounts for...

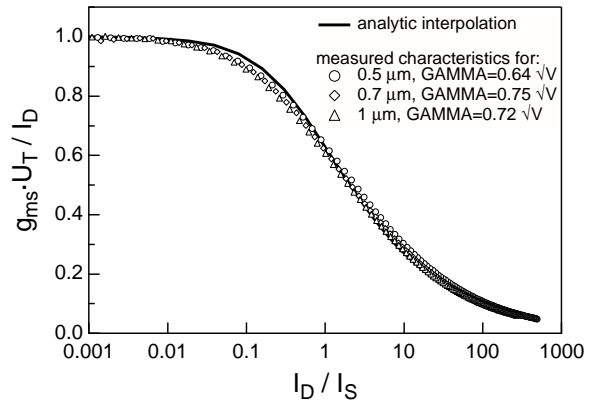
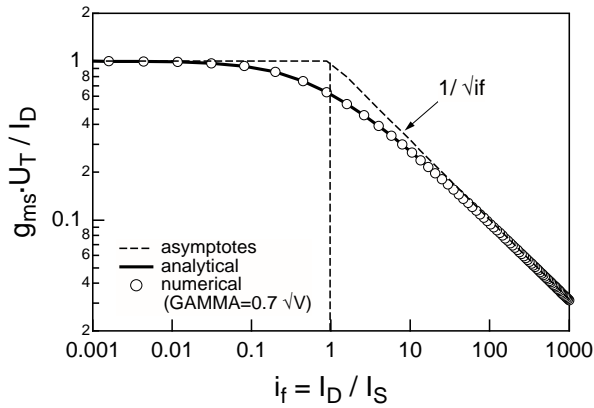
✓ **threshold voltage** V_{TO} and **substrate effect** $\gamma = (\sqrt{2q\epsilon_s N_{sub}}) / C'_{ox}$

$$V_P = V_G - V_{TO} - \gamma \cdot \left[\sqrt{V_G - V_{TO} + \left(\sqrt{\Psi_0} + \frac{\gamma}{2} \right)^2} - \left(\sqrt{\Psi_0} + \frac{\gamma}{2} \right) \right] \quad (4)$$

⇒ **Slope factor** n :

$$n = \left[\frac{\partial V_P}{\partial V_G} \right]^{-1} = 1 + \frac{\gamma}{2\sqrt{\Psi_0 + V_P}} \quad (5)$$

Charge-based Static Model



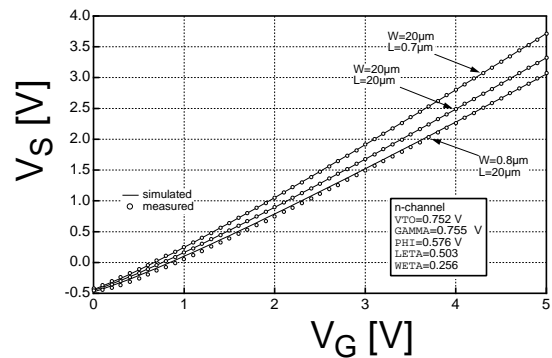
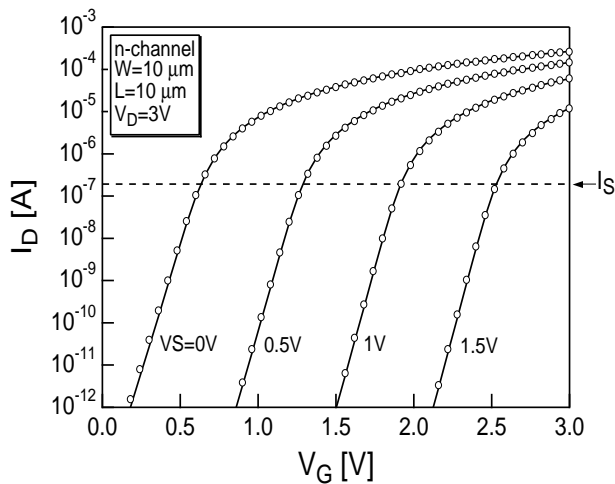
➤ Normalized transconductance-to-current ratio $g_{ms} \cdot U_T / I_D$ vs. normalized current I_D / I_S from weak through moderate to strong inversion.

✓ Comparison with numerical solution of the Poisson equation.

✓ Comparison with three different CMOS processes (long-channel devices in saturation).

✓ Almost technology independent!

Drain Current and Pinch-off Voltage

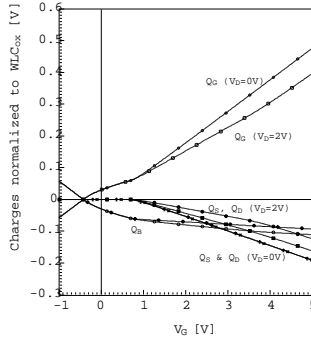


➤ Valid from weak to strong inversion, and from linear to saturation.

➤ Accuracy of weak inversion slope and substrate effect.

✓ no additional parameters used for adapting weak inversion slope

Quasistatic Charge- & Transcapacitances Model



$$C_{OX} = C'_{ox} \cdot W \cdot L$$

Node charges: integration of inversion charge density along channel:

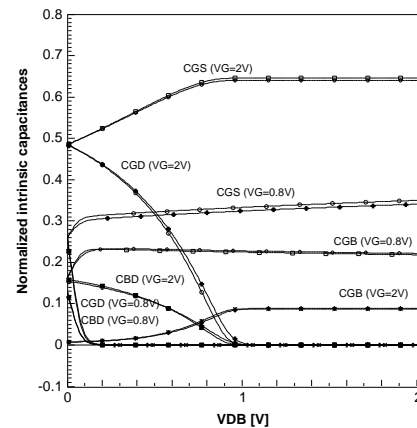
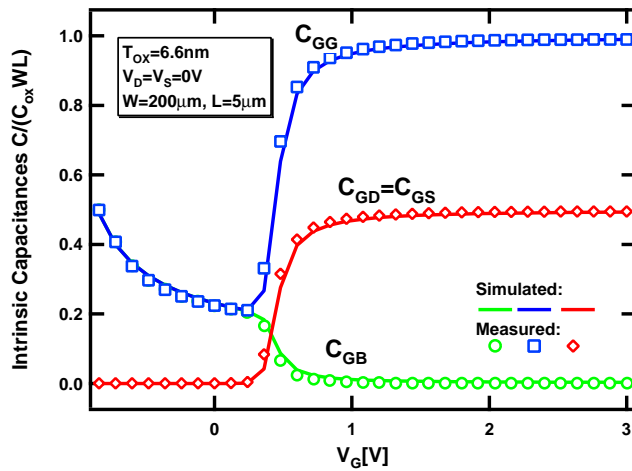
$$Q_I = W \cdot \int_0^L Q_I'(x) \cdot dx \quad Q_D = W \cdot \int_0^L Q_I'(x) \cdot dx \quad Q_S = Q_I - Q_D \quad (6)$$

$$Q_B = -\gamma \cdot C_{OX} \cdot \sqrt{V_P + \Psi_0} - \left(\frac{n-1}{n} \cdot Q_I\right) \quad Q_G = -Q_I - Q_B - Q_{ox} \quad (7)$$

✓ Drain and source charges are obtained using Ward's charge partitioning scheme.

✓ Single equation expressions are used from weak to strong inversion.

(Trans-)Capacitances Model



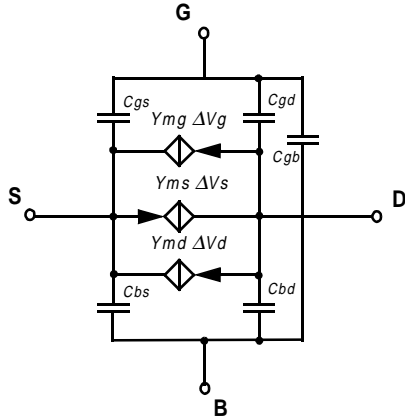
Transcapacitances: derivation with respect to the terminal voltage:

$$C_{MN} = \pm \frac{\partial}{\partial V_N} (Q_M) \quad M, N = G, D, S, B \quad (8)$$

✓ Accurate capacitances through all inversion levels.

✓ Symmetric C_{GS} and C_{GD} at $V_D=V_S=0$.

Intrinsic MOST - Small Signal Equivalent



Transcapacitances are not shown

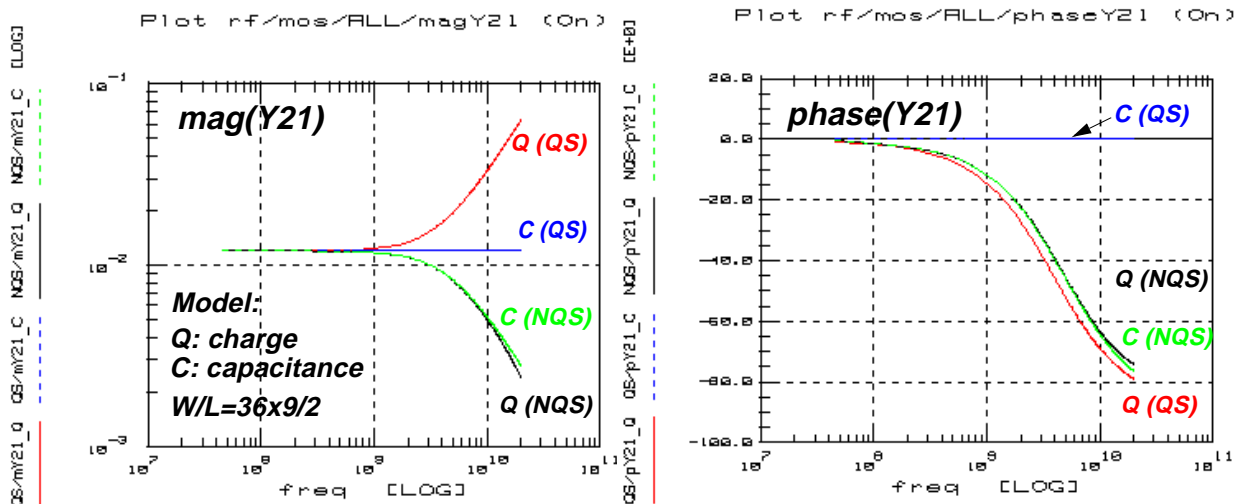
Distributed time constant accounting for "transmission line effect"

✓ First-order model for the transadmittances using bias-dependent time constant τ :

$$Y_{m(g, d, s)} \equiv \frac{\partial i_d}{\partial v_{(g, d, s)}} = \frac{g_{m(g, d, s)}}{1 + s \cdot \tau} \quad \text{with } \tau = \tau_0 \cdot f(i_f, i_r) \quad (9)$$

$$\tau_0 = \frac{L^2}{2 \cdot \mu \cdot U_T} \quad (10)$$

Non-Quasistatic Model

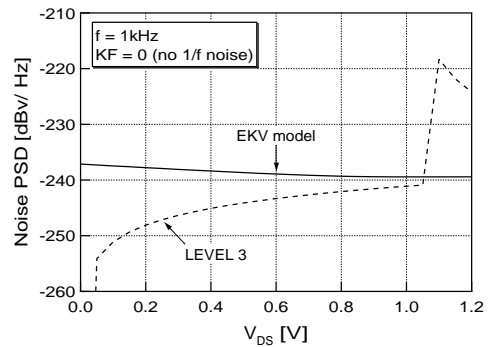
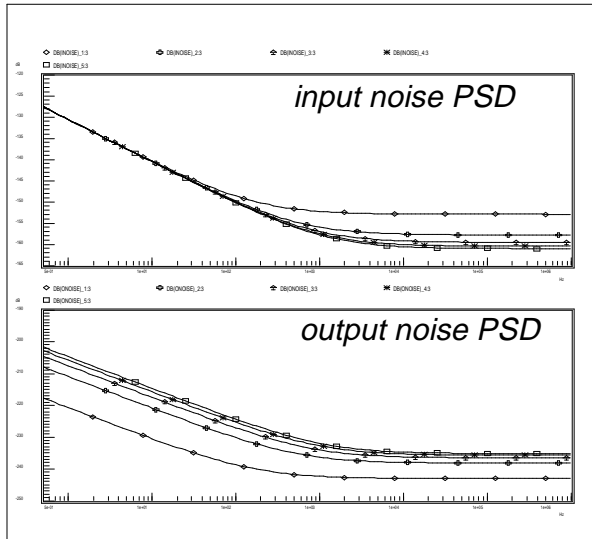


✎ Intrinsic MOST: effect of QS/NQS models on charges-transcapacitances- and capacitances-only models.

✓ Y21 Phase prediction is similar for all models except C-only QS model.

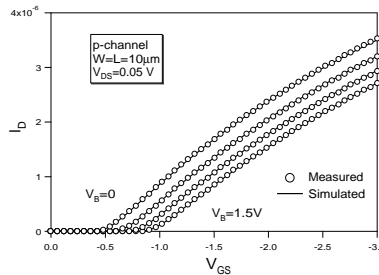
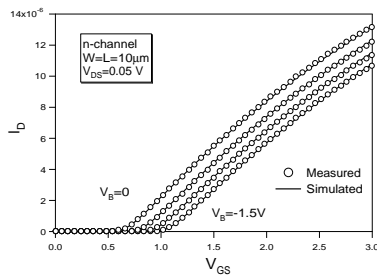
✓ Y21 Magnitude prediction is incorrect for Q (QS) and C (QS) models.

Noise Model



- ☞ Thermal noise is proportional to total inversion charge Q_I .
- ✓ Valid for all inversion levels, and from linear to saturation.
- ☞ 1/f noise modelling included.

Mobility Model



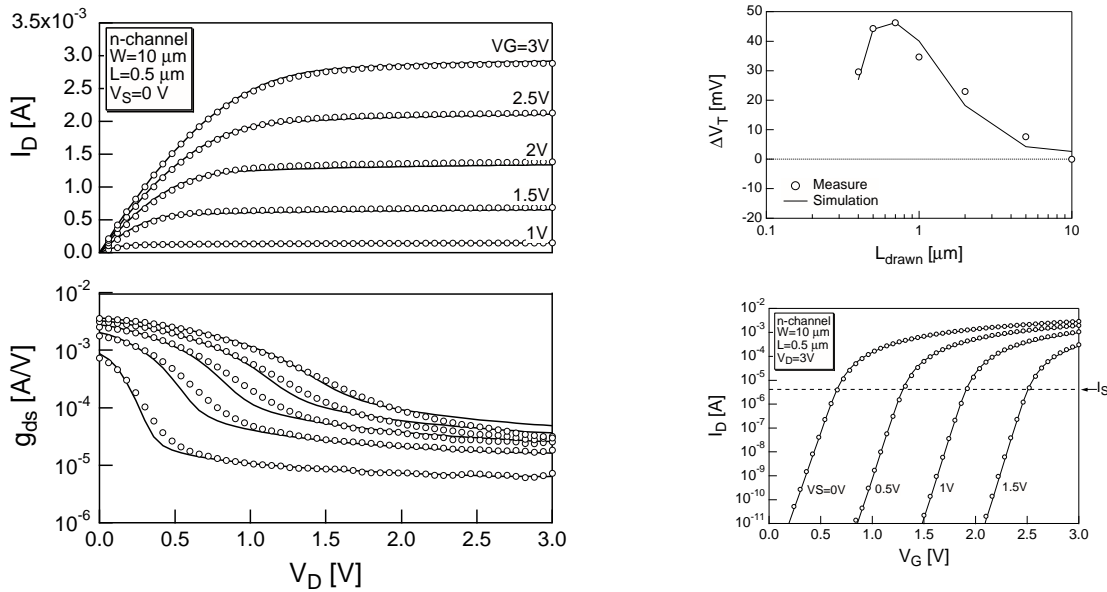
EKV v2.6 for 0.5um CMOS (NMOS, PMOS)

- ☞ Field- and position-dependent mobility:

$$\mu(x) = \frac{\mu_0'}{1 + \frac{E_{eff}(x)}{E_0}} \quad \text{where:} \quad E_{eff}(x) = \frac{Q'_B(x) + \eta \cdot Q'_{inv}(x)}{\epsilon_0 \epsilon_{si}} \quad (11)$$

- ☞ One parameter: E_0 vertical critical field in the oxide
- ✓ $\eta = 1/2$ for n-channel, $\eta = 1/3$ for p-channel)
- ✓ No back-bias dependence needed due to inclusion of bulk charge.

Short-channel Effects



- ☞ Includes short-channel effects (here: 0.5 μm CMOS)
 - ✓ Velocity saturation, Channel length modulation (CLM), 2D-charge sharing, RSCE

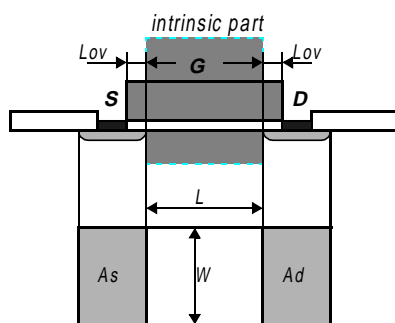
Summary

- ☞ EKV v2.6 MOST model is a charge-based compact model
 - ✓ Continuous, physics-based and valid for all bias conditions.
 - ✓ Includes charge-based static and dynamic models, and noise.
 - ✓ Non-quasistatic (NQS) model for small-signal.
- ☞ Availability early '99:
 - ✓ Eldo, SmartSpice, Saber, Spectre, HSpice, PSpice, APlac, Smash (check model versions).
- ☞ EKV v2.6 on the web: <http://legwww.epfl.ch/ekv/>

- **Intrinsic MOST and Extrinsic Parasitic Elements**
- **RF Test Structure**
- **Simulation and Measurement Environment**
- **DC Measurements and Simulations**
- **RF Measurements and Simulations**

Intrinsic MOST and Extrinsic Parasitic Elements

Structure of the MOST

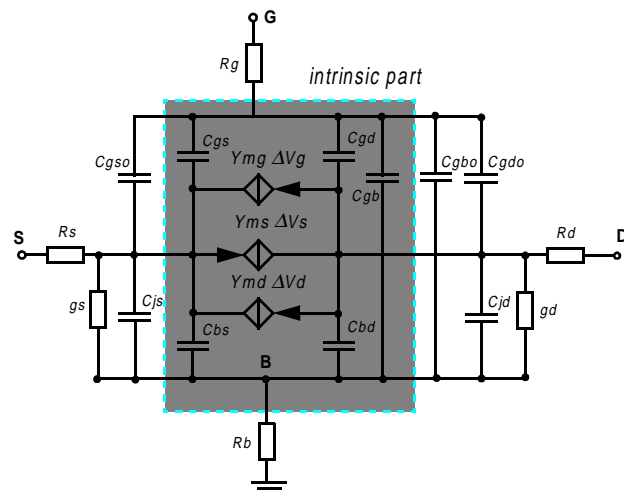


$$C_{js(d)} = A_{s(d)} * C_j + P_{s(d)} * C_{jsw}$$

$$C_{ov} = W * L_{ov} * C_{ox}$$

P_s, P_d - perimeter
 A_s, A_d - area

Corresponding small-signal EKV model



☞ Measurements:

- ✓HP8510 and HP 8719 Network Analyzers
- ✓HP4145 and HP4156 DC Parameter Analyzers
- ✓Cascade HF Probe Station
- ✓Ground-Signal-Ground (GSG) probes

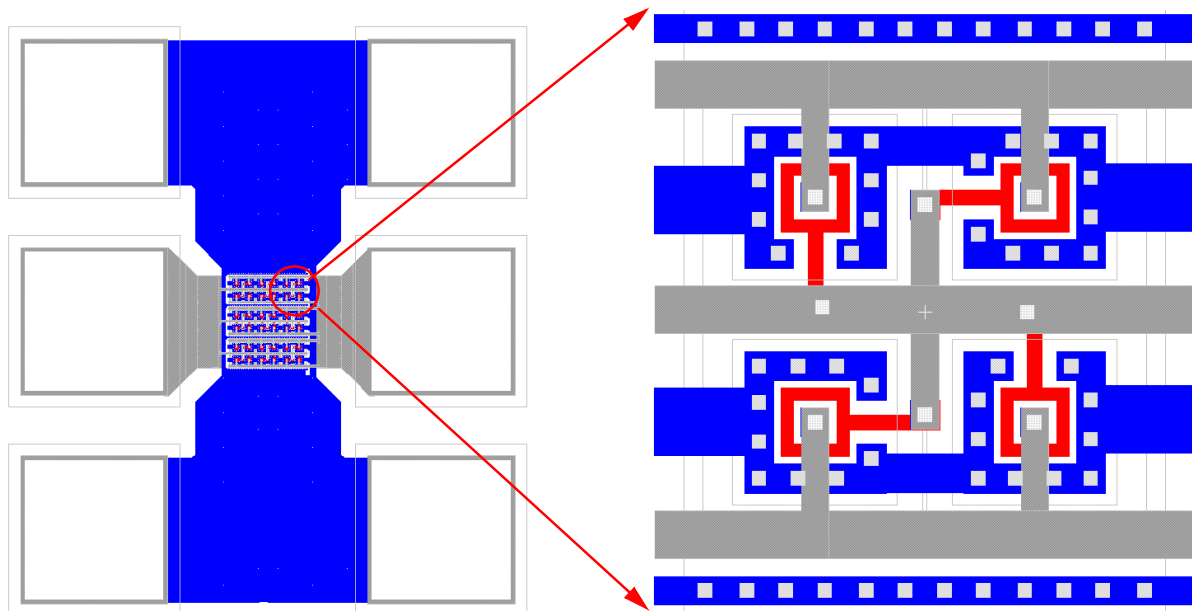
☞ Test Devices:

- ✓RF MOS transistor matrix with 36 parallel devices in GSG pad frame
- ✓Geometry of single circular MOST: $L = 0.5 \mu\text{m}$, $W = 9.2 \mu\text{m}$
- ✓OPEN pad frame for de-embedding thru Y parameters

☞ Parameter Extraction and Simulation:

- ✓IC-CAP 5
- ✓ELDO v4.6 with EKV v2.6 (LEVEL=44)

RF Test Structure

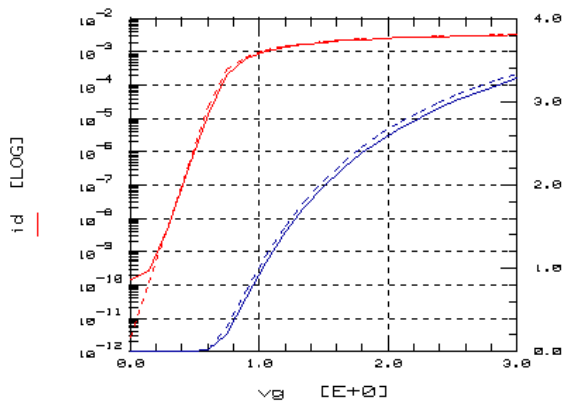


courtesy A.-S. Porret

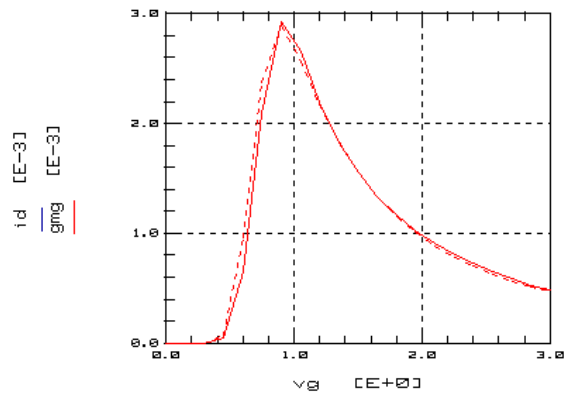
☞ The GSG pad frame and matrix of the RF MOSTs

- ✓Minimized extrinsic drain capacitance using circular layout

DC Measurements and Simulations



I_D vs. V_G

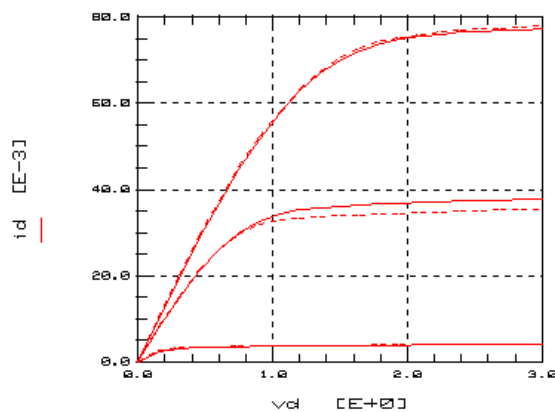


g_m vs. V_G

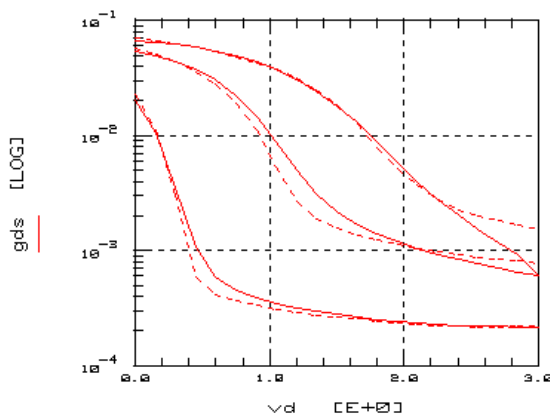
☞ Transfer current and conductance characteristics

✓ $V_D = 50\text{mV}$

DC Measurements and Simulations



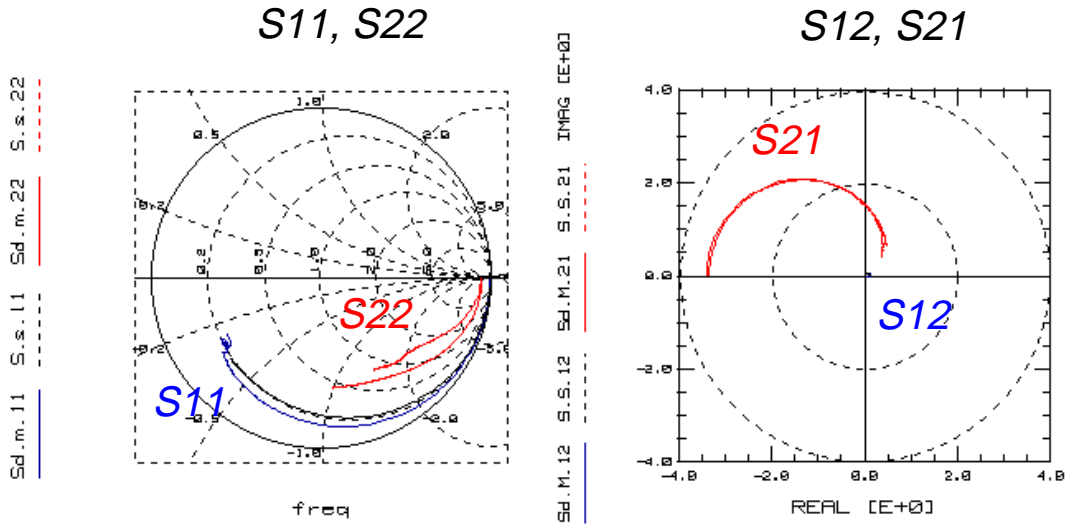
I_D vs. V_D



g_{ds} vs. V_D

☞ Output current and conductance characteristics

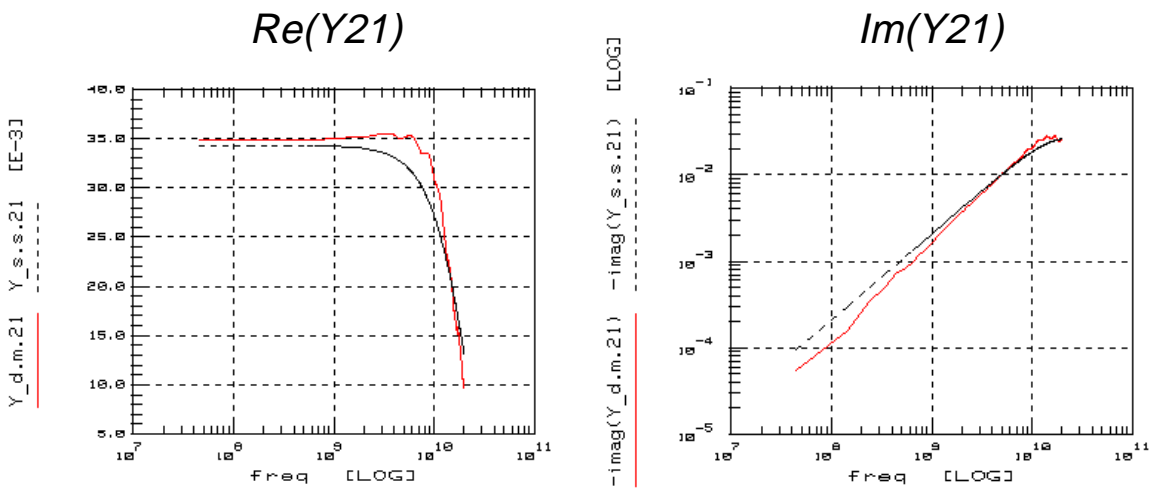
RF Measurements and Simulations



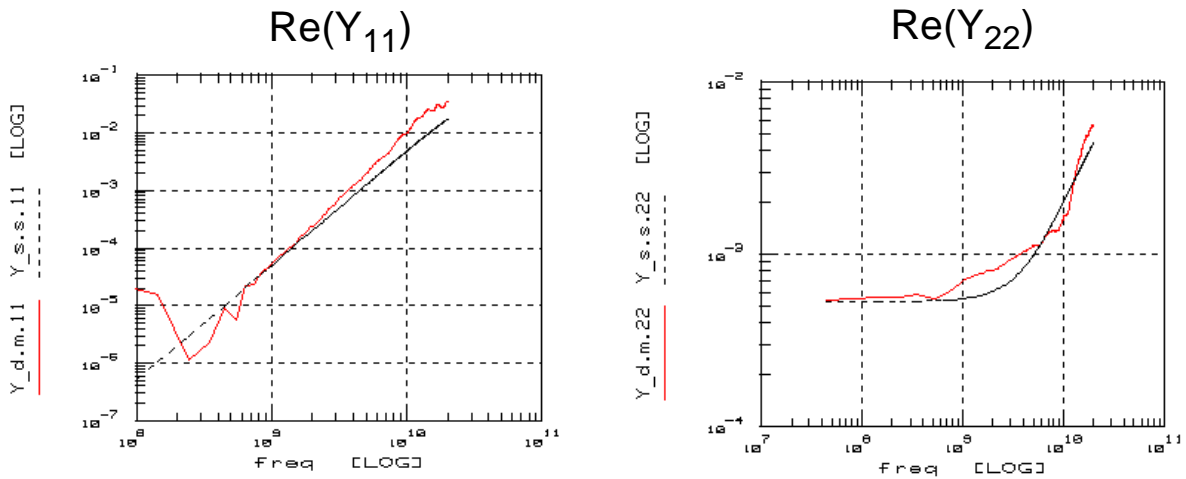
☞ Measured de-embedded and simulated S-parameters

- ✓ Frequency sweep 45MHz - 20 GHz
- ✓ DC bias $I_D=18\text{mA}$ @ $V_G = 1.5\text{V}$ $V_D = 3.0\text{V}$

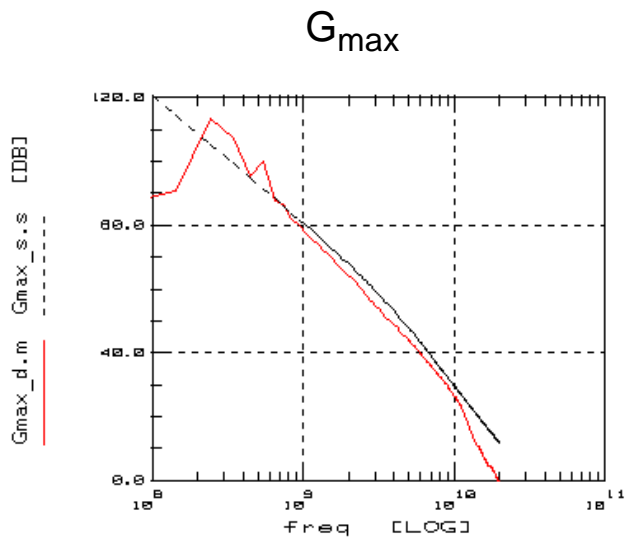
RF Measurements and Simulations



☞ Real and Imaginary parts of the forward admittance Y_{21}



☞ Real parts of the input and output admittances Y_{11} , Y_{22}



☞ Maximum power gain G_{max}

Summary

- ➔ Application of the physics-based EKV v2.6 MOST model for RF simulation has been presented
 - ✓DC parameter set was verified on the RF MOST test structure measurements
 - ✓The small-signal characteristics were corrected for interconnections and bond pads parasitics
 - ✓Effective gate and bulk (substrate) resistances were introduced to allow proper small signal simulation
 - ✓Simulated small-signal S- and Y- parameters match on-the-wafers measurements over wide range of frequencies (45MHz - 20GHz)