A Compact Non-Quasi-Static Extension of a Charge-Based MOS Model

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***Abstract*—This paper presents a new and simple compact model for the intrinsic metal oxide semiconductor (MOS) transistor, which accurately takes into account the non quasistatic (NQS) effects. This is done without any additional assumption or simplification than those required in the derivation of the classical description of the MOS channel charge. Moreover, the model is valid from weak to strong inversion and nonsaturation to saturation.**

The theoretical results are in very good agreement with measured data performed on devices of various channel length, from 300 μm down to 0.5 μm, and in various modes of operation.

***Index Terms*—Charge-sheet model, compact modeling, EKV model, MOS transistor modeling, non-quasi-static (NQS).**

I. Introduction

ALTHOUGH the small-signal non quasistatic (NQS) regime of the intrinsic metal oxide semiconductor (MOS) transistor has already been investigated in several papers [1]–[10], these descriptions are often mathematically cumbersome, so that they give little insight to the circuit designers. Moreover, the operating frequency of most high frequency circuits is forced in a range where NQS effects are almost negligible ($\ll f_T$) by the capacitive load of the active devices. However, when an inductive load tunes out the capacitance at some nodes, NQS effects might be the limiting factor. Also, the PMOS biasing current sources of RF circuits might easily suffer from these effects because of the lower mobility of holes. Finally, low frequency circuits sometimes require extremely long devices, like 100 μm, exhibiting an NQS cutoff frequency much lower than 1 MHz.

If the NQS regime must be checked for, a well known, but crude, first-order approximation can be used [11], [12]. However, there is no fundamental reason for banning devices operating in this mode, provided that they have not to be active at high frequency. The goal of this paper is therefore to provide a simple model to accurately predict the small signal behavior of a MOS transistor at any frequency.

A. DC Model

This work is based on a charge-based description of the MOS transistor as was first proposed by D. E. Ward in [13]. Such a description is for example used in the EKV compact model [14]. It has the advantage of being physically based and provide simple analytical formulations for long channel devices which are valid in all modes of operation.

In the context of charge-based models, the drain current I is written as the difference between a forward component $I_{\rm F}$, which is solely dependent on the local charge density at the source, and a reverse component $I_{\rm R}$, which depends only on the drain charge. Strictly speaking, this partitioning is only valid when the mobility can be assumed constant along the channel, i.e., at low electrical fields. However, mobility reduction due to the vertical field can be taken into account by decreasing the mobility globally. Also, velocity saturation can be dealt with by dividing the channel into two sections, one with a constant mobility and another where carriers travel at saturation velocity [15], [16].

The states of charge inversion at the source and drain are described by the variables χ_f and χ_r, respectively, which have no direct physical meaning and are unitless. χ_f and χ_r tend toward $1/2$ in weak inversion and increase proportionally with the local charge densities at the source (χ_f) or drain (χ_r) in strong inversion. The equations[1] linking these intermediate variables to the voltages applied at the transistor terminals are then, from [14], [17], or [18]

$$\frac{V_{\rm G}-V_{\rm T0}-nV_{\rm S(D)}}{nU_T}=2\chi_{f(r)}-1+\ln\left(\chi_{f(r)}-\frac{1}{2}\right) \quad (1)$$

where

- $V_{\rm S}, V_{\rm D}$, and $V_{\rm G}$ — the source, drain, and gate voltages referred to the bulk;
- $V_{\rm T0}$ — threshold voltage at $V_{\rm S}=0$;
- $U_T=k_BT/q_{\rm e}$ — thermodynamic voltage;
- n — transistor slope factor due to the body effect (see [11] and [14] for an expression of this parameter, or [19] if polysilicon depletion is not negligible in the gate).

With χ_f and χ_r given, the dc current becomes simply

$$I_{F(R)}=I_{\rm S}\cdot\left(\chi_{f(r)}^2-\frac{1}{4}\right),\quad I=I_{\rm S}\cdot\left(\chi_f^2-\chi_r^2\right) \quad (2)$$

$$\text{with}\quad I_{\rm S}=2n\cdot\mu C'_{\rm OX}\cdot U_T^2\cdot\frac{W_{\rm eff}}{L_{\rm eff}} \quad (3)$$

where

- $W_{\rm eff}$ and $L_{\rm eff}$ — effective width and length of the device, including channel length modulation (CLM);

[1]To avoid any unnecessary repetition, only the expressions related to the source will be given. Use subscripts in bracket to get the expressions corresponding to the drain

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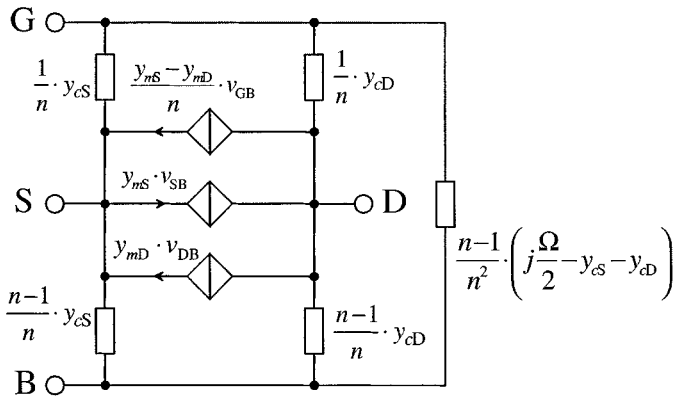

Fig. 1. Small signal NQS equivalent circuit.

$C'_{\rm OX}$ gate oxide specific capacitance;
μ effective average mobility, possibly taking into account the high field effects previously cited.

Finally, the dc source, drain and gate transconductances $g_{m\rm S}$, $g_{m\rm D}$ and $g_{m\rm G}$ are given by

$$g_{m\rm S(D)} = -(+)\frac{\partial I}{\partial V_{\rm S(D)}} = \frac{I_{\rm S}}{U_T}\cdot\left(\chi_{f(r)}-\frac{1}{2}\right) \quad (4)$$

$$g_{m\rm G} = \frac{\partial I}{\partial V_{\rm G}} = \frac{g_{m\rm S}-g_{m\rm D}}{n}. \quad (5)$$

The low frequency transcapacitances are not listed here, since they can be deducted from the general NQS expressions or found in [9], [12], [14]. This simple and efficient formulation gives a good description of the MOS operation, from weak to strong inversion and nonsaturation to saturation, and can be extended to introduce advanced features [14], [18]–[20].

B. NQS Small Signal Operation

Keeping the same framework than for the dc equations, it has been previously shown in [9] that a compact formulation of NQS effects can be derived without any additional assumption. These results, which are briefly reminded in an appendix, are at the root of the derivation presented in the next sections. However, the initial formulation is difficult to manipulate, since it is expressed in term of Bessel functions of fractional orders and of complex arguments. Such functions are not available in most programming environments, and their numerical evaluation tends to be slow and have a poor convergence.

Therefore, the results call for a simplification in order to become practical. Section II proposes a simple equivalent small-signal circuit, where only two fundamental functions of frequency are sufficient for expressing the values of all the elements. Then, by using a careful normalization, Section III shows that these functions can be represented in two simple abacus, which are valid for any transistor operating in any state. Next, in Section IV, approximate expressions are proposed. Finally, Section V compares the model with various measurements.

II. Equivalent Circuit

By studying the relationships between the generic (trans)admittances expressions given in [9], the equivalent circuit of Fig. 1 can be deducted, where the only remaining variables are $y_{c\rm S}$, $y_{m\rm S}$, $y_{c\rm D}$, and $y_{m\rm D}$. The complete expression for these quantities can be found in the appendix.

TABLE I
Normalization Factors

	Symbol	Normalization factor	Units
Voltage	$v = V/U_T$	$U_T = k_B T/q_e$	V
Current	$i = I/I_{\rm S}$	$I_{\rm S} = 2n\mu C'_{\rm OX}U_T^2\cdot\frac{W_{\rm eff}}{L_{\rm eff}}$	A
Admittance	$y = Y/Y_0$	$Y_0 = I_{\rm S}/U_T$	S
Capacitance	$c = C/C_{\rm SP}$	$C_{\rm SP} = 2nC'_{\rm OX}\cdot W_{\rm eff}L_{\rm eff}$	F
Frequency	$\Omega = \omega/\omega_0$	$\omega_0 = \mu U_T/L_{\rm eff}^2$	rad/s

Note that, from this point, all quantities (currents, voltages, frequencies, impedances) are normalized according to Table I. Normalized, unitless, quantities will be denoted by using lower case letters (i, v, y), as opposed to "normal" variables written in capitals (I, V, Y).

Thanks to the intrinsic device symmetry, the expressions of $y_{m\rm D}$ and $y_{c\rm D}$ can be obtained by exchanging χ_f and χ_r in the formulation of $y_{m\rm S}$ and $y_{c\rm S}$

$$y_{m\rm S} = y_m(\Omega,\chi_f,\chi_r) \quad y_{c\rm S} = y_c(\Omega,\chi_f,\chi_r) \quad (6)$$

$$y_{m\rm D} = y_m(\Omega,\chi_r,\chi_f) \quad y_{c\rm D} = y_c(\Omega,\chi_r,\chi_f). \quad (7)$$

Therefore the complete solution of the small-signal NQS behavior of the MOS model can be reduced to the two functions $y_m(\Omega,\chi_1,\chi_2)$ and $y_c(\Omega,\chi_1,\chi_2)$.

III. Further Frequency and Admittance Normalization

A further step can be achieved by separating each of the two remaining independent functions, y_m and y_c, into two factors: a low frequency term and an NQS term. At the same time, an additional normalization of the frequency can be introduced in such a way that the NQS term will depend only on the ratio $r = \chi_1/\chi_2$ (χ_f/χ_r at the source, χ_r/χ_f at the drain). The source factor $r = \chi_f/\chi_r$, is close to 1 in weak inversion or linear region. In strong inversion mode, it tends toward ∞ in forward saturation mode and toward zero in reverse saturation.

In order to achieve this simplification, a new normalized characteristic frequency $\Omega_{\rm crit}$ is introduced. It corresponds to the

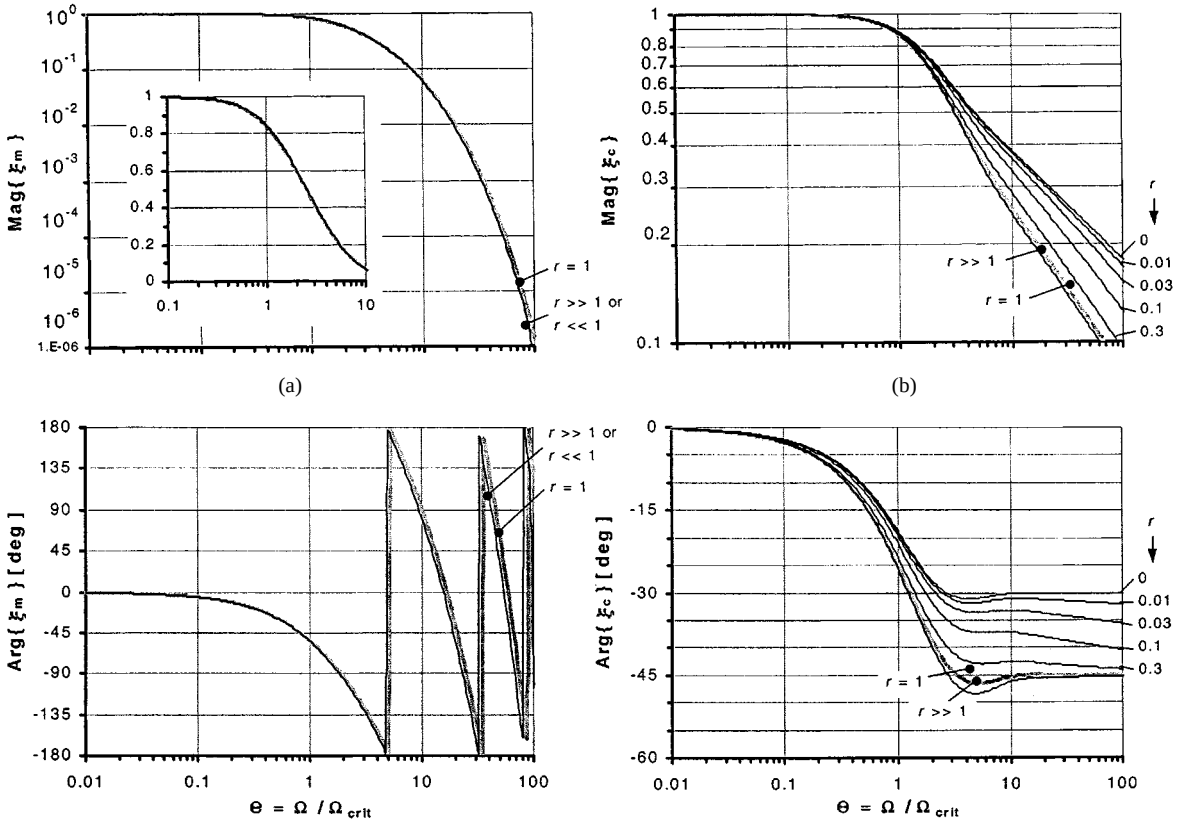

Fig. 2. To the left: Normalized $\xi_m(\Omega/\Omega_{\rm crit}, r)$ function for $r = 1$ (thick gray curve) and for $r \gg 1$ or $r \ll 1$ (thin curve). *To the right:* Normalized $\xi_c(\Omega/\Omega_{\rm crit}, r)$ function for $r = 1$ (thick gray curve), for $r \gg 1$ (lowest thin curve) and for $r = 0.3, 0.1, 0.03, 0.01$ and $r \to 0$ (other thin curves).

first pole of the characteristic function of the system (*i.e.*, of the denominator which is shared by both functions, $D(\Omega)$ in the appendix)

$$\Omega_{\rm crit} = \frac{15}{2} \cdot \frac{(\chi_f + \chi_r)^3}{\chi_f^2 + 3\chi_f\chi_r + \chi_r^2}. \tag{8}$$

Note that the expression of $\Omega_{\rm crit}$ is symmetrical in χ_f and χ_r, so that it is identical for the drain and source transconductances.

With this new definition, and from the relations recalled in the appendix, one can state

$$y_m(\Omega, \chi_1, \chi_2) = g_{m0} \cdot \xi_m\left(\frac{\Omega}{\Omega_{\rm crit}}, \frac{\chi_1}{\chi_2}\right) \tag{9}$$

$$y_c(\Omega, \chi_1, \chi_2) = j\Omega \cdot c_{c0} \cdot \xi_c\left(\frac{\Omega}{\Omega_{\rm crit}}, \frac{\chi_1}{\chi_2}\right) \tag{10}$$

with

$$g_{m0} = \left(\chi_1 - \frac{1}{2}\right) \tag{11}$$

$$c_{c0} = \left(\chi_1 - \frac{1}{2}\right) \cdot \frac{\chi_1 + 2\chi_2}{3 \cdot (\chi_1 + \chi_2)^2} \tag{12}$$

g_{m0} and c_{c0} are the normalized, low-frequency, fundamental ac transconductance and capacitance.

At frequencies Ω much lower than $\Omega_{\rm crit}$, corresponding to quasistatic (QS) operations, the two NQS functions ξ_m and ξ_c tend toward unity resulting in

$$y_m(\Omega, \chi_1, \chi_2) \to g_{m0} \cdot \left(1 - j \cdot \frac{\Omega}{\Omega_{\rm crit}}\right) \tag{13}$$

$$y_c(\Omega, \chi_1, \chi_2) \to j\Omega \cdot c_{c0}. \tag{14}$$

It can be verified that these last results correspond exactly to the usual small-signal QS model [12], [14]. In particular, the imaginary part of y_m in (13) corresponds to the drain-source transcapacitance. It comes from the first-order Taylor expansion of ξ_m in (9).

The two NQS functions $\xi_m(\Theta, r)$ and $\xi_c(\Theta, r)$ are plotted in Fig. 2, versus the renormalized frequency $\Theta = \Omega/\Omega_{\rm crit}$, and for different values of the parameter $r = \chi_1/\chi_2$. The two leftmost plots show that the transadmittance of the MOS device, quickly degrades with frequency. Indeed, a phase lag slightly in excess of 45° is already observed at $\Theta = 1$ and a factor of 2 is lost at $\Theta = 2.5$. Therefore, if NQS effects are to be avoided, the condition $\Theta \ll 1$ must be enforced. Surprisingly, the function ξ_m appears to be only weakly dependent on parameter r, so that this dependence can almost be ignored in practice.

The two rightmost plots of Fig. 2 show the degradation of the fundamental instrinsic capacitance with frequency. In the NQS regime, the channel must be considered as a distributed, nonuniform, RC line. So, y_c, which increases proportionally to Ω at low frequencies, start to vary only with $\sqrt{\Omega}$. Therefore, $\xi_c = 1$ for $\Theta \ll 1$ and $\xi_c \propto 1/\sqrt{\Theta}$ for $\Theta \gg 1$. The exact factor of proportionality at high frequencies depends on the ratio $r = \chi_1/\chi_2$. For $r \ll 1$ (reverse saturation), the -10 dB per decade slope is only reached at extremely high frequencies, which are not of practical interest and are not shown on the plots. Finally, it must be noted that the curves vary very little between $r = 1$,

corresponding to the linear regime or the weak inversion mode ($I \ll I_S$), and $r \to \infty$, corresponding to complete saturation in strong inversion mode ($I_F \gg I_S, I_R \approx 0$).

IV. Approximate Expressions

A. Linear Region or Weak Inversion ($r \approx 1$)

The special case $r = 1$ is important since, as noted above, it includes both the triode regime when $V_S = V_D$ and, asymptotically, the weak inversion mode. Moreover, the MOS behavior in saturation mode can be approximately described with the same set of functions.

From [9], the following simple equations can be derived:

$$\xi_m(\Theta, 1) = \tilde{\xi}_m(\Theta) \text{ where } \tilde{\xi}_m(\Theta) = \frac{\lambda}{\sinh \lambda} \tag{15}$$

$$\xi_c(\Theta, 1) = \tilde{\xi}_c(\Theta) \text{ where } \tilde{\xi}_c(\Theta) = 2 \cdot \frac{\cosh \lambda - 1}{\lambda \cdot \sinh \lambda} \tag{16}$$

$$\text{with} \quad \lambda = (1 + j) \cdot \sqrt{3\Theta}. \tag{17}$$

B. Forward Saturation ($r > 1$ and $\chi_r = 1/2$)

For the saturation mode, from weak to strong inversion, approximations which are within an accuracy of a few percents can be derived from (9)–(12) and Fig. 2

$$y_{mS} \approx \left(\chi_f - \frac{1}{2}\right) \cdot \tilde{\xi}_m(\Theta) \tag{18}$$

$$y_{cS} \approx j\Omega \cdot \frac{2(2\chi_f - 1) \cdot (\chi_f + 1)}{3(2\chi_f + 1)} \cdot \tilde{\xi}_c(\Theta) \tag{19}$$

$$y_{mD} \approx 0, \quad y_{cD} \approx 0. \tag{20}$$

C. General Case, Valid in any Mode of Operation

As previously stated, the function $\xi_m(\Theta, r)$ can already be considered as independent of r, even for $r < 1$ (again, see Fig. 2). However, this is not the case for the function ξ_c, the behavior of which varies significantly when $r \to 0$. Even so, the following approximation can be used:

$$\xi_m(\Theta, r) \approx \tilde{\xi}_m(\Theta) \tag{21}$$

$$\xi_c(\Theta, r) \approx \frac{\tilde{\xi}_c(\Theta)}{\sqrt[3]{\varrho + (1 - \varrho) \cdot \tilde{\xi}_c\left(\frac{\Theta}{2}\right)}} \tag{22}$$

$$\text{with} \quad \varrho = \left(\frac{10 \cdot r \cdot (r+2)^2}{9 \cdot (r+1) \cdot (r^2 + 3r + 1)}\right)^{3/2}. \tag{23}$$

Factor ϱ is always comprised between 0 ($r \to 0$) and 1.17 ($r \to \infty$). The approximation is done in such a way that the asymptotic behaviors, both for $\Theta \to 0$ and $\Theta \to \infty$, are preserved. The accuracy is always kept better than 1% of the dc transconductance value.

V. Experimental Results

A. Low-Frequency Impedance Measurements

In order to verify our theoretical approach, low frequency measurements on very long devices have first been undertaken. This kind of measurements are relatively easy to realize and quite accurate, since a precision LCR-meter can be used. Because the device can be made fairly large, the extrinsic elements can be ignored, eliminating the need for a manual de-embedding. Fig. 4 is an example of such a measurement performed on a 300×300 μm PMOS device integrated in a 0.35 μm process, and for a frequency varying between 75 kHz and 30 MHz. It shows an excellent agreement with theory, for a broad range of overdrive gate voltages, over three decades of frequency. The slight discrepancies appearing in the high frequency range are attributed to the extrinsic elements, mostly due to the packaging of the device. Note that, since high gate potential where applied, the effect of mobility reduction had to be taken into account. It was extracted from a standard $I(V_G)$ dc measurement.

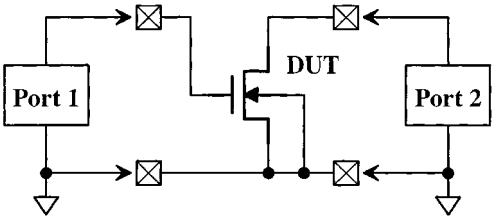

Fig. 3. Two-port on-wafer measurement setup.

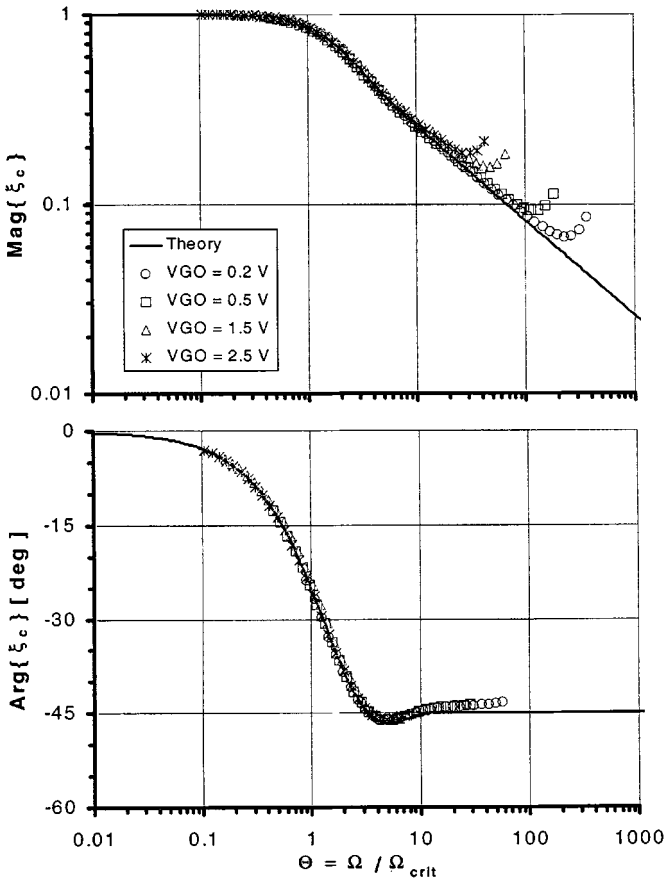

Fig. 4. Measurement of the ξ_c function (symbols), deduced from the normalized drain-to-gate transadmittance in linear mode, measured with an HP4285 LCR-meter. The device is a 300×300 μm PMOS transistor. The gate overdrive voltage was set to 0.2, 0.5, 1.5, and 2.5 V. The curves correspond to the theory.

B. High-Frequency S-Parameters Measurements

In order to verify the validity of the theory for shorter devices and at higher frequencies, test structures for on-wafer measurements were realized. Devices of various length between 10 and

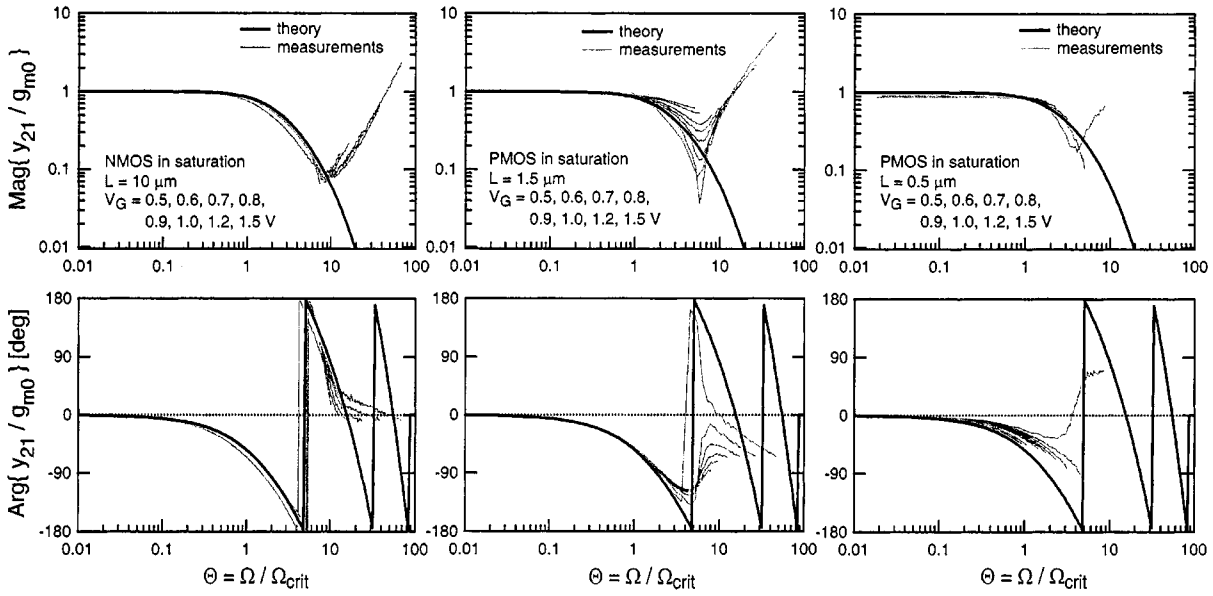

Fig. 5. Normalized gate transadmittance function, computed from the measured y_{21} parameter of the setup of Fig. 3 , with the device operating in saturation mode. 10 μm NMOS device measured between 1 MHz and 1 GHz (left), 1.5 μm (center) and a 0.5 μm (right) PMOS devices measured between 100 MHz and 10 GHz. The top plots represent magnitude, the bottom ones phase in degrees. The x axis is always the normalized frequency $\Theta = \Omega/\Omega_{\rm crit}$. In each case, the gate overdrive voltage is varied between 0 and about 1 V, corresponding to the moderate and strong inversion regions. The black curves correspond to the theory.

0.5 μm were integrated on a 0.35 μm process. The measurements were carried out by using a standard wafer prober station and a network analyzer. This kind of S-parameters measurements are less accurate than with an LCR-meter, but they are the only available technique at frequencies higher than a few MHz. Note also that the measurements are even made more difficult since a wide impedance range is required, in order to cover a large frequency and operating point range.

The two-port measurement setup is depicted in Fig. 3. The selected de-embedding process is two-step. First, as usual [21], [22], the pad and interconnects contribution must be removed from each device under test (DUT) measurements by subtracting the Y-parameters matrix of an "open" test structure from the Y-matrix of the DUTs. For the frequency range that was required here ($<$ 10 GHz), the series access impedance can be assumed negligible.

The second step consists in removing the effect of the extrinsic elements (mostly overlap and junction capacitor). This was done by subtracting two Y-matrix of the same DUT, the first one with the device biased normally, and the second one at a zero gate voltage, in order to almost achieve the flat-band condition under the gate.

The resulting Y-parameters, normalized to Y_0, can be expressed in terms of the fundamental transconductances

$$[\mathbf{y}] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{n^2}\cdot(y_{c\rm S}+y_{c\rm D}) & \frac{1}{n}\cdot y_{c\rm D} \\ \frac{1}{n}\cdot(y_{m\rm S}-y_{m\rm D}) & y_{m\rm D}+y_{c\rm D} \end{bmatrix}. \quad (24)$$

This relation assumes that the extrinsic capacitances vary little with the gate voltage. As this condition does not completely apply to the overlap capacitances, the validity range of this kind of extraction is limited. However, if not perfect, this process still appears to be the only simple way to capture the intrinsic behavior of the device without adding many tuning parameters.

In saturation mode and in the linear region ($V_{\rm S} = V_{\rm D}$), respectively, the Y-matrix reduces to

$$[\mathbf{y}_{\rm sat}] \approx \left(\chi_f - \frac{1}{2}\right) \times \left(\tilde{\xi}_m(\Theta)\cdot\begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} + \frac{5}{4}\cdot j\Theta \cdot \frac{(\chi_f+1)(2\chi_f+1)}{4\chi_f^2+6\chi_f+1}\cdot\tilde{\xi}_c(\Theta)\cdot\begin{bmatrix} \frac{1}{n^2} & 0 \\ 0 & 0 \end{bmatrix}\right) \quad (25)$$

$$[\mathbf{y}_{\rm triode}] = \left(\chi_f - \frac{1}{2}\right) \times \left(\tilde{\xi}_m(\Theta)\cdot\begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} + 3j\Theta\cdot\tilde{\xi}_c(\Theta)\cdot\begin{bmatrix} \frac{2}{n^2} & \frac{1}{n} \\ 0 & 1 \end{bmatrix}\right). \quad (26)$$

Parameter y_{21} in saturation, y_{12} and y_{22} in the linear region have been measured on different devices. They are plotted in Figs. 5–7, respectively, and are compared to the theoretical values using the following expressions, derived from (25) and (26):

$$\begin{aligned} \frac{y_{21,\rm sat}}{g_{m0}} &= \tilde{\xi}_m(\Theta); \\ \frac{y_{12,\rm triode}}{g_{m0}} &= 3j\Theta\cdot\tilde{\xi}_c(\Theta); \\ \frac{y_{22,\rm triode}}{g_{m0}} &= \tilde{\xi}_m(\Theta) + 3j\Theta\cdot\tilde{\xi}_c(\Theta). \end{aligned} \quad (27)$$

In each figure, the measured normalized phases and magnitudes are compared to their theoretical value for a 10 μm length

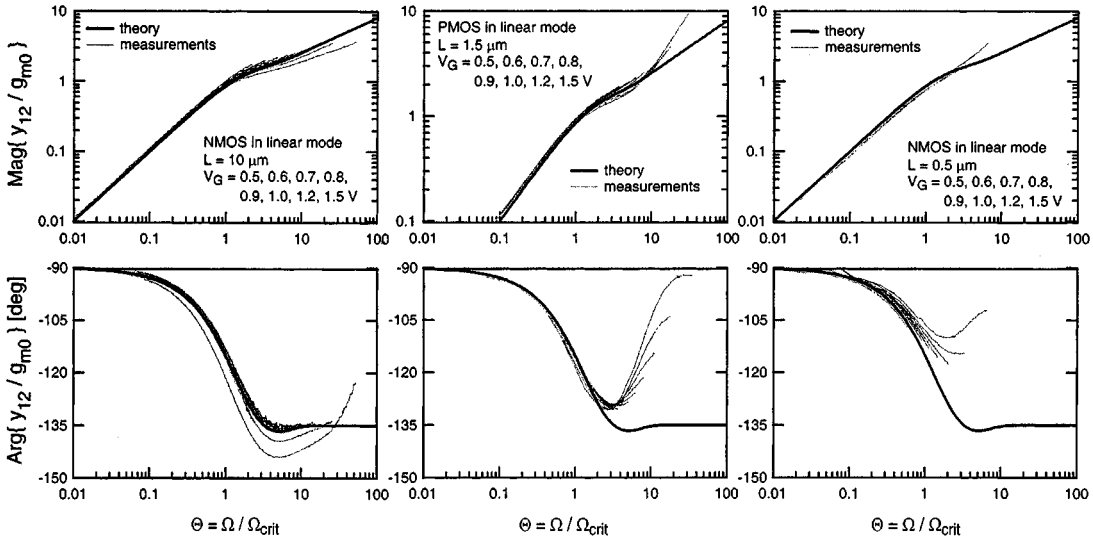

Fig. 6. Normalized drain-to-gate transadmittance function, computed from the measured y_{12} parameter of the setup of Fig. 3, with the device operating in linear mode. See the caption of Fig. 5 for further information.

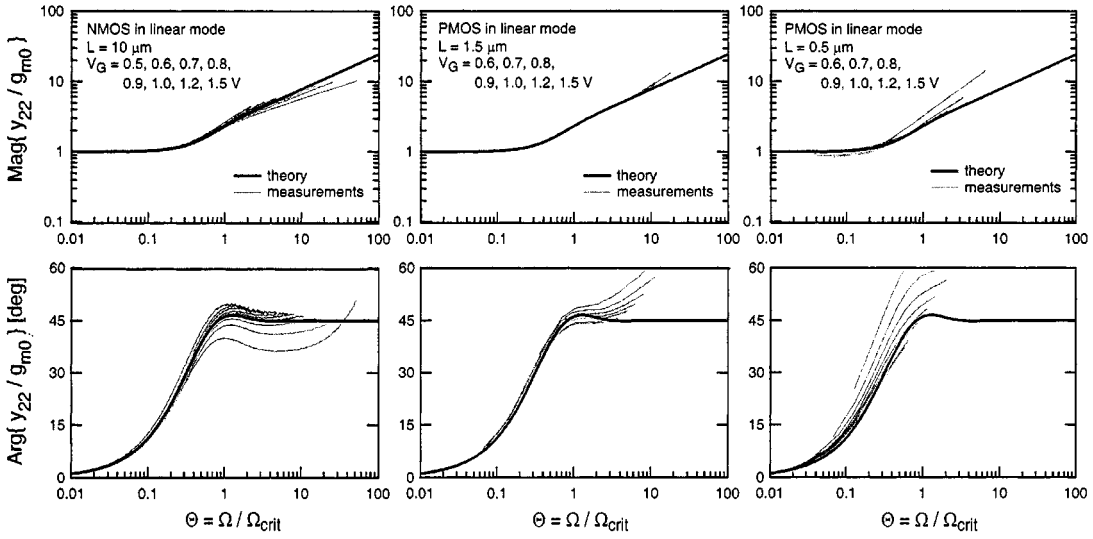

Fig. 7. Normalized drain admittance function, computed from the measured y_{22} parameter of the setup of Fig. 3, with the device operating in linear mode. See the caption of Fig. 5 for further information.

NMOS device, a 1.5 μm and a 0.5 μm PMOS devices, for frequencies up to 10 GHz, and at different levels of inversion. Other device lengths (5, 1 and 0.7 μm) have also been measured with similar results. For short channels, P-type devices have been selected since their characteristic frequency is lower.

Fig. 5 shows the evolution with frequency of the gate-to-drain transadmittance (corresponding to $g_{m\mathrm{G}}$) at low frequency. For the 10 μm device, a very good agreement is found up to 10 times the characteristic frequency, corresponding to a complete 360 ° turn in phase. For shorter channels, the trend is also clearly seen, even though extrinsic elements limit the range of validity to about 6 Ω_{crit} for the 1.5 μm device and only 3 Ω_{crit} at 0.5 μm.

The second set of plots, in Fig. 6, describes the drain-to-gate capacitive coupling. It shows a similar agreement and clearly validates the proposed normalization. Finally, Fig. 7, displaying the drain output admittance in the linear region, indicates again that the NQS behavior is well captured by the simple proposed formulation. Note that in all these figures, all the measured curves fall very close to each other, which confirms the validity of the frequency and bias normalization processes.

VI. Conclusion

A compact charge-based description of the small-signal NQS effects in the intrinsic MOS transistor has been presented. Using a proper normalization of all quantities in the model, it was possible to reduce it to a simple equivalent circuit, which could be fully described by only two frequency-dependent generic functions.

This theoretical approach was confirmed by measurements, up to 10 GHz, of both N-type and P-type MOS transistors operated in various state of inversion, either in triode or in saturation mode. For the first time, clean measurements of NQS effects in submicron devices (down to 0.5 μm) which are not dominated by extrinsic elements have been presented. They clearly corroborate the normalization procedure as well as the proposed model.

APPENDIX
EXACT NQS EXPRESSIONS

This paper is based on the exact small-signal NQS expressions given in [9]. All the functions appearing in the equivalent circuit of Fig. 1 can be computed without any simplification with the following:

$$y_{m\mathrm{S(D)}}(\Omega) = \left(\chi_{f(r)} - \frac{1}{2}\right) \cdot \frac{\chi_f^2 - \chi_r^2}{\chi_f \cdot \chi_r} \cdot \frac{3\sqrt{3}}{4\pi \cdot D(\Omega)} \quad (28)$$

$$y_{c\mathrm{S(D)}}(\Omega) = y_{m\mathrm{S(D)}}(\Omega) \pm \left(\chi_{f(r)} - \frac{1}{2}\right) \times \frac{j-1}{2} \cdot \sqrt{\frac{\Omega}{\chi_{f(r)}}} \cdot \frac{N_{f(r)}(\Omega)}{D(\Omega)} \quad (29)$$

$$D(\Omega) = J_{-2/3}[F_f(\Omega)] \cdot J_{2/3}[F_r(\Omega)] - J_{-2/3}[F_r(\Omega)] \cdot J_{2/3}[F_f(\Omega)] \quad (30)$$

$$N_{f(r)}(\Omega) = J_{-1/3}[F_{f(r)}(\Omega)] \cdot J_{-2/3}[F_{r(f)}(\Omega)] + J_{1/3}[F_{f(r)}(\Omega)] \cdot J_{2/3}[F_{r(f)}(\Omega)] \quad (31)$$

$$F_{f(r)}(\Omega) = \frac{2}{3} \cdot (1-j) \cdot \sqrt{\frac{\Omega}{\chi_{f(r)}}} \cdot \frac{\chi_{f(r)}^2}{\chi_f^2 - \chi_r^2} \quad (32)$$

where $J_\nu(x)$ is the Bessel function of the first kind of order ν. In (29), the plus sign corresponds to the expression of $y_{c\mathrm{S}}$, the minus sign to $y_{c\mathrm{D}}$. These expressions leads to $0/0$ indeterminates when $\chi_r = \chi_f$ (triode mode or asymptotic weak inversion regime). Use the alternate expressions (15) and (16) given in Section IV in these cases.

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