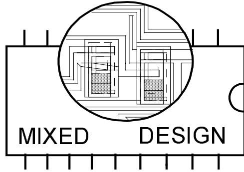

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ADVANCEMENTS IN DC AND RF MOSFET MODELING WITH THE EPFL-EKV CHARGE BASED MODEL

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ABSTRACT:
We discuss new developments of the compact EPFL-EKV charge based model for analog circuit simulations that are consistent with advanced CMOS technology. The physical foundations of the EKV model and in particular the normalization of the currents and charges are presented and their implications on the model structure are discussed. Based on the hierarchical model description, new effects such as poly gate depletion and quantum confinement can be simply considered as a model generalization. Finally, the consistency of the model is illustrated through the related RF derivation whose equivalent circuit, based on normalized transadmittances and frequencies, can be expressed as a combination of two generic functions only.

INTRODUCTION

The EKV model was initially developed [1] for low voltage-low power applications, for which the transitions between the different modes of operation of the MOS transistor must be especially well described. In particular the requirement for good CMOS analog circuit simulation requires accuracy and continuity of the large and small signal characteristics [2] even for advanced technologies. Until 1994 when the EKV model was presented for the first time, no continuous model was available in public domain. Originally [1], the EKV model was based on a mathematical interpolation of the MOS transistor current between weak and strong inversion and from conduction to saturation using a minimum set of model parameters. The model introduces new concepts, which are essential to the definition of normalized variables useful for hand calculation. A major improvement was further achieved by adopting a physical description of the inversion charge density, owing to derive continuous expressions for the MOS charges valid in all modes of operation [3-5]. Based on the particular structure of the model, new submicron CMOS technology effects can be simply considered as a generalization of the basic definitions [6], still keeping a minimum number of parameters (less than 20 parameters for the model discussed here). In particular, exact and efficient analytical solution to non-quasi-static operation in small signal regime could be derived without any extra assumption compared to the DC model [7,8].

THE DC MODEL

A detailed description of the model formulation and related parameter extraction procedures can be found in [5,9,10]. In this section, we will illustrate important concepts that are used in EPFL-EKV model.

Basic Model Concepts

According to the charge sheet approximation approach, the channel current in a MOS transistor can be expressed a function of the surface potential at source and drain ends whose values can be evaluated numerically. Despite this approach needs no assumption, it can hardly be used for DC and AC hand calculations, in contrast with the EKV model [1,2]. Moreover, unlike most other simulation models, the gate, source and drain voltages are referred to the substrate owing to preserve the symmetry of the device. Among the new features introduced by the model, three of them are of major importance and need to be discussed, namely the linearization of the inversion charge density, the normalization of currents and charges and the definition of the pinch-off voltage.

Linearization of the inversion charge is shown on fig. 1 (full line) where the inversion charge density Q'_I is calculated numerically as a function of the surface potential ψ_S for a given gate voltage.

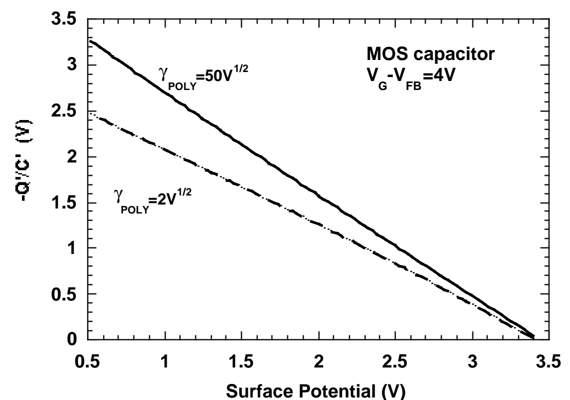


Figure 1. *Inversion charge density as a function of the surface potential. Dotted line corresponds to the poly-depletion case.*

Despite basic MOS relations involved in this evaluation are highly non linear, the inversion charge density is found to vary almost linearly with the surface potential from weak to strong inversion (fig. 1).
This is considered as the starting point for the new derivation of the EKV charge based model. A simple and useful relation can then be obtained between the inversion charge density Q'_I and the surface potential ψ_S in a differential form [3,6]:

$$dQ'_I / C'_{OX} = n_Q \cdot d\psi_S \tag{1}$$

The factor n_Q represents the *normalization factor*. Its value depends on the gate voltage but is still close to unity (see fig. 3). It can be shown that this approximation is valid from weak to strong inversion, i.e. for a large range of gate voltages.

The normalization of currents and charges is a direct consequence of the linearization concept. Starting from the general current expression in a MOS transistor, we can define a normalized current i as:

$$i = I / I_S \tag{2}$$

and a normalized inversion charge density q_I':

$$q'_i = Q'_I / Q_S \tag{3}$$

where I_S and Q_S are the specific current and charge [1,7]:

$$I_S = 2 \cdot n_Q \cdot \mu \cdot C'_{OX} \cdot U_T^2 \cdot W/L \tag{4}$$

$$Q_S = 2 \cdot n_Q \cdot C'_{OX} \cdot U_T \tag{5}$$

(U_T is the thermal voltage, other symbols having their usual meaning). Furthermore, the normalized current i can be expressed as the difference between a forward i_f and a reverse i_r normalized currents:

$$i = i_f - i_r \tag{6}$$

whose values depend on the normalized inversion charges at the source and at the drain [7]:

$$i_{f,r} = q'^2_{s.d} - q'_{s,d} \tag{7}$$

A different definition of the forward and reverse current was originally proposed in [1]. Equivalence between these two definitions is discussed in annex B.
Normalized current representation is a very efficient tool to characterize the operating point of the MOS transistor. For example, i_f less than 0.1 corresponds to weak inversion, i_f equal to 1 is the center of moderate inversion and i_f above 10 is strong inversion [1,2]. Then, knowing the technological parameters and providing the normalized currents are calculated, the MOS transistor is completely characterized. However, it can be shown in annex A that the evaluation of these charges requires the knowledge of the channel potential for which the inversion charge density, extrapolated from strong inversion, becomes zero [1,7]. This last point constitutes the third important concept of the EKV model.

The definition of the pinch-off voltage is depicted on fig. 2 where the inversion charge density is represented as a function of the channel potential V_{CH}, for a given gate voltage. The pinch off voltage corresponds to the value of the channel potential for which the inversion charge density, extrapolated from strong inversion, becomes zero (according to the discussion in annex B, the dashed surface represents the normalized current *i*). Furthermore, fig. 3 shows that the gate voltage dependence of the pinch-off voltage is nearly linear. This allows deriving a simplified but useful expression of $V_P(V_G)$ as a function of two parameters only, V_{TO} and n_V:

$$V_P = (V_G - V_{TO}) / n_V \tag{8}$$

The factor n_v is called the *slope factor* and depends slightly on the gate voltage, varying from 1.2 to 1.6 in strong and weak inversion respectively (see full line on fig. 3). The definition of the slope factor will be the essential to obtain a reduced representation of the small signal MOSFET parameters. From fig. 3 (full lines) and according to relation (8), the threshold voltage V_{TO} corresponds to the gate voltage that cancels the inversion charge under equilibrium condition, i.e. $V_P = 0$ (provided the source potential is set to 0, this definition is equivalent to the threshold voltage in source referenced models). Defining normalized voltages as $v = V / U_T$, it can be shown (annex A) that the drain and source inversion charge densities are given by the important relation:

$$\ln(-q'_{s,d}) - 2 \cdot q'_{s,d} = v_p - v_{s,d} \tag{9}$$

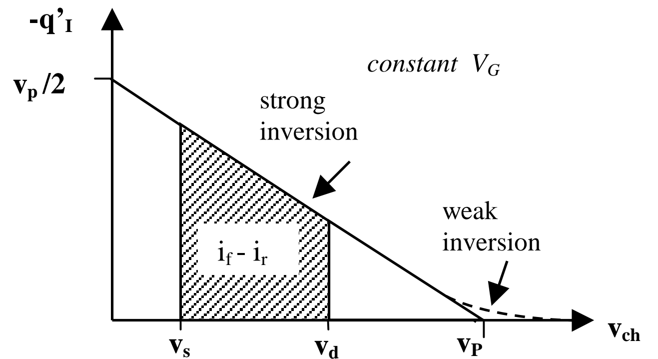


Figure 2. *Schematic representation of the normalized inversion charge density as a function of the channel voltage.*

Then, knowing gate, source and drain potentials, normalized charges and currents can be calculated through relations (9) and (7) as well as the linearization factor [7]. Based on this simple model structure, additional effects imposed by submicron CMOS technologies will be taken into account in a coherent way. It is important to note here that according to relation (1), the model equations can be equivalently formulated in terms of the surface potential ψ_S. As a consequence, the EPFL-EKV model can also be considered as *a surface potential based model.*

Second Order Effects

The use of thin gate oxides, high levels of channel doping concentration and poly-silicon gates lead to increased influence of polysilicon depletion and quantum effects. The goal of this section is not to give an exhaustive enumeration of second order effects that are included in the EKV model, but rather to illustrate most recent corrections, which can be considered as a generalization of the model itself. Other effects such as non-uniform substrate doping, reverse short channel effects, short and narrow channel effects, mobility reduction and velocity saturation are discussed in more details in [5,11-14].

Depletion of the polysilicon gate is accentuated in advanced CMOS technologies and should be well modeled since it affects all the device characteristics, in particular the charges and transcapacitances [6]. Figure 3 (dotted line) depicts how polysilicon gate depletion affects the dependence of the inversion charge density versus the surface potential.
The substrate and polygate body factors that are given by $\Gamma_{sub,poly} = \sqrt{2 \cdot q \cdot \varepsilon \cdot N_{sub,poly}} / C_{OX}^{'}$, and both depend on the substrate and gate doping concentrations. Particularly, for strong polydepletion case ($\Gamma_{poly} = 2$), the inversion charge density remains almost linear versus the surface potential. However, the normalization factor n_Q is found to decrease as compared to the ideal case (see dotted lines on fig. 3), implying that under polydepletion, the inversion charge density is reduced for the same surface potential (relation (1)).

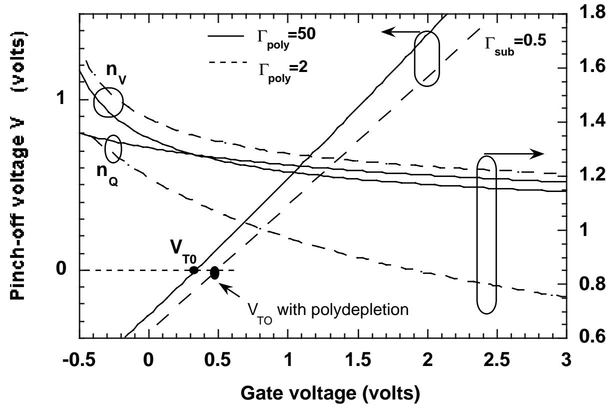


Figure 3. *Normalization factor, slope factor and pinch-off voltage as a function of the gate voltage for Γ_{poly}=2 (polydepletion) and Γ_{poly}=50 (no polydepletion).*

Furthermore, polydepletion also weakens the dependence of the pinch off voltage versus the gate voltage (dotted line on fig. 3), thus increasing the slope factor n_v and the threshold voltage V_{T0} as shown on fig. 3. This can be interpreted as a lower effect of the gate voltage as compared to the channel potential.

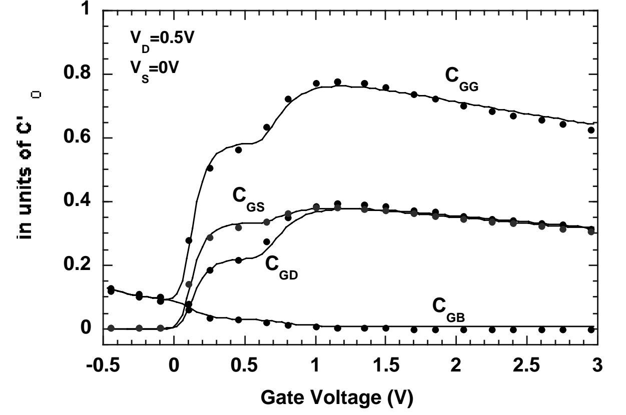


Figure 4. *Effect of polydepletion on the MOS transcapacitances. Dots represent 2D simulations. Lines are the model prediction.*

As a consequence, polydepletion has two distinct effects: a decrease of the normalized currents and charges through the decrease in the pinch-off voltage V_p, and a decrease in the specific current and charges through the linearization factor n_Q. It can be shown that the pinch-off voltage is weakly affected by polydepletion. Then, polydepletion will have negligible effect on normalized currents and charges.
Finally, since this approach is derived locally (we do not define an averaged gate oxide capacitance), all the MOS transcapacitances are well predicted even under non-equilibrium conditions (see fig. 4). Note that only one extra parameter was introduced in the model, namely the gate substrate doping concentration, or equivalently the polysilicon body effect Γ_{poly}.

Quantum effects in MOS transistors are the consequence of energy quantization in the channel due to the high electric field at the Si-SiO_2 interface in nanometer scaled gate oxide. Despite an exact calculation of this effect requires a quantum theory approach thus the charge linearization scheme could still be extended to account for this new effect.
We have shown that adopting a charge based description of the energy quantization [15], this effect could be taken into account simply by defining new values for the gate oxide capacitance C'_{QE}, for the substrate body factor Γ_{sub}^{QE} and for an apparent polysilicon gate body factor Γ_{poly}^{QE}, without introducing any new model parameter:

$$C_{QE}^{'} = C_{OX}^{'} / \left(1 + a_1 \cdot C_{OX}^{'}\right) \tag{10}$$

$$\Gamma_{sub}^{QE} = \Gamma_{sub} \cdot \left(1 + a_1 \cdot C_{OX}^{'}\right) \tag{11}$$

$$\Gamma_{poly}^{QE\,2} = \Gamma_{poly}^{2} \cdot \left(1 + a_1 \cdot C_{OX}^{'}\right)^2 \cdot \left[1 - a_2 \cdot \left(\Gamma_{poly} \cdot C_{OX}^{'}\right)^2\right]^{-1} \tag{12}$$

where a_1 and a_2 are positive coefficients independent of the technology parameters of the MOS transistor. Based on this approach, quantum effects can be only considered as a correction to the MOS transistor parameters, leaving unchanged the fundamental model equations. In particular, as for polydepletion, charges

are locally calculated along the channel, owing to correctly describe the charges in the MOS transistor even under non-equilibrium conditions.

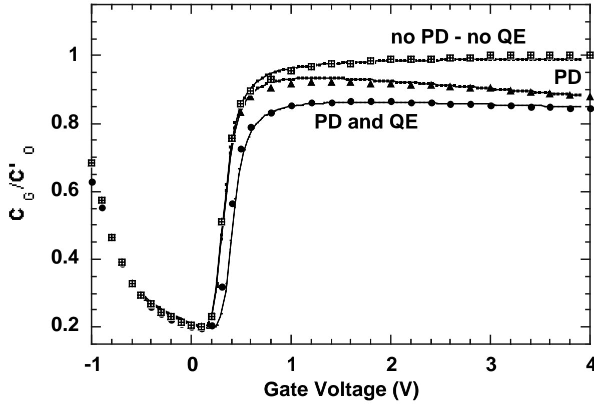


Figure 5. *Gate capacitance versus gate voltage for different combinations of polydepletion and quantum effects (symbols: 2D simulation, lines: analytical model).*

According to the relations (10) to (12), quantum effects can be simply considered as a decrease in gate oxide capacitance and increases in the substrate body factor. Concerning Γ_{poly}^{QE}, it can no longer be identified to a polysilicon gate body factor since $\left(\Gamma_{poly}^{QE}\right)^2$ can be either positive or negative. This can be interpreted as an apparent reduction of the polydepletion by quantum effects.

As a consequence, the pinch-off voltage V_P, the slope factor n_v and the linearization factor n_Q will also be affected by channel quantization. Note that for small values of the gate oxide capacitance, quantum effects become negligible, leaving unchanged the technological MOS parameters. Combined effects of polydepletion and quantum confinement are illustrated in fig. 5 where the analytical model (lines) accurately fits the 2D numerical device simulations (symbols) of the gate capacitance (C_G) of an n-channel MOS transistor from depletion to strong inversion.

THE NON QUASI-STATIC MODEL

Accurate modeling and efficient parameter extraction of the small signal MOS transistor at high frequency is a difficult task for submicron CMOS technology [16-18]. It is well known that for frequencies higher than a given device-dependant limit, the current gain of a MOS transistor is quickly degrading. This phenomenon is due to the fact that the modulation of the inversion channel charge is not instantaneous for fast varying external potentials. Hence, neglecting these so-called Non-Quasi-Static (NQS) effects can result in unpredictable behavior of high-frequency circuits. Despite various efforts devoted to high frequency and transient modeling of the MOS transistor, using both numerical and analytical approaches, only incomplete sets of first order NQS expressions were proposed for the kind of model discussed here.

An exact analytical solution of the small signal NQS behavior of MOS transistors built on a charge-based compact model and valid in all the modes of operation, was derived without any assumption [7] and was validated by measurements on the submicron CMOS devices. This NQS model is derived from the charge conservation principle and basic DC MOS transistor relations (see (1) to (7)). The time dependence of the small signal currents and charges was derived analytically through the whole channel in term of Bessel functions of imaginary argument.

In addition to the normalization of the currents and charges introduced in the DC model (relations (2) to (5)), we introduce a normalized frequency Ω defined by:

$$\Omega = \omega / \omega_0 \tag{13}$$

where $\omega_0 = \mu \cdot U_T / L^2$ depend on the MOS transistor parameters. As consequence, it is possible to define normalized transconductances as a function of the normalized variables (frequency Ω, and forward and reverse currents (i_α) and voltages (v_β)) [7]:

$$y_{\alpha\beta} = \delta i_\alpha / \delta v_\beta \tag{14}$$

By studying the relationships between the generic transadmittance expressions [7], the equivalent circuit of fig. 6 can be deducted [8] (where $n=n_v$). The only remaining variables are y_{cs}, y_{ms}, y_{cd}, and y_{md} as shown on fig. 6. Furthermore, thanks to the device symmetry, y_{md} and y_{cd} can be obtained from y_{ms} and y_{cs} by exchanging i_f and i_r only, thus reducing the calculation of the 16 transadmittances to the evaluation of 2 generic functions.

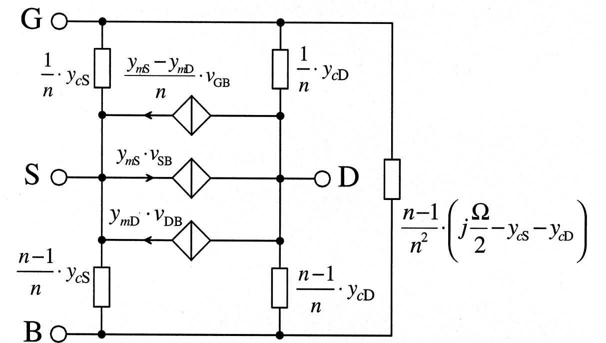


Figure 6. *Small signal NQS equivalent circuit.*

However, since the exact formulations of these functions are expressed in terms of Bessel functions of imaginary argument, this formulation is difficult to manipulate. Such functions are not available in most programming environments. Therefore, first and second order expansions are required. Figure 7 compares the first order (dashed lines) and second order (dotted lines) approximations of y_{dg} (or equivalently $y_{21} = (y_{ms} - y_{md})/n_v$) to the exact solution (full lines).

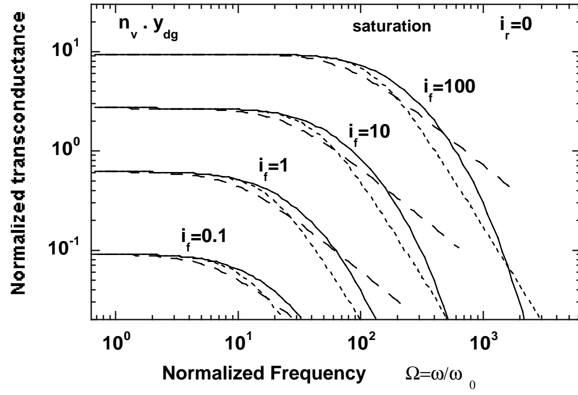


Figure 7. *Normalized transadmittance y_{dg} (y_{21}) as a function of the normalized frequency Ω for different level of inversion and in saturation. Full line: exact calculation. Dashed and dotted lines: first and second order approximations respectively.*

Going a step further, low frequency small signal parameters are obtained from the first order development of the non-normalized transconductances [7], reducing to:

$$Y_{\alpha\beta} = g_{\alpha\beta} + j \cdot \omega \cdot C_{\alpha\beta} \tag{15}$$

where $g_{\alpha\beta}$ and $C_{\alpha\beta}$ represent the transconductance and transcapacitance between nodes α and β. According to the general relations between transconductances (see fig. 6), only 6 independent real parameters (4 transcapacitances and 2 transconductances) are needed to fully describe the low frequency small signal behavior of the intrinsic MOS transistor, namely g_{ds}, g_{sd}, C_{dg}, C_{sg}, C_{ds}, C_{sd} [7].

Figure 8 demonstrates some of the 16 transcapacitances as a function of the pinch-off voltage for V_{DS}=1 volt. Note that the transcapacitances are continuous from weak to strong inversion as well as consistent with charge conservation principle.

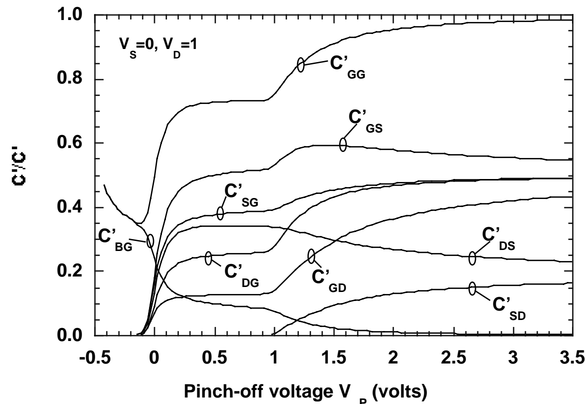


Figure 8. *Normalized transcapacitances as a function of the pinch-off voltage derived from the NQS model.*

In addition, a useful relation is obtained for the normalized transconductance to current ratio useful for analog design [19] and independent of temperature and MOS parameters. It is included in the normalization and slope factor calculation:

$$g_m/i = 2/\left(1+\sqrt{1+4\cdot i}\right) \tag{16}$$

Further frequency and admittance normalization is achieved by identifying a low frequency term and a non quasi static term in the independent functions y_{ms} and y_{cs}. An additional normalization of the frequency is introduced. Defining Ω_{crit} as the first pole in the first order developpement of the normalized transconductances [7] (Ω_{crit} is the same for source and drain transconductances) allows to obtain an expression in the form [8]:

$$y_m\left(\Omega/\Omega_{crit}, q'_s, q'_d\right) = g_{m0} \cdot \xi_m\left(\frac{\Omega}{\Omega_{crit}}, \frac{0.5-q'_s}{0.5-q'_d}\right) \tag{17}$$

$$y_c\left(\Omega, q'_s, q'_d\right) = j \cdot \Omega \cdot c_0 \cdot \xi_c\left(\frac{\Omega}{\Omega_{crit}}, \frac{0.5-q'_s}{0.5-q'_d}\right) \tag{18}$$

where q'_s and q'_d are the normalized inversion charge densities at the source and at the drain, and g_{m0} and c_0 are the normalized low frequency basic transconductance and transcapacitance given by:

$$g_{m0} = -q'_s \tag{19}$$

$$c_0 = -q'_s \cdot \frac{3/2 - q'_s - q'_d}{3 \cdot \left(1 - q'_s - q'_d\right)^2} \tag{20}$$

The functions ξ_m and ξ_c represent the NQS correction that will depend only on the normalized source and drain inversion charge densities $r = \left(0.5 - q'_s\right)/\left(0.5 - q'_d\right)$. In the low frequency limit, i.e. $\Omega << \Omega_{crit}$, corresponding to the quasi static operation, these two functions tend to unity. As a consequence, the generic function y_m and y_c will tend to the usual small signal relations. Furthermore, the function ξ_m can be considered as independent of the ratio *r*, allowing depicting any transistor operating at any inversion level by a unique curve. However, such approximation cannot be used the function ξ_c whose behavior varies significantly with the normalized inversion charge densities [8].

Approximate expressions that can be implemented in circuit simulators can be derived from the above frequency normalisation and shows an excellent accuracy compared with exact expressions for both ξ_m and ξ_c functions [8]. Moreover, since ξ_m can be considered as independent of the normalized inversion charge densities ratio *r*, the MOS transistor behavior can be approximately described with the same function obtained for *r=1* that only involve hyperbolic sine and cosine. This is not the case for the ξ_c function that varies with *r*. However, it is possible to simplify the expressions of ξ_c for asymptotic values of *r,* allowing obtaining a very simple formulation, which is within one

percent accuracy compared with exact analytical expressions [8].

RF measurements on MOS channel length ranging from 300 to 0.5 µm integrated on a 0.35µm CMOS process confirm the validity of this derivation.
In order to verify our approach, low frequency measurements have been carried out on a 300µm length MOS transistor, thus reducing the contribution of parasitic elements. Such measurements are quite accurate since a precision LCR-meter can be used. Figure 9 depicts the measurement of the normalized y_{12} or equivalently y_{dg}, according to the definition given in relation (14) for a frequency varying between 75kHz and 30MHz and for $V_D=V_S=0$. It shows an excellent agreement with theory over three decades of frequency for a broad range of gate voltages. Note that the bump occurring around $\Omega/\Omega_{crit}=4$ is very well predicted. Figures 10a and 10b shows the module and phase of the normalized gate-to-drain transadmittance y_{21} (or equivalently y_{gd}) under various levels of inversion, both for theoretical and experimental data, and without any parameter fitting. The measured normalized phases and amplitudes of the normalized gate to drain transadmittance are compared to their theoretical value for a 10 µm length NMOS device (fig. 10a) and a 0.5 µm PMOS device (fig. 10b). The agreement between the theory and measurements is very good for measurements up to 10GHz and under different levels of inversion.

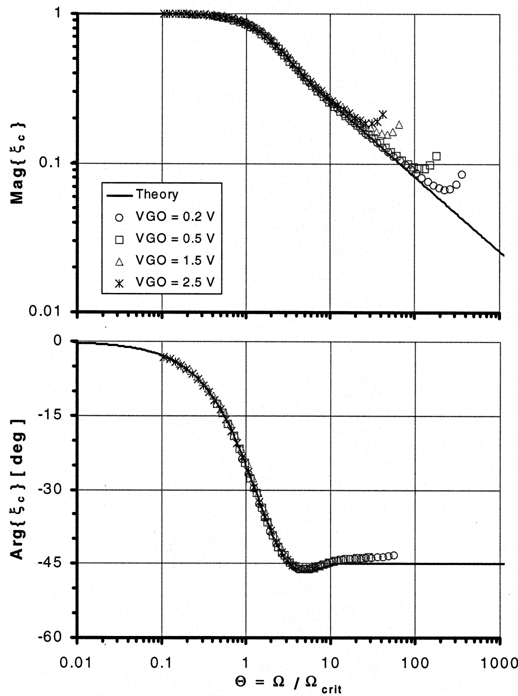
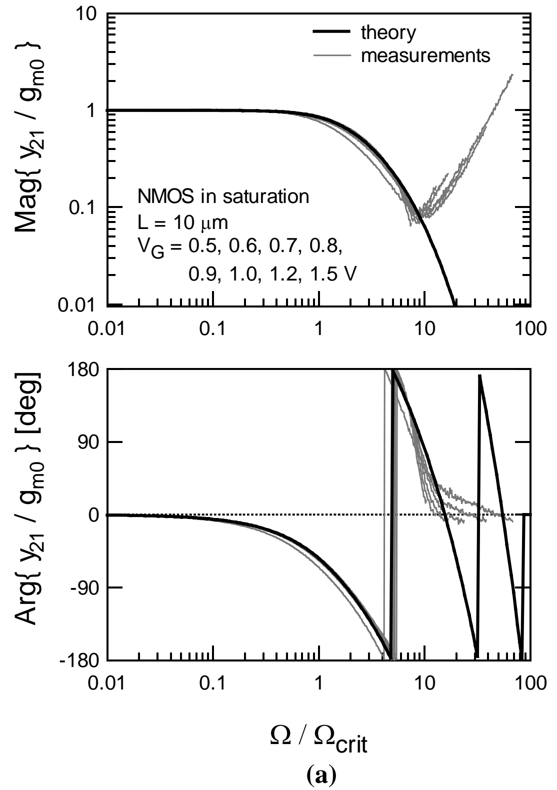
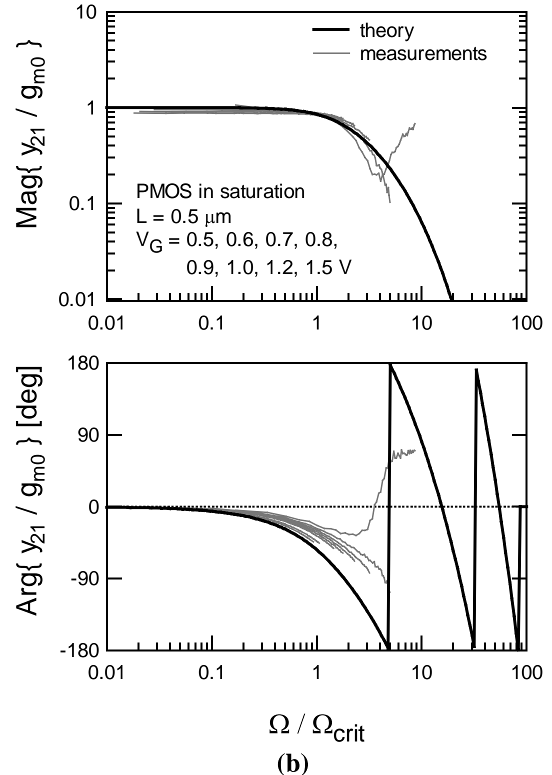


Figure 9. *Measurement of the ξ_c function (symbols) obtained from drain-to-gate transadmittances in linear mode and for various gate voltages. The curves correspond to theory.*



(a)



(b)

Figures 10. *Normalized module and phase of the gate transconductance for a 10µm NMOS device operating in saturation between 1MHz and 1GHz (a) and for a PMOS device operating in saturation between 100MHz and 10GHz (b). Both cases cover moderate to strong inversion regimes.*

Again, for very high frequencies, extrinsic elements, mostly due to the measurement setup, degrades accuracy. For the 10 µm device, a very good agreement is found up to 10 times the characteristic frequency,

corresponding to a complete 360 turn in phase (fig. 10a). For shorter channels, the trend is also clearly seen, even though extrinsic elements limit the range of validity to 3 Ω_{crit} at 0.5 µm (fig. 10b).
Note that in all these figures, all the measured curves fall very close to each other, which clearly validates the model foundations and the proposed normalization processes. From the bias voltages, the normalized inversion charge densities q'_s and q'_d must first be computed according to relation (9) and used in the calculation of g_{m0}, c_0 and Ω_{crit}. The effect of geometry lies fully in the normalization frequency Ω.

CONCLUSION

We have presented more recent developments of the EPFL-EKV charge based model. Starting from fundamental assumptions, we derived complete DC and RF normalized expressions that lead to a very compact description in terms of the normalized charges, currents and frequency. It was shown that new effects imposed by advanced technology could be simply considered as a model generalization, still keeping a minimum set of model parameters.

ANNEX A

A derivation of the pinch-off voltage was already presented in [7]. However, this approach was based on the current and source transconductance expressions, which were based on 'hidden' assumptions. In this section, we demonstrate how the definition of the pinch-off voltage is a direct consequence of the inversion charge linearization as derived from the charge sheet approximation.
Noting x and y the coordinates along and perpendicular to the channel, we show that $\frac{d\psi(x,y)}{dx}$ and $V_{CH}(x,y)$ are assumed independent of y when deriving the well-known channel current relations A3 and A4.
Considering that the flow of electrons is laminar, the channel current at x and between a slice y, $y+dy$ can be expressed as:

$$dI(x,y) = -(W \cdot dy) \cdot \mu \cdot q(x,y) \cdot \frac{dV_{CH}(x,y)}{dx} \qquad \text{(A1)}$$

or equivalently (A2):

$$dI(x,y) = W \cdot dy \cdot \mu \cdot \left(U_T \cdot \frac{dq(x,y)}{dx} - q(x,y) \cdot \frac{d\psi(x,y)}{dx} \right)$$

where $q(x,y)$ is the local inversion charge density. In order to obtain the relations (A3) and (A4), it is necessary to integrate (A1) and (A2) along y *assuming* that $\frac{d\psi(x,y)}{dx}$ and $V_{CH}(x,y)$ are independent of y over the inversion region, i.e. $\frac{d\psi(x,y)}{dx} \approx \frac{d\psi_S(x)}{dx}$:

$$I(x) = -W \cdot \mu \cdot Q(x) \cdot \frac{dV_{CH}(x)}{dx} \qquad \text{(A3)}$$

$$I(x) = W \cdot \mu \cdot \left(U_T \cdot \frac{dQ(x)}{dx} - Q(x) \cdot \frac{d\psi_S(x)}{dx} \right) \qquad \text{(A4)}$$

where $Q(x)$ represents the inversion charge integrated over the inversion region at the x coordinate in the channel:

$$Q(x) = \int_{inv.region} q(x,y) \cdot dy \qquad \text{(A5)}$$

Furthermore, from fundamental semiconductor relations, the inversion charge density $q(x,y)$ can be expressed as:

$$q(x,y) = q_0 \cdot \exp\left(\frac{\psi(x,y) - V_{CH}(x,y)}{U_T} \right) \qquad \text{(A6)}$$

where q_0 is the inversion charge density at equilibrium.
Relation (A5) becomes:

$$Q(x) = q_0 \cdot \int_{inv.region} \exp\left(\frac{\psi(x,y) - V_{CH}(x)}{U_T} \right) \cdot dy \qquad \text{(A7)}$$

Derivating relation (A7) versus x and recalling that $\frac{d\psi(x,y)}{dx}$, $V_{CH}(x,y)$ are independent of y, we obtain:

$$\frac{dQ(x)}{dx} = \frac{1}{U_T} \cdot Q(x) \cdot \left(\frac{d\psi_S(x)}{dx} - \frac{dV_{CH}(x)}{dx} \right) \qquad \text{A(8)}$$

Introducing the normalized quantities and inserting relation (1) in (A8) leads to the differential equation:

$$\frac{dq_i'(x)}{dx} = q_i'(x) \cdot \left(\frac{dq_i'(x)}{dx} - \frac{dv_{ch}(x)}{dx} \right) \qquad \text{A(9)}$$

whose solution is given by :

$$\ln\left(-q_I'\right) - 2 \cdot q_I' = v_P - v_{ch} \qquad \text{(A10)}$$

where v_P represents the constant of integration called the pinch-off voltage and that can be interpreted as the channel voltage that cancel the inversion charge density extrapolated from strong inversion (i.e. neglecting the logarithmic term).

ANNEX B

The forward (reverse) current can also be written as:

$$i_{f,r} = \int_0^{q'_{s,d}} \left(2 \cdot q_i' \cdot dq_i' - dq_i' \right) \qquad \text{(B1)}$$

Differentiating relation A10 with respect to v_{ch}, we have:

$$dq_i' = 2 \cdot q_i' \cdot dq_i' - q_i' \cdot dv_{ch} \qquad \text{(B2)}$$

Replacing equation (B2) in (B1) and noting that $q_i' \approx 0$ for $v_{ch} = \infty$, in relation (9), we obtain:

$$i_{f,r} = \int_{v_{s,d}}^{\infty} - q_i^{'} \cdot dv_{ch} \qquad \text{(B3)}$$

Relation (B3) represents the original definition of the forward and reverse normalized currents as proposed in [1]. As a consequence, both definitions, relations (7) and (B3), are entirely equivalent. This implies that the forward (reverse) current is depicted by the surface from v_s (v_d) to infinity in the $q_i^{'}(v_{ch})$ representation shown on fig. 2 with the normalized channel current marked as the dashed area.

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