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# Scalable GM / I Based MOSFET Model

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## 1. Introduction

The continuing decrease of supply voltage to reduce power consumption of digital circuits strongly affects the design of the analog part of mixed analog/digital ICs. As a consequence, MOS transistors in analog circuits often operate in moderate inversion. Compact MOSFET models for deep sub-micron technologies therefore need to describe the full operating range from weak to strong inversion in a physical and continuous way. Scalability over the full range of available geometries is required without resorting to a large number of parameters or parameter "binning".

This paper describes a scalable and unified MOS transistor model based on the normalized transconductance-to-current characteristic, $g_{ms} \cdot V_t / I_D$, used in the 'EKV' model [1][2]. This approach describes the transistor behavior at different current levels from weak to moderate and strong inversion. The new features with respect to previous model versions are addressed here, in particular, a new universal mobility degradation model due to vertical field, reverse short-channel effect (RSCE), drain-induced barrier lowering (DIBL), and bias-dependent series resistance. The large-signal static model as well as the dynamic charges and thermal noise models are derived in a unified way and are valid in all modes of operation. The compact scalable model is a strong candidate for application to deep sub-micron technologies. It is efficient for parameter extraction and circuit simulation and, due to its continuity, alleviates convergence problems. A single set of as few as 25 process-related, intrinsic and extrinsic DC model parameters can be extracted for all geometries including short and narrow devices in a simple and straightforward sequence.

The drain current is derived under typical assumptions for charge-sheet models and includes drift and diffusion components [3] as well as major physical effects in a single equation:

$$I_D = I_S \cdot (i_f - i_r) = \frac{2 \cdot n \cdot \mu_s \cdot C_{ox}' \cdot W_{eff} \cdot V_t^2}{L_{eff} - \Delta L + \delta_0 \mu_s V_{ds}' / v_{sat}} \cdot (i_f - i_r) \qquad (1)$$

where $\mu_s$ is the surface mobility including vertical field dependence, $C_{ox}'$ is the gate oxide capacitance, $V_t$ is the thermal voltage, $I_S$ is the specific current related to aspect ratio, $i_f$ and $i_r$ are symmetrical forward and reverse normalized currents [1], depending on $V_P - V_S$ and $V_P - V_D$, respectively, and $n$ is the slope factor depending on $V_P$. The concept of the pinch-off voltage $V_P$ [1], which is essentially a function of the gate voltage, is used to account for effects of doping concentration, such as threshold voltage, body effect, charge-sharing for short- and narrow-channel effects, RSCE, DIBL and non-uniform doping [4][5]. $V_P$ represents the channel voltage at a given gate voltage for which the inversion charge density $Q'_I$ in the channel becomes negligible with respect to the depletion charge density $Q'_B$. $\Delta L$ accounts for channel length modulation (CLM). Velocity saturation is handled similarly to [6]. The model is formulated symmetrically in terms of $V_S$ and $V_D$ and has a hierarchical structure. It also includes temperature effects and substrate current [7].

## 2. Long-Channel Model

A means of integration for the drain current is provided by the normalized conductance [1] $G(i) = g_{ms} V_t / I_D$ where $g_{ms} \equiv -\partial I_D / \partial V_S \big|_{V_G, V_D}$. A suitable function is needed to describe the behavior of $G(i)$ [1][8], with correct asymptotes, which are 1 in weak inversion and $1/\sqrt{i}$ in strong inversion, respectively. A simple and accurate analytical expression has recently been proposed [9]:

$$G(i) = \frac{g_{ms} V_t}{I_D} = \frac{di/dv}{i} = \frac{2}{1 + \sqrt{1 + 4i}} \qquad (2)$$

Both (2) and the $g_{ms} \cdot V_t / I_D$ characteristic, calculated from the numerical solution of Poisson and Gauss equations under uniform doping and long-channel assumptions, are plotted in Fig. 1a , with respect to the normalized current $i_f \equiv I_D / I_S$ in saturation, and are found to match very well. The above numerical characteristic varies negligibly over a large range of doping levels and oxide thicknesses. The measured results from long-channel devices of three CMOS technologies, with minimum feature sizes ranging from 1 $\mu m$ to 0.5 $\mu m$ , are shown in Fig. 1b to match (2) very well from weak to strong inversion. For scaled deep sub-micron technologies, this characteristic is expected to remain sufficiently

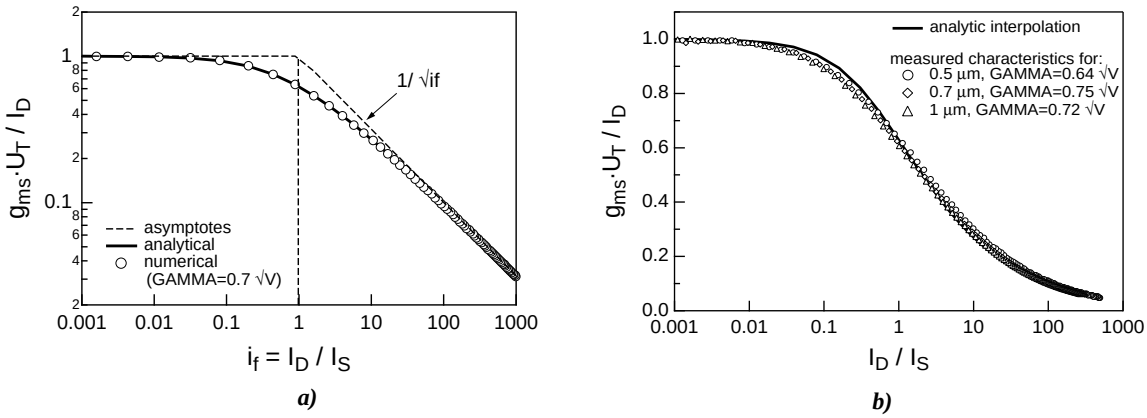


**Fig. 1:** *The normalized $g_{ms}/I_D$ characteristics versus normalized current a) computed by numerically solving the Poisson equation for a long-channel device and interpolated by (2). b) measured on long n-channel devices for three different CMOS processes and analytical interpolation (2).*

unchanged and thus remain valid as a basis of this modeling approach. Integrating (2) yields the relation between normalized current $i$ and voltage $v$:

$$v = \sqrt{1+4i} - 1 + \ln(\sqrt{1/4+i} - 1/2) \qquad (3)$$

which unfortunately cannot be inverted analytically as would be required for the computation of $i_f$ and $i_r$ in (1). However a simple Newton-Raphson scheme allows an efficient inversion without loss of accuracy, such that the full drain current can now be expressed as a function of the terminal voltages.

If (2) is combined with the relationship between channel conductance and inversion charge density, $g_{mx}(V) = -\mu(x) \cdot Q'_I(V)$, where $V$ is the channel potential at a given point $x$ in the channel, the inversion charge density can be expressed as a function of the normalized current:

$$-Q_I'(x) = 2 \cdot n \cdot V_t \cdot C_{ox}' \cdot (\sqrt{1/4+i} - 1/2) \quad (4)$$

Integrating (4) allows us to formulate a consistent quasi-static charge/capacitance model. This approach has been used in the EKV model since the publication of [9], and has also been published in [10] recently. Thermal noise is simply proportional to the total inversion charge $Q_I$ [1].

Using these derivations, the mobility reduction due to vertical effective field can be elegantly accounted for. A general expression for the localized mobility dependence on vertical field is given by:

$$\mu_s(x) = \mu_0 \Big/ \left[1 + \sum_k [E_{eff}(x)/E_k]^k\right] \qquad (5)$$

where $k$ is the order of effective field taken into account, and $E_k$ is the $k^{th}$-order parameter. The effective field dependence on inversion and depletion charge densities is commonly described by $E_{eff}(x) = \left|Q_B'(x) + \eta \cdot Q_I'(x)\right| / \varepsilon_0 \varepsilon_{si}$, where $\eta \approx 0.5$ for nMOS and $\eta \approx 0.3$ for pMOS [11] at room temperature. To account for mobility reduction globally, (5) is integrated along the channel:

$$\mu_s = \frac{1}{L}\left[\int_0^L \frac{1}{\mu_s(x)}dx\right]^{-1} \qquad (6)$$

$$= \frac{\mu_0}{L}\left[\int_0^L \left(1 + \sum_k \left[\frac{\left|Q_B'(x) + \eta \cdot Q_I'(x)\right|}{\varepsilon_0 \varepsilon_{si} E_k}\right]^k\right)dx\right]^{-1}$$

$$= \frac{\mu_0}{i_f - i_r}\left[\int_{if}^{ir} \left(1 + \sum_k \left[\frac{\left|Q_B'(i) + \eta \cdot Q_I'(i)\right|}{\varepsilon_0 \varepsilon_{si} E_k}\right]^k\right)di\right]^{-1}$$

Using the expressions for the charge densities $Q_I'(i)$ and $Q_B'(i)$ [1], this form can be easily integrated for any order of $k \geq 1$. To the authors' knowledge, this is the first time that such formulation was carried out. Integrating the 1st-order term yields

$$\mu_s = \mu_0 \Big/ \left[1 + \frac{\left|Q_B + \eta \cdot Q_I\right|}{\varepsilon_0 \varepsilon_{si} E_0 WL}\right] \qquad (7)$$

For the purposes of this compact model, the 2nd-order model has been formulated and used. Unlike in other MOS models, the 2nd-order term used here represents the fully integrated form of the local effective field dependence.

Note that the above formulation also implies a dependence with the lateral field. The correlation between mobility reduction due to vertical field and velocity saturation [7] has to be carefully considered when formulating the global model (1) including both these effects.

The long-channel model described so far is valid and continuous among all operating regions, for static, dynamic and noise models. It needs now to be suitably complemented for short-channel effects.

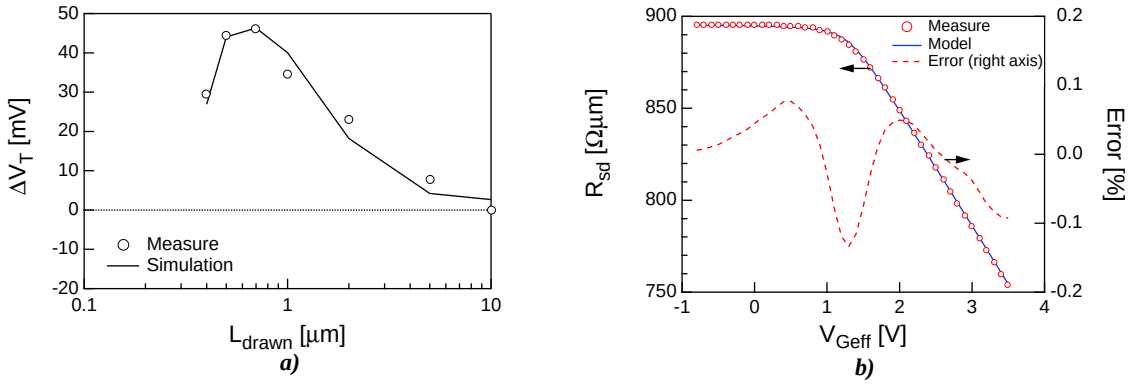


**Fig. 2:** *a) Variation of the threshold voltage with channel length due to RSCE for n-channel devices of a 0.5µm standard CMOS process; b) gate bias dependence of series resistance [12] of a device from a 0.35µm CMOS process.*

### 3. Short-Channel Model

Two short-channel effects, RSCE and DIBL, are included in the pinch-off voltage $V_P$ [1] in addition to the charge-sharing concept to extend the model's range of applicability. Various models for RSCE have been proposed, and can be summarized as a correction either of substrate doping [12], or threshold voltage [13]. Both use CPU-expensive exponential terms, which also may lead to convergence problems during parameter extraction. A new simple yet accurate model is derived from [13], without the use of exponentials:

$$\Delta V_{fb_{RSCE}} = \frac{2 \cdot Q_0}{C_{ox}'} \cdot \left[1 + \frac{1}{2} \cdot \left(\xi + \sqrt{\xi^2 + 4 \cdot \varepsilon_1^2}\right)\right]^{-2} \quad (8)$$

where $\xi = C_1 \cdot (10 \cdot L_{eff}/L_k - 1)$, $\varepsilon_1$ and $C_1$ are constants. The parameters used are the peak charge density at the source/drain ends $Q_0$ and the characteristic length of charge distribution $L_k$. The current model for DIBL is a simplified form of [6]:

$$\Delta V_{fb_{DIBL}} = \sigma_0 \cdot (V_D - V_S) \cdot \left[\frac{\varepsilon_0 \varepsilon_{si}}{C_{ox}' \cdot L_{eff}}\right]^m \quad (9)$$

where $\sigma_0$ is the DIBL parameter and $m = 2$; it may be refined as discussed in [14]. The global threshold voltage is a superposition of the charge-sharing, RSCE and DIBL effects with geometry and bias [7], which can be strongly process-dependent. The threshold voltage variation as a function of drawn gate length is shown in Fig. 2a in the case of a 0.5 µm process displaying RSCE. Parameter extraction can follow the method of $V_P$ vs. $V_G$ measurement [4][5][15] at constant current.

Series resistance is a critical parameter for process engineering, device modeling and circuit design. Present CMOS technologies commonly use LDD structures with gate bias dependent resistivity. Although bias dependence of series resistance may decrease for very advanced technologies [16], even small variations may have a considerable effect on extracted channel length and series resistance. The existing models [12][17] typically use exponentials. The simple model for the bias dependent series resistance proposed in this paper avoids the use of exponentials without noticeable loss of accuracy,

$$R_{sd} = R_{sh0} \cdot \left[1 - \left(\frac{1}{2} \cdot r + \sqrt{r^2 + 4 \cdot \varepsilon_2^2}\right)\right] \quad (10)$$

where $r = S_{Vk} \cdot (V_{Geff}/V_k - 1)$, $V_{Geff} = V_G - V_{TO}$ is the effective gate voltage, and $\varepsilon_2$ is a constant. The parameters are sheet resistance $R_{sh0}$, characteristic voltage $V_k$ and coefficient $S_{Vk}$. A comparison with the measured data [12] for a 0.35 µm process in Fig. 2b shows good agreement.

Note that if series resistance is to be explicitly accounted for in drain current and conductances, the following relations are used as discussed in [18]:

$$\frac{I_D}{I_{D0}} = \frac{g_m}{g_{m0}} = \frac{g_{ms}}{g_{ms0}} = \frac{g_d}{g_{d0}} \cong \frac{1}{1 + g_{ms0}R_S + g_{d0}R_D} \quad (11)$$

where the subscript '0' denotes current or conductances calculated without series resistance.

### 4. Results and Discussion

The new scalable model has been implemented as a compact model in the Eldo™ circuit simulator. The scaling performance with channel length is illustrated for a 0.5 µm process in Fig. 2a, where the simulated equivalent threshold voltage is shown to match the experimental data with a small maximum error of 6 mV, for drawn channel lengths ranging from 0.4 µm to 10 µm. For the same technology, the measured and simulated $I_D$ vs. $V_G$ characteristics in saturation for different $V_S$ are compared in Fig. 3 for three different channel lengths. The fit is excellent for all channel lengths from weak to strong inversion. Fig. 3 also presents the output characteris-

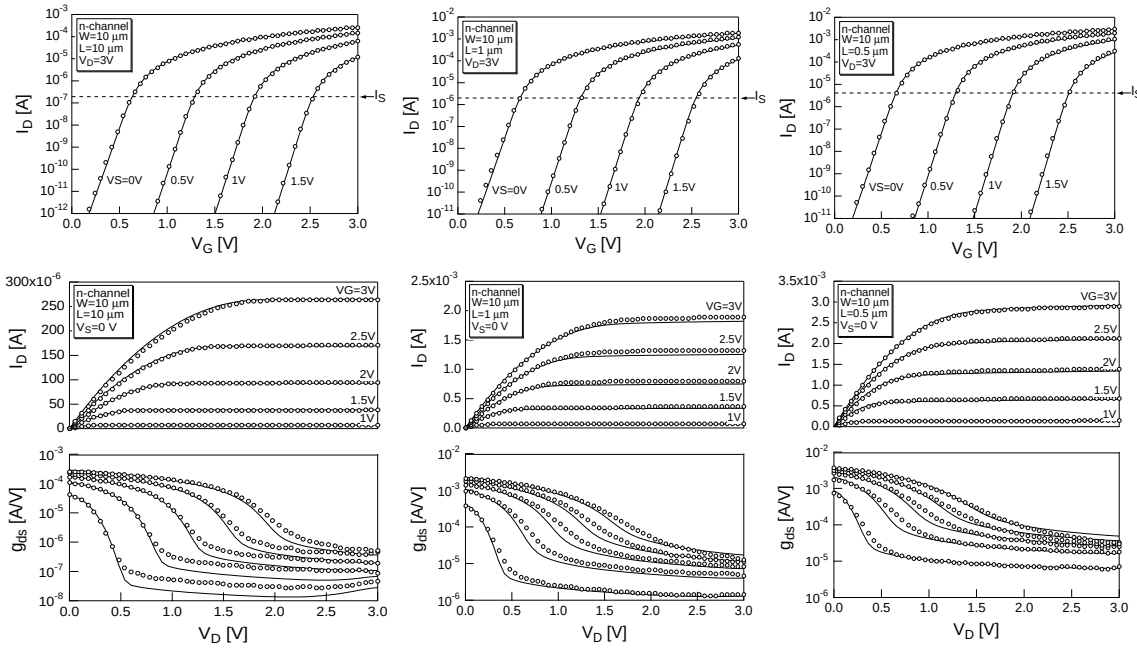


**Fig. 3:** *Comparison of measured (o) and simulated (-) characteristics $I_D$ vs. $V_G$ at different $V_S$ ; $I_D$ and $g_{ds}$ vs. $V_D$ at different $V_G$ . for n-channel devices of a 0.5 µm standard CMOS process, for long (L=10 µm ), intermediate (L=1 µm ) and short (L=0.5 µm ) drawn channel lengths respectively.*

tics $I_D$ and $g_{ds}$ vs. $V_D$ at different $V_G$. The output conductance $g_{ds}$ is continuous and well modeled for all geometries both in conduction and saturation. These figures demonstrate the continuity among all operating regimes and the model's scalability, since a single parameter set has been used for all devices.

## 5. Conclusions

In summary, a unified, physical and scalable compact MOS transistor model based on a simple but accurate interpolation of the normalized $g_{ms}/I_D$ characteristic has been presented. The model is symmetric and has a hierarchical structure. The long-channel static model, including mobility effects, the dynamic charge model as well as thermal noise model are derived in a unified and continuous way, valid from weak to strong inversion and from linear to saturation regions. Short-channel effects, such as RSCE and bias dependent series resistance, are included in the model to achieve scalability, and are formulated in an adequate and efficient way for parameter extraction and circuit simulation. Experimental results demonstrate the model's scalability for a 0.5 $\mu m$ CMOS process using a single set of no more than 25 intrinsic and extrinsic DC parameters. The model is well suited for deep sub-micron analog and mixed-mode IC design.


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