ACCURATE MOS MODELLING FOR ANALOG CIRCUIT SIMULATION USING THE EKV MODEL

Matthias Bucher, Christophe Lallement, Christian Enz, François Krummenacher

Swiss Federal Institute of Technology (EPFL), Electronics Laboratory, ELB-Ecublens, CH-1015 Lausanne, Switzerland

Phone: +41 21 693 39 79, Fax: +41 21 693 36 40, E-mail: enz@leg.de.epfl.ch, bucher@leg.de.epfl.ch

ABSTRACT

Effective, manufacture-oriented design and simulation of high-performance analog and mixed-mode integrated circuits and systems is known to critically depend on the quality of extracted device parameters as well as the simulation model being used. This has gained increased relevance for low-voltage low-current designs, either in bulk CMOS or emerging SOI technologies. The EKV model is introduced within a complete, statistically efficient and simple characterisation methodology. Valuable insight into the behavior of transistors in strong, moderate and weak inversion is gained, which also allows for increased design creativity. Measured results from a submicron bulk CMOS and a fully depleted SOI process illustrate the accuracy of the EKV model and the associated parameter extraction under several geometries and regions of device operation.

1. INTRODUCTION

The requirements for good MOS analog simulation models such as accuracy and continuity of the large- and small-signal characteristics are well established [1][2]. The EKV MOST model [3][4] has been developed keeping in mind computational efficiency, ease of parameter extraction and the designer's needs for insight into the device behavior. Effects relevant for precise analog low-current (LC) and low-voltage (LV) circuit design have been included in the model.

An efficient and simple characterisation method is formulated to obtain complete geometry independent parameter sets. Threshold voltage and channel doping characterisation is achieved through a single measurement of the pinch-off voltage characteristic at a constant current bias in moderate inversion [5].

Table I: *Main EKV intrinsic model parameters for first and second order effects and default values and units where applicable.*

Name	Description	Default Values, Units			
COX	Gate oxide capacitance	-	F/μm^2	-	F/m^2
VTO	Nominal threshold voltage	0.5	V	0.5	V
GAMMA	Body effect factor	1	V$^{1/2}$	1	V$^{1/2}$
PHI	Bulk Fermi potential (2x)	0.7	V	0.7	V
KP	Transconductance parameter	50e-6	A/V^2	50e-6	A/V^2
THETA	Mobility reduction coefficient	0	1/V	0	1/V
UCRIT	Longitudinal critical field	2	V/μm	2e6	V/m
XJ	Source & drain junction depth	0.1	μm	1e-7	m
DL	Channel length correction	0	μm	0	m
DW	Channel width correction	0	μm	0	m
LAMBDA	Depletion length coefficient	0.5	-	0.5	-
LETA	Short channel effect coefficient	0.1	-	0.1	-
WETA	Narrow width effect coefficient	0.25	-	0.25	-

Table II: *Summary of basic DC simulation model equations.*

Description	Equation
Pinch-off voltage	$V_P = V_G' - \mathrm{PHI} - \gamma' \cdot \left(\sqrt{V_G' + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2}\right)$ $V_G' = V_G - \mathrm{VTO} + \mathrm{PHI} + \mathrm{GAMMA} \cdot \sqrt{\mathrm{PHI}}$
Slope factor	$n = 1 + \frac{\mathrm{GAMMA}}{\sqrt{V_P + \mathrm{PHI}}}$
Transconductance, mobility reduction	$\beta = \mathrm{KP} \cdot \frac{W_{eff}}{L_{eq}} \cdot \frac{1}{1 + \mathrm{THETA} \cdot V_P}$
Effective length & width	$L_{eff} = L + \mathrm{DL}$, $W_{eff} = W + \mathrm{DW}$
Channel length modulation & velocity saturation	$L_{eq} = L_{eff} - \Delta L + \frac{V_{DS}'}{\mathrm{UCRIT}}$ $\Delta L = \mathrm{LAMBDA} \cdot L_C \cdot \ln\left(1 + \frac{V_R}{L_C \cdot \mathrm{UCRIT}}\right)$ $L_C = \sqrt{\frac{\varepsilon_0 \varepsilon_{si}}{\mathrm{COX}}} \cdot \mathrm{XJ}$ $V_D - V_S \le V_{DS}' \le V_{DSS}$ $0 \le V_R < V_D - V_S - V_{DSS}'$ *V_{DS}' and V_R are continuous functions, V_{DSS} and V_{DSS}' depend on bias, L_{eff}, UCRIT and LAMBDA*
Short & narrow channel effects	$\gamma' = \mathrm{GAMMA} - \frac{\varepsilon_0 \varepsilon_{si}}{\mathrm{COX}} \cdot \left[\frac{\mathrm{LETA}}{L + \mathrm{DL}} \cdot \sqrt{V_D + \mathrm{PHI}} + \left(\frac{\mathrm{LETA}}{L + \mathrm{DL}} - \frac{3 \cdot \mathrm{WETA}}{W + \mathrm{DW}}\right) \cdot \sqrt{V_S + \mathrm{PHI}}\right]$
Drain current and Specific current	$I_D = I_F - I_R$ $I_{F(R)} = \begin{cases} I_S \cdot \exp\left[(V_P - V_{S(D)})/U_t\right] & \text{(WI)} \\ I_S \cdot \left[(V_P - V_{S(D)})/2U_t\right]^2 & \text{(SI)} \end{cases}$ $I_S = 2 \cdot n \cdot \beta \cdot U_t^2 \quad U_t \equiv k \cdot T/q$

2. SIMULATION MODEL

Continuity of the large- and small-signal characteristics from weak (WI) through moderate (MI) to strong inversion (SI) and from conduction to saturation is one of the main features of the EKV MOST model. A set of 13 intrinsic parameters, shown in Table I, is used for first- and second-order effects. A summary of the relevant simulation model equations is presented in Table II.

In the EKV model, the gate, source and drain voltages, V_G, V_S and V_D, are all referred to the substrate to preserve the intrinsic symmetry of the MOS transistor. The threshold voltage VTO is defined as the gate voltage for which the inversion charge forming the channel is zero at equilibrium $V_D = V_S = 0$. The pinch-off volt-

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age V_P, depending mainly on the gate voltage V_G and the parameters VTO, GAMMA and PHI, corresponds to the value of the 'channel potential' for which the inversion charge becomes zero in a non-equilibrium state. The weak inversion slope factor n is a function of V_P and depends on the same parameters.

The drain current is expressed as the difference of the forward and reverse currents I_F and I_R, depending respectively on V_P -V_S and V_P -V_D. Both components are interpolated in a continuous manner from weak to strong inversion with exponential and quadratic asymptotic behavior respectively, using the specific current as a normalization factor $I_S \equiv 2n\beta U_t^2$. For design purposes, the function $I_{F(R)} \cong I_S \cdot [\ln(1 + \exp[(V_P - V_{S(D)})/2U_t])]^2$ is used to obtain simple expressions for drain current, transconductances and intrinsic capacitances in different operating regions [3][4]. For circuit simulation, the interpolation function takes a precise form resulting from the numerical resolution of the surface potential for long channel and uniformly doped substrate approximations.

Mobility reduction due to the vertical field, channel length modulation and velocity saturation are included in the transconductance factor β. Careful modelling ensures the first-order derivatives to be continuous at the transitions between operation regions over the entire geometrical range. Short- and narrow-channel effects are accounted for in the modified body effect factor γ', derived from the charge sharing approach, the effect of which is equivalent to drain induced barrier lowering.

The simulation model is completed with continuous expressions for the quasi-static capacitances, the first-order non-quasi-static transadmittances, temperature behavior and thermal noise, valid for all regions of device operation. Substrate current effects, requiring three additional parameters, are also included in the model.

3. DC PARAMETER EXTRACTION

The extraction of the threshold voltage and channel doping related parameters is of particular importance. The simple scheme of Fig. 1 is used to measure the pinch-off vs. gate voltage characteristic V_P *vs.* V_G, performed at a constant current bias in MI [5]. For V_S to be equal to V_P, the bias current I_B has to be set to half the specific current I_S, making the transistor operate in MI, where velocity saturation effects are negligible. I_S depends on the device size and is determined from the strong inversion slope of $\sqrt{I_D}$ *vs.* V_S. VTO is determined as the particular value of V_G corresponding to $V_P = 0$, and GAMMA and PHI are extracted by fitting the measured V_P *vs.* V_G characteristic of a long and large device. Leaving the latter as two independent parameters allows to account for non-uniform doping to a certain degree [6], resulting in parameter values slightly smaller than those obtained for uniform doping. The robustness of the method is illustrated by the small sensitivity of the extracted parameters with respect to the bias current I_B, which is less than 5% for a one octave change of the bias current.

The pinch-off voltage extraction method has several advantages compared with other constant current V_{th} methods: the bias current is given a precise meaning and VTO is extracted with a unique value without extrapolation. The method is furthermore simple, fast and efficient. GAMMA and PHI are obtained from the same single measurement, in a much simpler way than with classical techniques [7].

Maintaining VTO from the wide and large device, the V_P *vs.* V_G characteristics for short and narrow devices (Fig. 1) are used to obtain the respective parameters LETA and WETA. This supposes the channel length and width corrections DL and DW to be previously determined, using methods that simultaneously yield the series resistances RS+RD [7].

Table III: *Summarized extraction procedure for the EKV model, featuring device sizes, measured characteristics, conditions (SI: strong, MI: moderate, WI: weak inversion, co.: conduction, sat.: saturation) and extracted parameters.*

Device sizes	Characteristics	Conditions	Parameters
matrix W/L	R *vs.* L_{eff} $1/R$ *vs.* W_{eff}	SI co.	DL,RS+RD DW
wide/long	I_D *vs.* V_S V_P *vs.* V_G I_D *vs.* V_G	SI sat. MI sat. SI sat.@V_S	I_S VTO,GAMMA,PHI KP,THETA
wide/short	I_D *vs.* V_S V_P *vs.* V_G I_D *vs.* V_D	SI sat. MI sat. SI co.-sat.	I_S LETA UCRIT,LAMBDA
narrow/long	I_D *vs.* V_S V_P *vs.* V_G	SI sat. MI sat.	I_S WETA

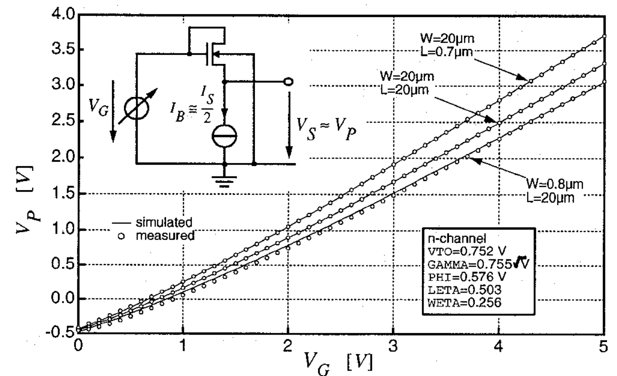
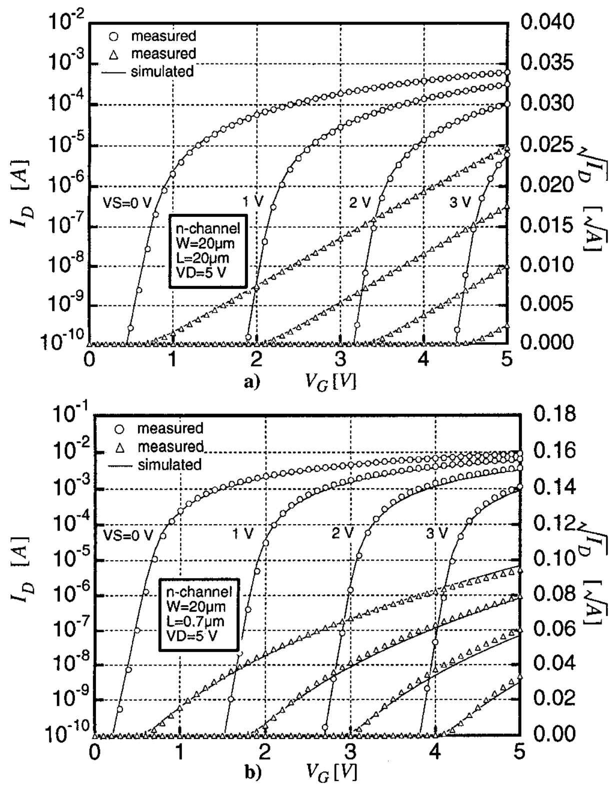


Fig. 1: *Circuit for V_P vs. V_G characteristic measurement and parameter extraction for three n-channel devices of a 0.7µm CMOS technology.*

Table III summarizes the complete extraction method to obtain a single geometry independent parameter set for a given technology, for either n- or p-channel. This method has been automatized in commercial characterisation tools. Nonlinear optimization in conjunction with full model equations in adequate operation ranges allows to achieve consistency with the model as well as to maintain flexibility. To increase the efficiency of the optimisation steps, reduced data sets and simplified model expressions can be used, especially for the V_P *vs.* V_G characteristic. To refine the accuracy of the extraction, fine tuning can be carried out, optionally using intermediate or minimum device sizes.

4. RESULTS AND DISCUSSION

Results of the complete extraction methodology are presented for submicron bulk and fully depleted silicon-on-insulator (FD SOI) technologies. All characteristics shown for the respective technologies have been obtained using a single parameter set. The inset in Fig. 1 specifies the parameter values obtained from n-channel bulk devices. Measured and simulated I_D *vs.* V_G currents are shown in Fig. 2 for a long and a short device. For the short device, the gate



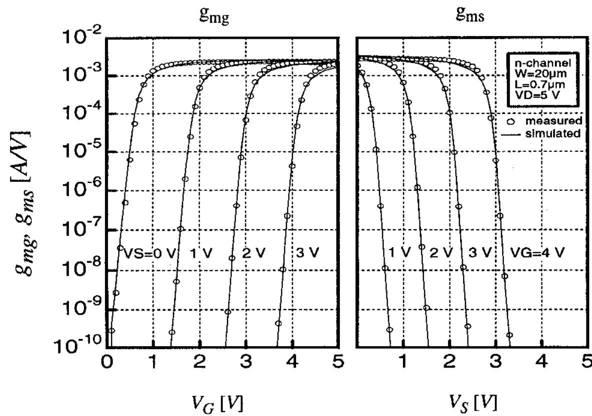


Fig. 2: *$log(I_D)$ & $\sqrt{I_D}$ vs. V_G characteristics of a) a long, b) a short n-channel device.*

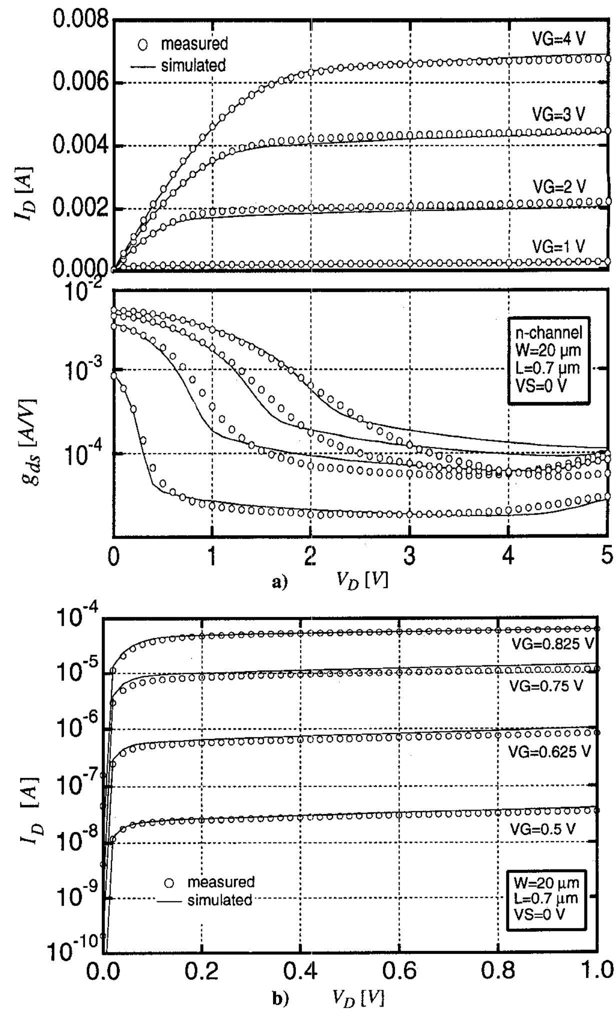


Fig. 4: *Output characteristics a) I_D and g_{ds} vs. V_D in strong inversion, b) $log(I_D)$ vs. V_D in weak inversion, of a short n-channel device.*

Fig. 3: *Gate and source transconductances g_{mg} vs. V_G and g_{ms} vs. V_S of a short n-channel device.*

and source transconductances are presented in Fig. 3, and output characteristics in Fig. 4. The transconductance to current ratio is shown in Fig. 5 for a long and a short device. Note the continuity of the first-order derivative of the model, particularly in the MI region, and the accuracy in subthreshold operation. As expected for FD SOI devices, an almost ideal subthreshold slope $n \cong 1.02$ is found (Fig. 6). The operating voltages, here referred to the back gate, need to be reduced to avoid kink effects [8]. As for the bulk devices, the model accurately predicts SOI behavior in all operating regions (Fig. 7).

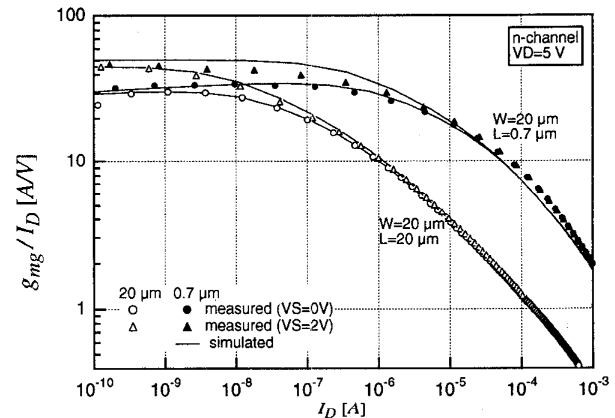


Fig. 5: *Transconductance to current ratio g_{mg}/I_D vs. I_D on a logarithmic scale of a long and a short n-channel device.*

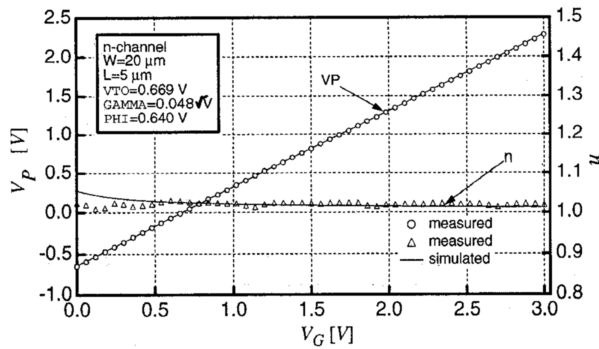


Fig. 6: *V_P vs. V_G and derived slope factor n vs. V_G characteristics for an n-channel FD SOI device.*

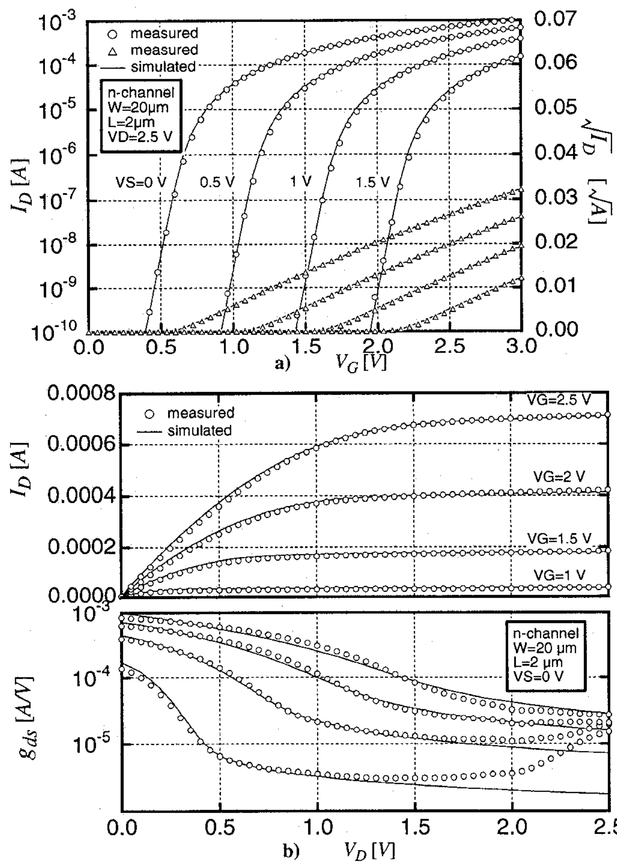


Fig. 7: *a) log(I_D) and $\sqrt{I_D}$ vs. V_G, b) I_D and g_{ds} vs. V_D characteristics for a wide and short n-channel FD SOI device.*

These results demonstrate the flexibility of the extraction method based on the V_P vs. V_G characteristic. Excellent match between measured and simulated characteristics can be observed over a wide bias range. Geometrical behavior is the result of a reasonable compromise between accuracy and simplicity. In practice, modelling of deep-submicron devices is found to be promising, however requiring more than a a single parameter set to cover the whole geometric range. Further refinements are under investigation in this respect as well as for non-uniform doping [6].

In circuit simulation practice, good convergence properties and computational efficiency have been observed for numerous circuits in analog and mixed-mode applications. CPU time comparisons with Spice level 3 model in several commercial simulators on both Sun and PC platforms give an advantage for EKV generally of 15% for DC analysis and better or comparable results for transient analysis. Convergence has consistently been observed to be better with the EKV model.

5. CONCLUSIONS

The EKV MOST model responds to the needs of low power low voltage circuit designers, giving insight into device behavior related with the model parameters, as well as allowing for a creative use of their simulation tool to investigate novel designs. Measured and simulated characteristics presented are in good accordance over large bias ranges. A simple and efficient parameter extraction method has been presented, based on the measurement of the pinch-off voltage vs. gate voltage characteristic in moderate inversion at constant current. An automated parameter extraction has been implemented in commercial extraction tools. High accuracy for low-current and low-voltage design and computational advantages are achieved through the use of the EKV model, shown to suit both submicron bulk and fully depleted SOI technologies.

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REFERENCES

[1] Y. Tsividis and K. Suyama, "MOSFET Modelling for Analog Circuit CAD: Problems and Prospects", JSSC, Vol. 29, No. 3, pp. 210-216, 1994.

[2] G. A. S. Machado and C. Toumazou, "Systematic Design-Oriented Characterisation of MOS Devices and Circuit Building Blocks in Engineering Education", Proc. of the IX Congress of the Brasilian Society of Microelectronics, pp. 243-257, 1994.

[3] C. C. Enz, F. Krummenacher and E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications", Special issue of the Analog Integrated Circuits and Systems Processing Journal on Low-Voltage and Low-Power Circuits, vol. 8, pp. 83-114, 1995.

[4] G. A. S. Machado, C. C. Enz and M. Bucher, "Estimating key parameters in the EKV MOST model for analogue design and simulation", Proc. of the IEEE Int. Symposium on Circuits and Systems, pp. 1588-1591, 1995.

[5] M. Bucher, C. Lallement, C. C. Enz: "An efficient Parameter extraction Methodology for the EKV MOST Model", IEEE Int. Conf. on Microelectronic Test Structures, Trento, Italy, March 26-28, 1996

[6] C. Lallement, C. C. Enz and M. Bucher, "Simple Solutions for Modelling the Non-Uniform Substrate Doping", Proc. of the IEEE Int. Symposium on Circuits and Systems, May, 1996.

[7] N. D. Arora, "Mosfets for VLSI Circuit Simulation, Theory and Practice", Chap. 9, Computational Microelectronics, Ed. S. Selberherr, 1993.

[8] J.-P. Colinge, "Silicon-On-Insulator Technology", Material to VLSI, Kluwer Academic Publishers, 1991.