A High Density Integrated Test Matrix of MOS Transistors for Matching Study

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Abstract – This paper describes a test structure for the characterization of MOS transistors matching. It integrates (on 1.5 mm square) a matrix of 480 transistors to be tested, together with the analog switches and shift registers necessary for an individual access to these transistors. This circuit has been integrated on an experimental fully depleted Silicon On Insulator (SOI) process [1] as well as on a standard bulk process. Results for the SOI matching properties are discussed.

MOTIVATION

Characterizing local matching properties of a CMOS process involves the measurement of a large number of samples. The cost and complexity of the measurement strongly depend on the test structure and its number of pads. The simplest structure, made of matched pairs having a pad per terminal, consumes a huge silicon area and requires on wafer testing with an automated chuck [e.g. 2]. The pad number is frequently decreased by connecting the transistors in a matrix where the devices under test (DUTs) are selected with a gate row and a drain column [e.g. 3]. As is, this structure however needs a low leakage switch matrix in order to multiplex the outputs of the chip to the DC analyzer. Moreover, the DUTs number is still limited by the number of available channels in the switch matrix.

Addressable matrices of transistors which directly integrate the multiplexing circuit on silicon allow to test an arbitrary number of DUTs with a fixed number of pads. Various circuits have been previously presented [4][5]. However, most of them present limitations : some are made of diode connected transistors, others need an individual switch for each DUT. Moreover, the integrated multiplexing circuit generally limits the current level of measurement and requires a dedicated extraction method of the transistor parameters.

In [6] is proposed a structure which does not need individual switches for each DUT but which remains limited to the measurement at low current levels. While similar to the latter, the presented structure however compensates the resistance of the switches and which provides the access to the 4 terminals of the transistor. Therefore, all the characteristics of the tested transistors can be measured over a wide current range, allowing various extraction methods.

This structure has been used to characterize local matching properties of a fully depleted SOI process and has also been successfully tested with a standard bulk process.

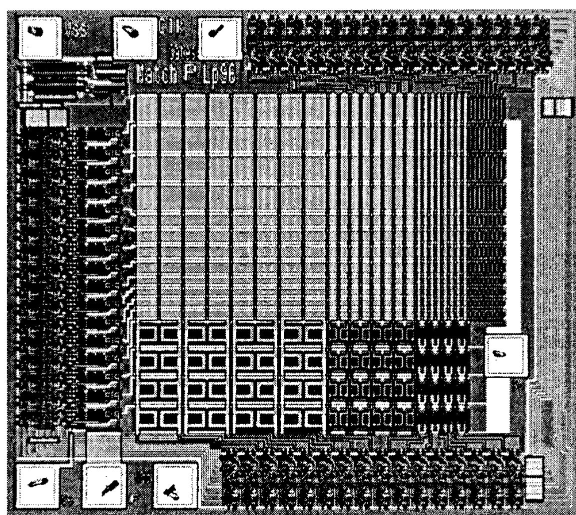

Fig. 1. Die photograph of the SOI PMOS matrix, the shift registers and the transmission gates. Total size is 1.3 mm by 1.1 mm. One metal layer and 2 μm design rules were used.

MATRIX DESCRIPTION

The transistors in the matrix share common gates for the columns and common sources for the rows (fig. 2). Drains are connected to a global terminal. Columns of transistors can be turned off by pulling their gates to the lowest potential of the circuit with the signals S_{Gx}, while two transmission gates isolate each unselected row with the signals S_{Sx}. These integrated switches present a non-negligible resistance. Nevertheless, their influence is eliminated by auxiliary transmission gates which allow force and sense measurement. A shift register (not drawn on fig. 2) surrounds the matrix and provides ON/OFF signals to the transmission gates.

In this circuit the DUTs act themselves as switches, yielding an extremely dense layout (fig. 3). Transistor sizes *W* and *L* are determined by the broadness of the polysilicon and diffusion strips. This circuit can be integrated with only one metal layer, which is appreciable during process development.

The SOI implementation needs 7 pads : V_D, V_F, V_S, V_{DD}, V_{SS}, V_{CLK}, V_G. During the programming of the matrix, data tokens are entered in the shift register through the pad V_G. In the bulk version, an additional pad is necessary for the

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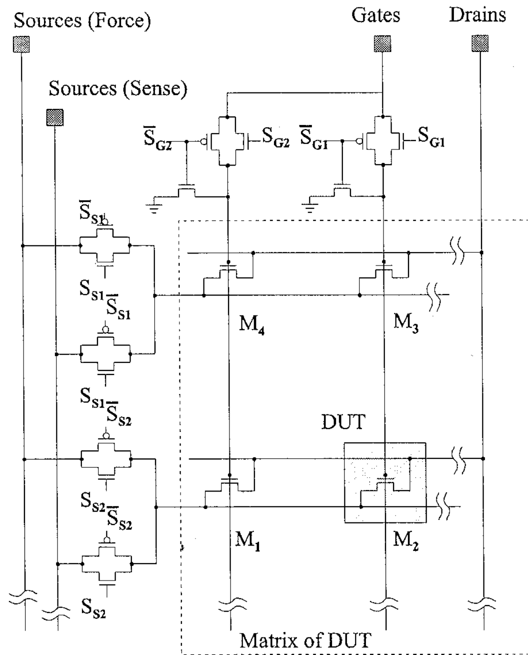

Fig. 2. Schematic of a NMOS transistors matrix and the multiplexing circuit. During the test of M_2, M_1 and M_4 have their gate voltage pulled to the lowest potential of the circuit while M_3 and M_4 see a high impedance at their source.

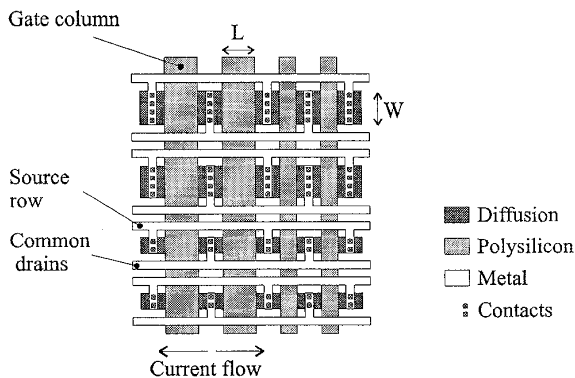

Fig. 3. Layout for the SOI implementation.

substrate of the transistors. The SOI circuit has no substrate but a global back gate node set to V_{SS}.

For the purpose of this study, transistors were drawn with gate lengths of 49, 19, 9 and 4 microns and widths of 49, 19 and 9 microns, resulting in 12 different combinations of W and L. In addition, concentric transistors with gate lengths of 9, 4 and 2 microns were added. Polysilicon columns were repeated 8 times for each size and diffusion rows 4 times, resulting in arrays of 32 transistors with the same dimensions. The total number of DUTs is 480. Table I summarizes these different dimensions.

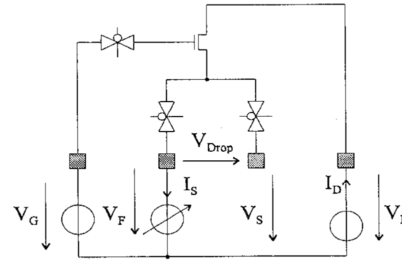

Fig. 4. Setup for the force and sense measurement of I_D vs. V_S characteristic.

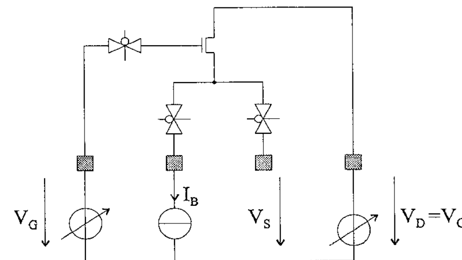

Fig. 5. Setup for the measurement of V_S vs. V_G. The bias current I_B is computed for each device from its I_D vs. V_S characteristic

DEVICE FABRICATION

Bulk samples were integrated on a standard N-well 2 μm process, with a 40 nm gate oxide. SOI devices use an experimental fully depleted process. SIMOX wafers (6 inches) with a buried oxide of 400 nm and a S_i film thickness of 110 nm are fabricated following a modified single poly 1 μm process [1]. No LDD was performed. These SOI devices have a 20 nm gate oxide over a final S_i thickness of 75 nm. Presently, the field isolation is performed with a LOCOS step. A parasitic transistor appears in the bird beak region of this LOCOS and deteriorates the subthreshold characteristics of finger style NMOS devices. In order to reach a threshold voltage of -0.4 V under a 3 V supply with a single doping polysilicon, the PMOS transistors are made of a $P^+P^-P^+$ structure instead of $P^+N^-P^+$ and are operated in accumulation mode [9]. Contrary to partially depleted SOI devices which suffer from floating body effects, fully depleted NMOS and PMOS have a macroscopic behavior similar to their bulk counterparts ; existing MOSFET models are therefore applicable [7][9].

MEASUREMENT AND PARAMETERS EXTRACTION

The measurement setup included a HP4156 semiconductor analyzer with 4 stimulus and measurement units (SMUs) and a programmable word generator. The SOI circuits were measured on wafer with their temperature kept at 35°C ± 0.2°C by a regulated chuck.

This matrix allows the access to the 4 terminals of the DUT and accepts current ranges from weak inversion to strong inversion. For example, output characteristics as well as transfer characteristics at constant V_{DS} with a compensation

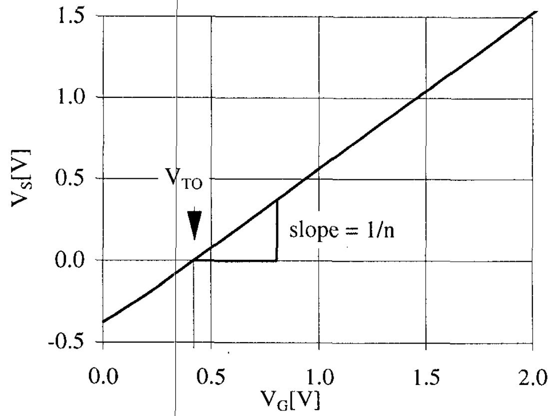

Fig. 6. Measured V_S vs. V_G of a SOI NMOS, 50 µm / 2 µm with I_B = 1.3 µA. The threshold voltage is defined as $V_{TO} = V_G = 0.420$V for $V_S = 0$. The slope factor n is the inverse of the slope of V_S vs. V_G.

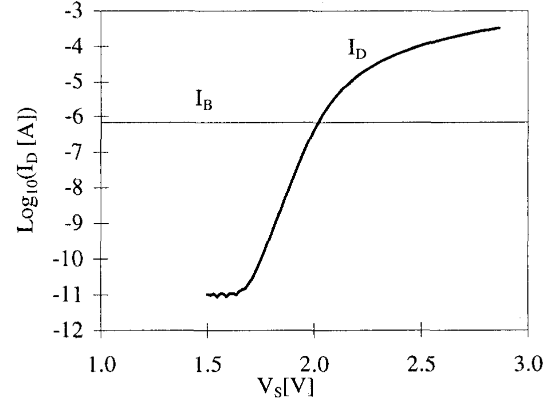

Fig. 7. I_D vs. V_S characteristics of a concentric SOI PMOS (50 µm / 2 µm) at $V_D = V_G = 1.5$ V. Bias current I_B used for the V_S vs. V_G measurement is displayed.

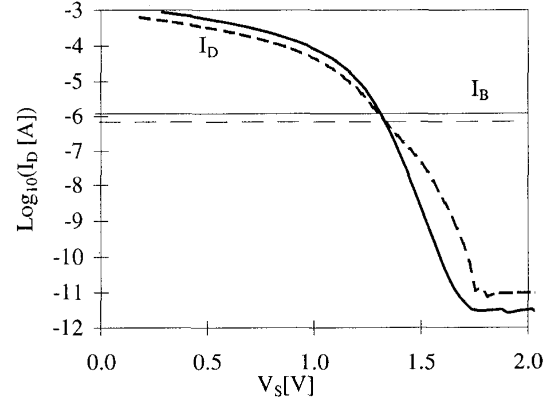

Fig 8. I_D vs. V_S characteristics for concentric SOI NMOS (50 µm / 2 µm, solid line) and finger style SOI NMOS (49 µm / 4 µm, dashed line) at $V_D = V_G = 1.8$ V. Corresponding bias currents I_B used for the V_S vs. V_G are displayed. Edge effects due the isolation process, which could not be fully suppressed, can be seen in the subthreshold slope of the finger style transistor.

of the voltage drop across the transmission gates by a feedback unit were successfully measured. However, for this study, the extraction methodology [6] developed for the EKV MOST model [7] was used for the threshold voltage V_{TO}, slope factor n and current factor β determination.

Current factor β extraction

Each DUT is first selected by programming of the register of the matrix. Its I_D vs. V_S characteristic is measured in strong inversion and saturation : the device gate and drain voltages are kept constant while the force terminal V_F is swept. I_S and I_D currents are measured (fig. 4). One of the SMU programmed in a zero current source is used to monitor the sense voltage V_S of the DUT. The product $n\beta$ is extracted from the maximum slope of the $I_D^{1/2}$ vs. V_S characteristic with (1) and (2).

$$I_D = \frac{\beta}{2n}\left(V_G - V_{TO} - nV_S\right)^2 \quad (1)$$

$$n\beta = 2\left(\frac{\partial\sqrt{I_D}}{\partial V_S}\right)^2 \quad (2)$$

Threshold voltage V_{TO} and slope factor n extraction

A second measurement is performed by biasing the transistor with a constant current source I_B. V_D and V_G are swept synchronously and the internal source voltage V_S is measured again (fig. 5). This bias current I_B is calculated for each device from its $n\beta$ product with (3). It equals half the so called *specific current* in the EKV model, and corresponds to the beginning of the moderate inversion of the channel (fig. 7 and 8).

$$I_B = n\beta U_T^2 \quad (3)$$

The threshold voltage V_{TO} and slope factor n are extracted from a linear regression over the V_S vs. V_G characteristic (fig. 6). The sensitivity of the linear regression to the measurement noise is low and therefore the DC analyzer can use short integration times. Moreover, as this measurement is done in moderate inversion, the source resistance of the DUT can be neglected. Finally, the accuracy of the threshold voltage weakly depends on the accuracy of the bias current itself when it is extracted in the subthreshold region, owing to the almost exponential characteristic of I_D vs. V_{GS}.

With a single circuit sample, the V_{TO} and β of 480 transistors from 15 arrays of identical size are extracted. However, mismatch variances cannot be computed directly from these arrays, because the 32 devices do not have an identical environment. Moreover, two contiguous columns of

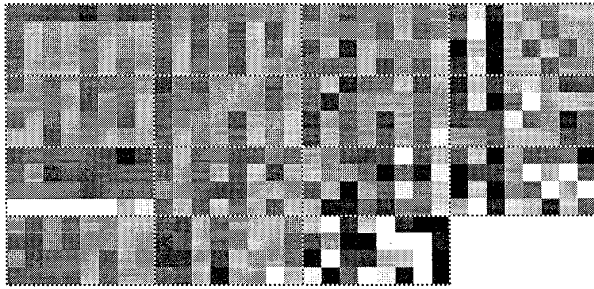

Fig. 9. Typical density plot of the normalized current factor β for a PMOS matrix. Higher values are darker. Systematic variations of β are observed at the at the edges of the matrix. Vertical strips are due to the influence of the direction of the current flow.

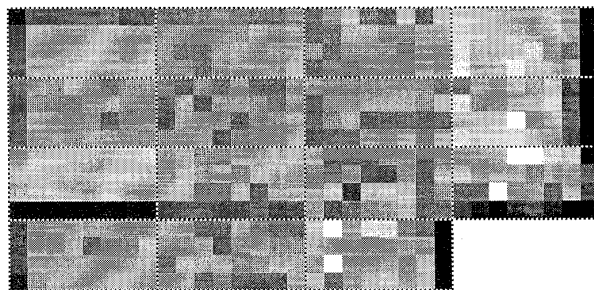

Fig. 10. Typical density plot of the normalized threshold voltage V_{TO} for a PMOS matrix. The more negative the V_{TO}, the darker its density. As for β, V_{TO} depends on the environment of the device.

transistors see their current flowing in opposite directions (fig. 3). First, the transistors from several circuits must be grouped into pairs having the same environment and orientation. Next, then the variance of the mismatch of these pairs is computed. Effects of the environment or the orientation of the matched pair as well as its layout style, like quads or interdigitized combinations, can also be studied with the same matrix.

RESULTS

Statistics were computed from 4 wafers, with 5 test matrices measured per wafer. For each type of transistor, 160 matched pairs were measured. Successive measurements of the same devices yielded standard deviations of 65 μVolts for ΔV_{TO} and 0.25‰ for $\Delta\beta/\beta_{mean}$. This measurement error is negligible in comparison with the intrinsic mismatch of the DUTs.

Matrix leakage

Leakage currents in the SOI matrices were evaluated by alternatively turning off the DUTs or the drain switches. Currents levels were below 20 pA. Indeed, it has been shown that leakage levels in this SOI process are extremely low [1].

Edge effects

Deterministic variations of parameters are observed at the edges of the matrices and at the border between finger style and concentric devices (fig. 9 and 10). Changes in the pattern of the gate as well as changes in the density of contact openings explain the latter deviation. Additionally, the β factor clearly relates to the direction of the current (fig. 9). For this reason transistors are grouped into pairs having a same environment before the computation of the mismatch.

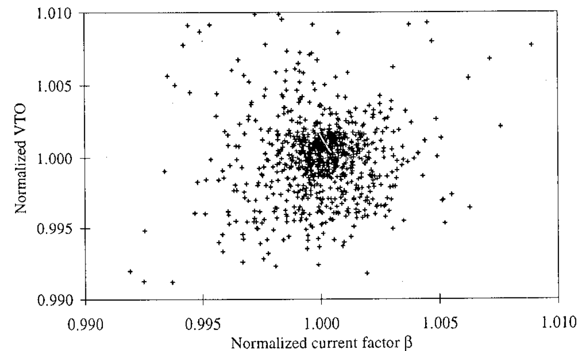

Fig. 11. Scatter plot of the normalized threshold voltage V_{TO} vs. the normalized current factor β for several PMOS matrices. The correlation coefficient is lower than 0.07.

Correlation between parameters

It was verified that the extraction procedure described before does not introduce a correlation between β and V_{TO}. The scatter plot of fig. 11 shows the independence of these two parameters.

Matching properties of fully depleted SOI MOSFETS

The standard deviation of the ΔV_{TO} and $\Delta\beta/\beta_{mean}$ for PMOS transistors follows a $WL^{-1/2}$ model, (4) and (5). The parameter A_{VTp} found for this SOI process is 16.5 mV/μm (fig. 12) which is slightly better than other values published for 1 μm bulk processes. The current matching parameter $A_{\beta p}$ is 4.1 %/μm (fig. 13), which is not as good as in bulk.

$$\sigma(\Delta V_{TO}) = \frac{A_{Vt}}{\sqrt{WL}} \tag{4}$$

$$\sigma\left(\frac{\Delta\beta}{\beta_{mean}}\right) = \frac{A_\beta}{\sqrt{WL}} \tag{5}$$

For NMOS transistors, the standard deviation of the threshold voltage clearly depends on the layout style (fig. 14). While the concentric devices exhibits a A_{Vtn} of 13 mV/μm, which is good for a 20nm t_{ox}, finger style transistors displays a A_{Vtn} of 44 mV/μm. This is obviously an effect of the parasitic transistor with a lower threshold voltage which appears in the bird beak region during the LOCOS (fig. 8). As the V_{TO} is extracted in moderate inversion, the mismatch reflects the influence of this parasitic effect. The current mismatch parameter of NMOS is also relatively high : $A_{\beta n}$ = 2.1 % / μm (fig. 15).

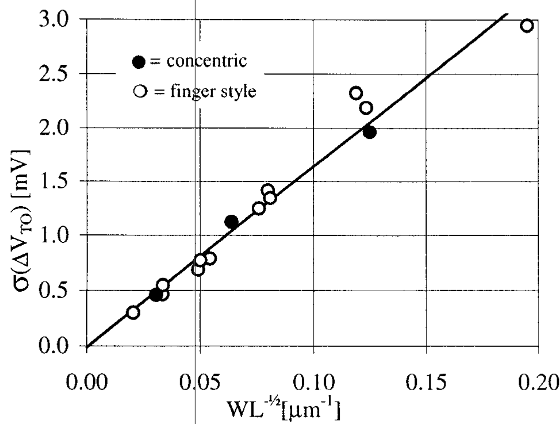

Fig. 12. Standard deviation of the threshold voltage mismatch ΔV_{TO} for SOI PMOS as function of the inverse of the square root of the effective area. A_{VTp} = 16.5 mV / μm.

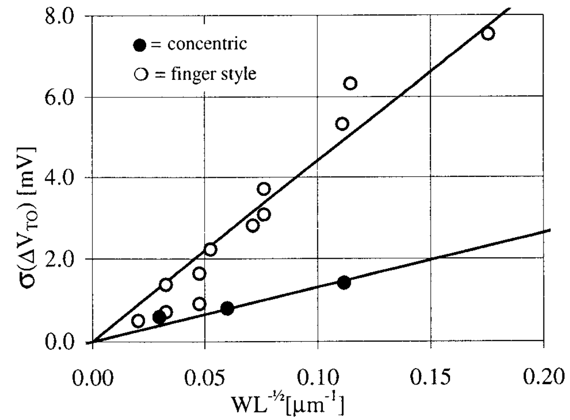

Fig. 14. Standard deviation of the threshold voltage mismatch ΔV_{TO} for SOI NMOS in function of the inverse of the square root of the effective area. A_{VTn} equals 44 mV / μm finger style devices and 13 mV / μm for concentric devices.

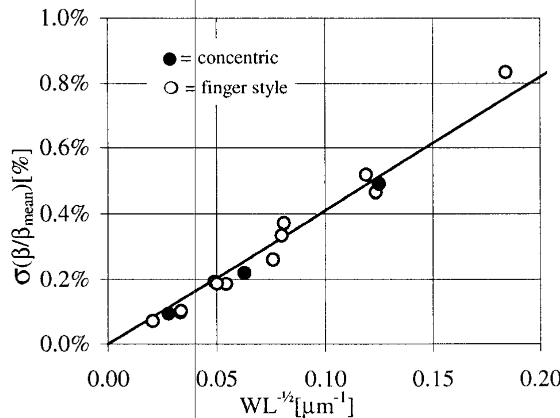

Fig. 13. Standard deviation of the relative current mismatch $\Delta\beta/\beta_{mean}$ for SOI PMOS as function of the inverse of the square root of the effective area. $A_{\beta p}$ = 4.1 % / μm.

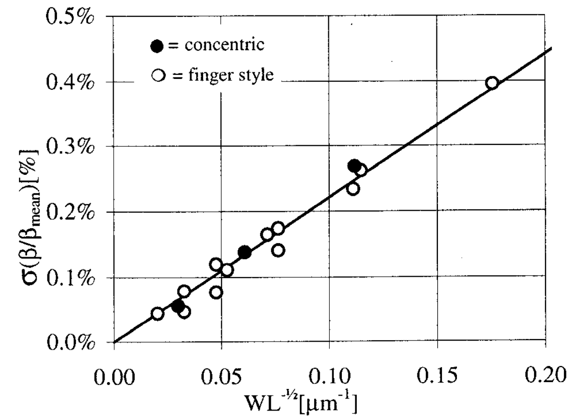

Fig. 15. Standard deviation of the relative current mismatch $\Delta\beta/\beta_{mean}$ for SOI NMOS as function of the inverse of the square root of the effective area. $A_{\beta n}$ = 2.3 % / μm.

Good A_{Vt} parameters are promising for low voltage analog applications, where the devices are operated in moderate inversion. On the other hand, the observed current matching is not as good as expected. It is important to keep in mind that the extraction method of β used here is sensitive to the mobility reduction and to the series resistor at the source side of the transistors. This problem is more pronounced than in bulk, due to the higher diffusion resistance of the SOI process. The higher resistance is caused by the silicon film thickness and the absence of a silicide step. The quality of the β matching might be improved by choosing a different extraction method.

Discussion

The measurements of the bulk samples illustrated another benefit of this test structure. Evidence of striation effect could be observed on some packaged circuits (fig. 16), supposedly due to packaging stress [10]. Matrices of closely located transistors allow a much denser sampling rate of the electrical parameters of the silicon surface compared to structures using differential pairs or quads. Therefore, low spatial frequency variations of the process parameters can be distinguished from high spatial frequency variations induced for example by packaging.

In this study, the matrix included 15 arrays of 32 identical transistors. However, the reorganization of these devices in into matched pairs leaves only 8 samples per arrays, which makes the measurement of several matrices necessary to establish a meaningful statistical analysis. Ideally, these arrays should count more identical transistors so that the statistics can be computed from one single matrix. This would allow to study the matching properties of a process as a function of the die position on the wafer.

CONCLUSION

A simple test structure that enables the characterization of a high number of closely located devices with a reduced equipment has been presented. This circuit features the cancellation of the transmission gates effect, provides an access to the four terminals of the devices and allows for parameters extraction from measurement in all operating regions of the device. Matching parameters for a fully depleted SOI process were presented.

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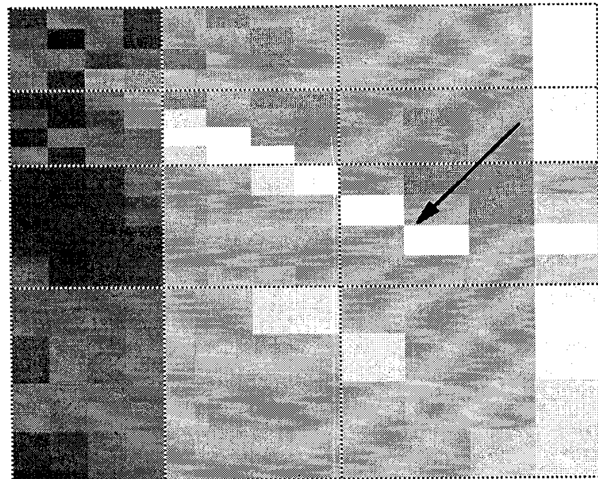

Fig. 16. Density plot of the threshold voltage V_{TO} of a NMOS bulk matrix. A striation clearly appears in the middle of the matrix, with a spacing of approximately 60 μm. Packaging stress might induce such an effect.

49 / 49	49 / 19	49 / 9	49 / 4
19 / 49	19 / 19	19 / 9	19 / 4
9 / 49	9 / 19	9 / 9	9 / 4
130 / 9 *)	75 / 4 *)	50 / 2 *)	

Table I. Organization of the SOI matrix. W / L are expressed in μm. Each W / L is repeated 32 times (4 row of 8 devices) in the matrix. *) indicates an estimated W for the concentric transistors.