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An Efficient Parameter Extraction Methodology for the EKV MOST Model

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Abstract- This paper presents a new parameter extraction methodology, based on an accurate and continuous MOS model dedicated to low-voltage and low-current analog circuit design and simulation (EKV MOST Model). The extraction procedure provides the key parameters from the pinch-off versus gate voltage characteristic, measured at constant current from a device biased in moderate inversion. Unique parameter sets, suitable for statistical analysis, describe the device behavior in all operating regions and over all device geometries. This efficient and simple method is shown to be accurate for both submicron bulk CMOS and fully depleted SOI technologies.

INTRODUCTION

The requirements for good MOS analog simulation models such as accuracy and continuity of the large- and small-signal characteristics are well established [1][2]. Continuity of the large- and small-signal characteristics from weak to strong inversion is one of the main features of the Enz-Krummenacher-Vittoz or EKV MOS transistor model [3][4][5].

One of the basic concepts of this model is the pinch-off voltage. A constant current bias is used to measure the pinch-off voltage versus gate voltage characteristic in moderate inversion (MI). This measure allows for an efficient and simple characterization method to be formulated for the most important model parameters as the threshold voltage and the other parameters related to the channel doping, using a single measured characteristic. The same principle is applied for various geometries, including short- and narrow-channel devices, and forms the major part of the complete characterization methodology.

The simplicity of the model and the relatively small number of parameters to be extracted eases the parameter extraction. This is of particular importance if large statistical data are to be gathered. This method has been validated on a large number of different CMOS processes. To show its flexibility as well as the abilities of the model, results are presented for submicron bulk and fully depleted SOI technologies.

SHORT DESCRIPTION OF THE STATIC MODEL

A detailed description of the model formulation can be found in [3]; important concepts are shortly recalled here since they form the basis of the parameter extraction. A set of 13 intrinsic parameters is used for first and second order effects, listed in Table I. Unlike most other MOS simulation models, in the EKV model the gate, source and drain voltages, V_G, V_S and V_D, are all referred to the substrate in order to preserve the intrinsic symmetry of the device.

Table I: *Main EKV intrinsic model parameters for first and second order effects. Parameters for impact ionization are not included.*

Name	Description	Units
COX	Gate oxide capacitance	F/m
VTO	Nominal threshold voltage	V
GAMMA	Body effect factor	$V^{1/2}$
PHI	Bulk Fermi potential (2x)	V
KP	Transconductance parameter	A/V^2
THETA	Mobility reduction coefficient	1/V
UCRIT	Longitudinal critical field	V/m
XJ	Junction depth	m
DL	Channel length correction	m
DW	Channel width correction	m
LAMBDA	Depletion length coefficient	-
LETA	Short channel effect coefficient	-
WETA	Narrow channel effect coefficient	-

The Pinch-off Voltage

The threshold voltage VTO, which is consequently also referred to the bulk, is defined as the gate voltage for which the inversion charge forming the channel is zero at equilibrium. The pinch-off voltage V_P corresponds to the value of the channel potential V_{ch} for which the inversion charge becomes zero in a non-equilibrium situation. V_P can be directly related to V_G:

$$V_P = V_G' - \mathrm{PHI} - \gamma' \cdot \left[\sqrt{V_G' + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2}\right] \tag{1}$$

$$V_G' = V_G - \mathrm{VTO} + \mathrm{PHI} + \mathrm{GAMMA} \cdot \sqrt{\mathrm{PHI}} \tag{2}$$

where the parameter $\mathrm{GAMMA} = \sqrt{2q\varepsilon_{si}N_{sub}}/C_{ox}$ is the body effect factor and the parameter PHI is the approximation of the surface potential in strong inversion. The weak inversion slope factor n is defined as the inverse of the partial derivative of the pinch-off voltage with respect to the gate voltage:

$$n \equiv \left[\frac{\partial V_P}{\partial V_G}\right]^{-1} = 1 + \frac{\mathrm{GAMMA}}{2 \cdot \sqrt{V_P + \mathrm{PHI}}} \tag{3}$$

For large device geometries, for which $\gamma' = \mathrm{GAMMA}$, the pinch-off voltage is a function only of the gate voltage and the three parameters VTO, GAMMA and PHI. This formulation is derived assuming uniform doping in the channel. It can be shown that leaving GAMMA and PHI, which are both related to

the channel doping, as two independent parameters, allows to account for weak non-uniform doping, with parameter values slightly different from their initial physical meaning. Another simple solution to take into account stronger non-uniform doping profiles is under investigation [6].

The corrected body effect factor γ' accounts for small geometry effects. This makes the pinch-off voltage depend on the effective channel length and width, and on the drain and source voltages V_D and V_S, through parameters LETA for short-channel and WETA for narrow-channel effects:

$$\gamma' = \mathrm{GAMMA} - \frac{\varepsilon_s}{\mathrm{COX}} \cdot \left[\frac{\mathrm{LETA}}{L + \mathrm{DL}} \cdot \sqrt{\mathrm{PHI} + V_D} + \left(\frac{\mathrm{LETA}}{L + \mathrm{DL}} - \frac{3 \cdot \mathrm{WETA}}{W + \mathrm{DW}}\right) \cdot \sqrt{\mathrm{PHI} + V_S}\right] \quad (4)$$

This formulation is based on the charge-sharing concept and can be shown to be equivalent to the drain induced barrier lowering (DIBL) [7].

Drain Current

The drain current is decomposed in a forward and a reverse current I_F and I_R, which are functions of V_P - V_D and V_P - V_S respectively:

$$I_D = I_F(V_P - V_S) - I_R(V_P - V_D) \quad (5)$$

Using a normalization factor called the specific current $I_S \equiv 2n\beta_{eff}U_T^2$, both components are interpolated from weak (WI) to strong inversion (SI):

$$I_{F(R)} = I_S \cdot \left[ln\left(1 + \exp\left[\frac{V_P - V_{S(D)}}{2 \cdot U_T}\right]\right)\right]^2 \quad (6)$$

where $U_T \equiv k \cdot T/q$ and the term $\beta_{eff} \sim \mathrm{KP}(W_{eff}/L_{eff})$ introduces the transconductance parameter KP. Both the I_F and I_R components account for drift and diffusion current. Note that in saturation I_R becomes negligible with respect to the I_F. Simple expressions for the drain current and the small-signal conductances in different operating regimes are obtained and conveniently listed in [4].

Mobility reduction due to the vertical field (THETA), velocity saturation (UCRIT) and channel length modulation (LAMBDA) effects are accounted for in the transconductance term β_{eff}. Although the EKV model accounts for the effects of impact ionization, requiring three additional parameters, these will not be discussed here for simplicity. It also includes a complete dynamic model, which does not require any additional intrinsic parameter. Further information concerning the formulation of the simulation model can be found in [5].

The Pinch-off Voltage Extraction Method

Pinch-off Voltage Measurement Principle

According to (6), the pinch-off voltage can be measured at the source end of the device in saturation, for a particular value of the drain current approximately equal to half the specific current I_S. The transistor is therefore biased in the middle of the moderate inversion (MI) region. The V_P *vs.* V_G characteristic is simply obtained by sweeping the gate voltage and measuring the source voltage $V_S \approx V_P$. Examples of such characteristics for a 0.7µm CMOS technology are shown in Fig. 2 for n- and p-channel devices of different geometries.

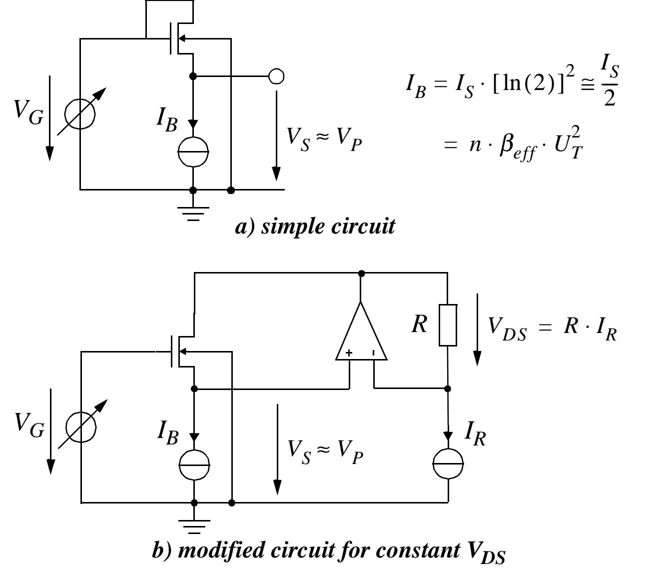


Fig. 1: *Circuits used for the measurement of the pinch-off voltage V_P vs. V_G characteristic.*

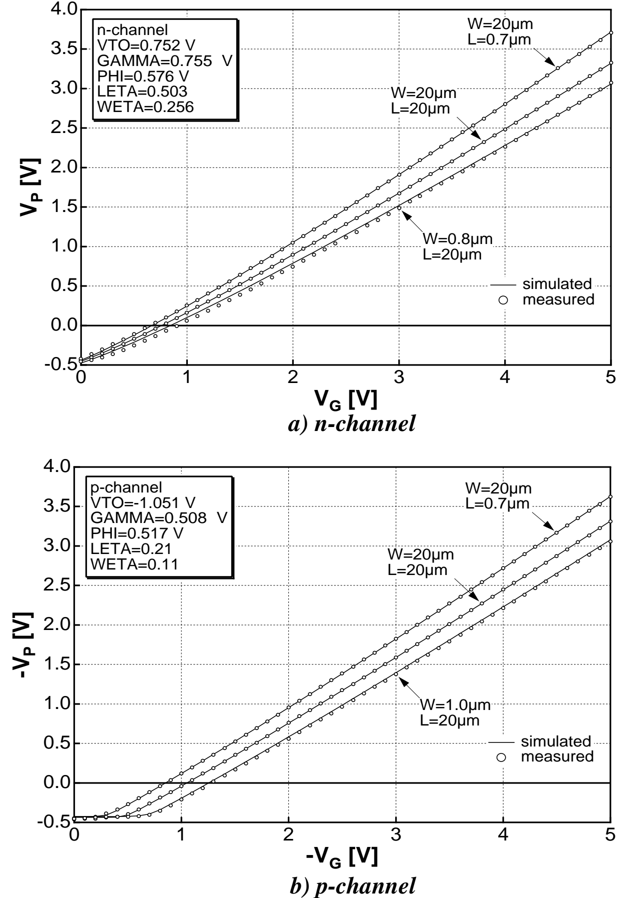


Fig. 2: *Pinch-off voltage characteristics V_P vs. V_G and parameter extraction for three device sizes for devices of a 0.7µm CMOS technology.*

A disadvantage of the circuit in Fig. 1a) is that the V_{DS} volt-

age is not kept constant when sweeping V_G. This results in a small error due to channel length modulation, affecting mainly short-channel devices. This drawback can be circumvented by connecting the drain terminal to an additional voltage source controlled either by the swept gate voltage or by the measured source voltage. In the first case V_D has to be a linear function of V_G with an adequate slope such that V_{DS} remains almost constant. The second case is illustrated in the circuit in Fig. 1b), where the V_{DS} voltage is imposed constant by means of an opamp and can be adjusted by current source I_R. Similar results can be obtained by using the 'analog feedback unit' provided with the HP4142 DC parameter tester. The imposed V_{DS} should not be too large in order to avoid velocity saturation effect. Since the transistor is biased in MI, a voltage of $V_{DS} > 5U_t$ is sufficient to maintain the transistor in saturation. It is worth mentioning that mobility reduction is found to be negligible thanks to the operation in MI.

Specific Current Determination

Since the specific current I_S depends on the device size, it has to be determined for any device prior to the pinch-off voltage measurement. For a given gate voltage (i.e. a fixed pinch-off voltage), it is thus simple to determine I_S from the strong inversion slope of the $\sqrt{I_D}$ *vs.* V_S characteristic, derived from the drain current expression in SI saturation:

$$\sqrt{I_D} = \sqrt{\frac{n \cdot \beta}{2}} \cdot (V_P - V_S) = \frac{\sqrt{I_S}}{2U_t} \cdot (V_P - V_S) \tag{7}$$

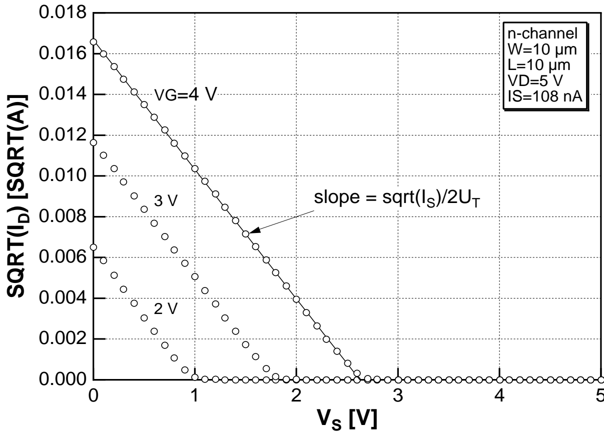


Fig. 3: *Principle of the determination of the specific current from the* $\sqrt{I_D}$ *vs.* V_S *characteristic in strong inversion saturation.*

The principle is illustrated in Fig. 3; lower values for V_D and V_G can reduce saturation and mobility reduction effects.

Parameter Extraction

VTO is determined as the particular value of V_G corresponding to the $V_P = 0$ cross point. GAMMA and PHI are extracted by fitting (1) to the measured characteristic. Note that this does not imply the entire evaluation of the simulation model which makes this operation simple. As shown in Table II for a 1µm CMOS process, the sensitivity of the extracted values of VTO, GAMMA and PHI with respect to I_B is low, demonstrating the robustness of the method.

Table II: *Extracted values of* VTO, GAMMA *and* PHI *and variations for changes of* I_B *with respect to its nominal value (bold), for a 1µm CMOS technology.*

I_B	I_B/I_S	VTO	Δ_{VTO}	GAMMA	Δ_{GAMMA}	PHI	Δ_{PHI}
nA		mV		$m\sqrt{V}$		mV	
n-channel, W=20µm, L=20µm							
71	*1/4*	*755*	*-35*	*672*	*-2*	*368*	*-16*
106.5	*3/8*	*775*	*-15*	*673*	*-1*	*378*	*-6*
142	***1/2***	***790***	**-**	***674***	**-**	***384***	**-**
213	*3/4*	*812*	*+22*	*674*	*-*	*395*	*+9*
284	*1*	*828*	*+38*	*675*	*+1*	*401*	*+17*
p-channel, W=20µm, L=20µm							
-20	*1/4*	*-1001*	*31*	*667*	*4*	*1009*	*10*
-30	*3/8*	*-1019*	*13*	*664*	*1*	*1000*	*1*
-40	***1/2***	***-1032***	**-**	***663***	**-**	***999***	**-**
-60	*3/4*	*-1052*	*-20*	*661*	*-2*	*994*	*-5*
-80	*1*	*-1068*	*-36*	*658*	*-5*	*983*	*-16*

The pinch-off voltage extraction method is comparable to other constant current methods [8]. The bias current is given a precise meaning here. VTO is extracted unambiguously with a unique value without need of extrapolation. GAMMA and PHI are obtained from the same measured characteristic. The advantages of this method are its simplicity, efficiency and speed. The pinch-off voltage extraction method also provides a means to explore behavior with changing bias and geometries. Further parameters are extracted from different device sizes as indicated below.

The Parameter Extraction Methodology

The extraction procedure for the EKV model strongly benefits from its simple formulation and its small number of parameters. The complete extraction method, formulated to obtain a single parameter set for all geometries of a given type of device, is summarized in Table III. Parameter extraction is performed sequentially from DC measurements, requiring at least three device sizes. The gate capacitance COX and the junction depth XJ are assumed to be known from a preliminary extraction.

The pinch-off voltage measurement is used to extract the parameters VTO, GAMMA and PHI from a long and large device as previously described (Fig. 2). From the same device, the mobility related parameters KP and THETA are obtained from the I_D *vs.* V_G characteristic.

Note that the V_P *vs.* V_G characteristic is also used for the extraction of parameters related to short- as well as narrow-channel effects. This requires the channel length and width corrections DL and DW to be previously extracted, which can be done with methods that simultaneously yield the resistance due to source and drain diffusions RS and RD [9].

Keeping the parameters obtained from the long and large device, in particular VTO, the parameters LETA and WETA related to short- respectively narrow-channel effects can be extracted from the measured pinch-off voltage characteristics for these devices (upper respectively lower curves in Fig. 2), using again (1), but taking into account the corrected body

Table III: *Summarized extraction procedure for the EKV model, featuring device sizes, measured characteristics, conditions (*SI: *strong,* MI: *moderate,* WI: *weak inversion,* co.: *conduction,* sat.: *saturation) and extracted parameters and fine tuning.*

Device sizes	Characteristics	Conditions	Parameters
Parameter Extraction			
matrix W/L	R *vs.* L_{eff} $1/R$ *vs.* W_{eff}	SI co.	`DL,RS+RD` `DW`

wide/long	I_D *vs.* V_S
	V_P *vs.* V_G
	I_D *vs.* V_G
		SI sat.
		MI sat.
		SI sat.@V_S
			I_S
			`VTO,GAMMA,PHI`
			`KP,THETA`

wide/short	I_D *vs.* V_S
	V_P *vs.* V_G
	I_D *vs.* V_D
		SI sat.
		MI sat.
		SI co.-sat.
			I_S
			`LETA`
			`UCRIT,LAMBDA`

narrow/long	I_D *vs.* V_S V_P *vs.* V_G	SI sat. MI sat.	I_S `WETA`
Parameter Fine Tuning			
wide/short	$log(I_D)$ *vs.* V_G I_D,$log(gds)$ *vs.* V_D	WI@V_S SI co.-sat.	`LETA` `DL,RS+RD,XJ`
narrow/long	I_D *vs.* V_G I_D,$log(gds)$ *vs.* V_D	WI@V_S SI co.-sat.	`WETA` `DW`

effect factor given by (4).

The only parameters remaining to be extracted are those related to velocity saturation (`UCRIT`) and channel length modulation (`LAMBDA`), which are obtained from the short-channel output characteristic. As a last step, some parameters may be fine tuned to further improve results in particular operation regions if needed.

The efficiency of nonlinear optimization algorithms strongly depends on the amount of data used and the complexity of the model equations to be evaluated. Further simplifications of the model equations are possible as is the case with the pinch-off voltage. Appropriate initial values for parameters to be optimized can be found using techniques similar to 'direct extraction' methods.

RESULTS AND DISCUSSION

Submicron CMOS technology

A comparison of measurements and simulation are presented for a 0.7µm CMOS technology. Fig. 2 specifies the parameter values obtained from the pinch-off voltage extraction. Measured and simulated I_D *vs.* V_G characteristics for a long and a short device are shown in Fig. 4. For the short channel device, the gate and source transconductances, differentiated numerically from the DC characteristics, are presented in Fig. 5 and clearly show the continuity of the first-order derivative of the model, in particular in the MI region. Output characteristics of Fig. 6 show a high accuracy in weak and strong inversion as well as in conduction and saturation regimes. Effects of impact ionization have been included in the simulation.

The accuracy in subthreshold operation is excellent over a large bias range. Note that there is no specific parameter to adjust the subthreshold slope and that a single parameter set

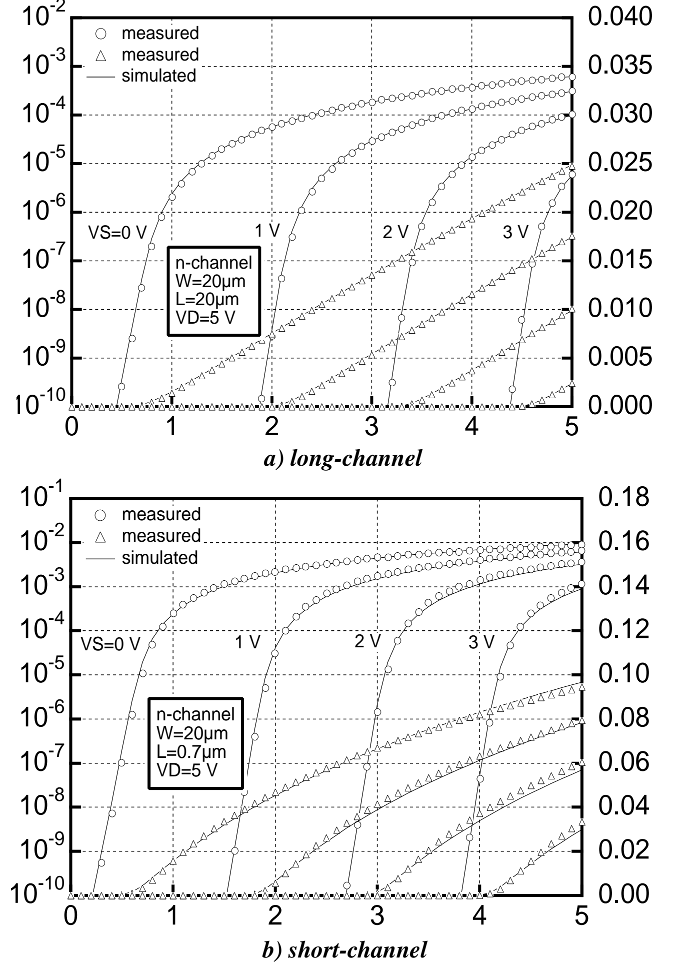


Fig. 4: *Transfer characteristics* $log(I_D)$ & $\sqrt{I_D}$ *vs.* V_G *of n-channel devices.*

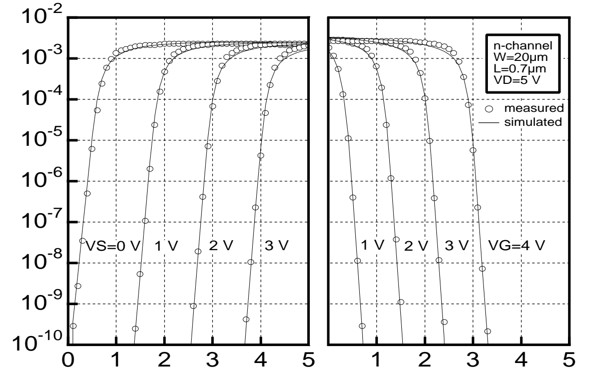
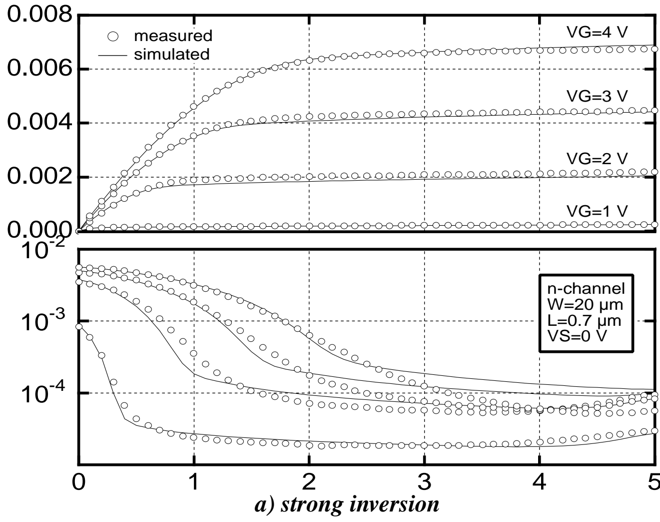


Fig. 5: *Gate and source transconductances* g_{mg} *vs.* V_G *respectively* g_{ms} *vs.* V_S *of a short n-channel device.*

has been used for all the simulated characteristics.

The scaling behavior of the model resulting from the formulation of (4) is acceptable, considering that there are no 'length- and width sensitivity' parameters. Single parameter sets could be obtained for many different CMOS technologies with minimum feature sizes ranging from 3µm to 0.7µm. However improvements of the scaling behavior are possible and further investigations using the pinch-off voltage extraction method are under progress.



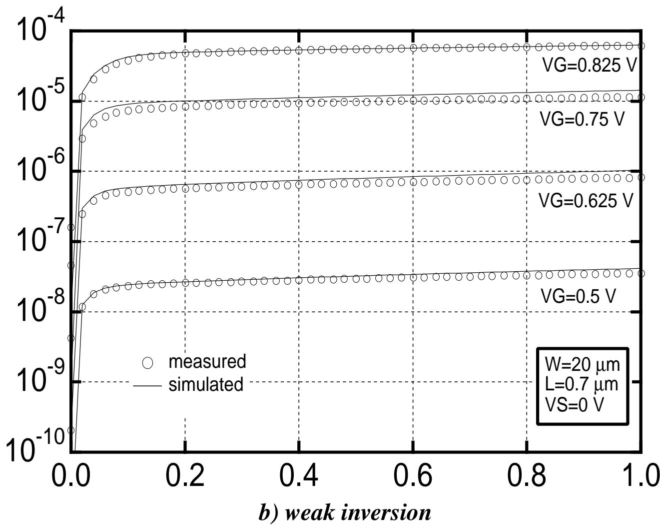


Fig. 6: *Output characteristics I_D & g_{ds} vs. V_D of a short n-channel device.*

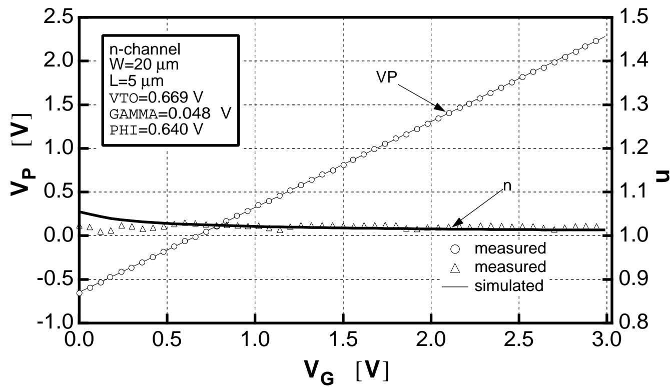


Fig. 7: *V_P vs. V_G characteristic and derived slope factor n for an n-channel device of a fully depleted SOI technology.*

Fully depleted SOI

Results presented here are obtained from a fully depleted silicon on insulator (SOI) 3V technology. The operating voltages, referred to the back gate in this case, need to be reduced to avoid kink effects [10]. As expected for fully depleted silicon on insulator (SOI) devices, the substrate effect is very low.

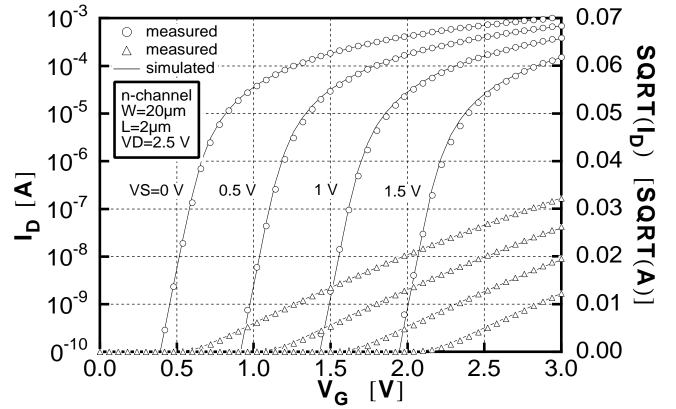


Fig. 8: *$log(I_D)$ & $\sqrt{I_D}$ vs. V_G characteristics for a short-channel device of a fully depleted SOI technology.*

Fig. 9: *Gate and source transconductances g_{mg} vs. V_G and g_{ms} vs. V_S of a wide and short SOI device.*

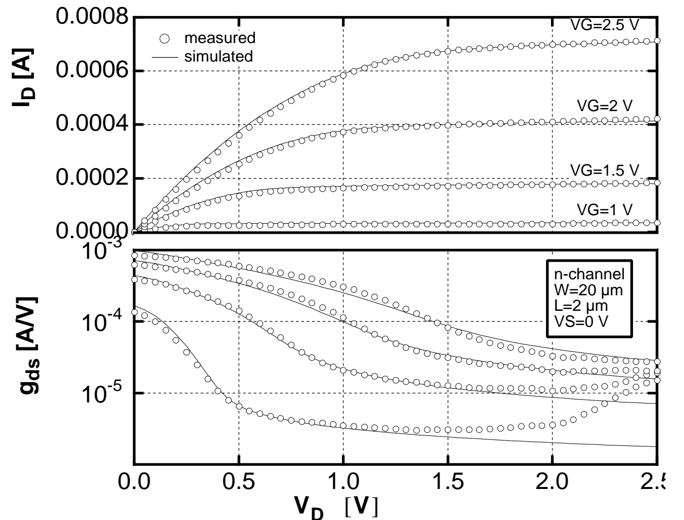


Fig. 10: *Output characteristics I_D & g_{ds} vs. V_D of a short n-channel device of a fully depleted SOI technology.*

An almost ideal slope factor *n* is found in Fig. 7, consistent with the low `GAMMA` value. The EKV MOST model accurately predicts device behavior in all operating regions, as shown in similar characteristics as before in Fig. 8 to 10. In the latter, the kink effect can be observed, which is not included in the simulation model.

CONCLUSION

A new parameter extraction technique based on the measurement of the pinch-off voltage vs. gate voltage characteristic in moderate inversion has been presented. These results demonstrate the abilities of the simulation model, as well as the flexibility of the extraction method based on the V_P *vs.* V_G characteristic. This fast and efficient method has been automated for the obtention of large statistical data, and is also made available in several commercial parameter extraction environments. Results of this extraction method and the accuracy of the EKV MOST model have been demonstrated for submicron CMOS bulk and fully depleted SOI technologies, using a single parameter set covering all device geometries.

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REFERENCES

[1] Y. Tsividis and K. Suyama, "MOSFET Modeling for Analog Circuit CAD: Problems and Prospects", JSSC, Vol. 29, No. 3, pp 210-216, 1994

[2] G. Machado and C. Toumazou, "Systematic Design-Oriented Characterisation of MOS devices and Circuit Building Blocks in Engineering Education", Proceedings of the IX Congress of the Brasilian Society of Microelectronics, pp. 243-257, Rio de Janeiro, August 1994.

[3] C. C. Enz, F. Krummenacher and E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications", Special issue of the Analog Integrated Circuits and Systems Processing Journal on Low-Voltage and Low-Power Circuits, July 1995.

[4] G. Machado, C. C. Enz and M. Bucher, "Estimating key parameters in the EKV MOST model for analogue design and simulation", IEEE ISCAS'95, April 29-May 3, 1995.

[5] M. Bucher, C. Lallement, C. Enz and F. Krummenacher, "Accurate MOS Modelling for Analog Circuit Simulation using the EKV MOST Model", to be published Proc. IEEE Int. Symposium on Circuits and Systems, 1996.

[6] C. Lallement, C. C. Enz and M. Bucher, "Simple Solutions for Modeling the Non-Uniform Substrate Doping", to be published Proc. IEEE Int. Symposium on Circuits and Systems, 1996.

[7] Y. P. Tsividis, "Operation and modelling of the MOS Transistor", McGraw-Hill, 1987.

[8] H. G. Lee, S. Y. Oh and G. Fuller, "A simple and accurate Method to Measure the Threshold Voltage of an Enhancement-Mode MOSFET", Trans. on Elec. Devices, Vol. ED-29, No. 2, pp 346-348, February, 1982.

[9] N. Arora, "MOSFET Models for VLSI Circuit Simulation: Theory and Practice", Chap. 9, Computational Microelectronics, Ed. S. Selberherr, 1993

[10] J.-P. Colinge, "Silicon-On-Insulator Technology", Material to VLSI, Kluwer Academic Publishers, 1991