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Design-Oriented Characterization of CMOS over the Continuum of Inversion Level and Channel Length

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Abstract

A methodology for small signal characterization of CMOS processes over the full range of inversion level and channel length is presented. Measured transconductance and output conductance of a 0.5mm standard CMOS process are presented from deep weak inversion to deep strong inversion for both NMOS and PMOS devices for channel lengths ranging from 0.5mm to 33.4mm. The data is presented in normalized form permitting device evaluation at any inversion level, channel length, and drain current. This characterization is useful for modern analog CMOS design anywhere in the continuum of inversion level and channel length. This method furthermore presents a novel and rigorous benchmark for evaluating the accuracy of compact MOS models. Initial results are given illustrating EKV MOS model transconductance accuracy. The characterization methodology can be extended to deeper submicron processes addressing the increasing uncertainty in small signal parameter values and MOS model accuracy.

1. Introduction

Analog CMOS design is greatly complicated by the large change in transconductance (g_m), output conductance (g_{ds}), and body-effect transconductance (g_{mb}) over the continuum of inversion level and channel length. In modern IC design, MOS devices may be operated anywhere in the weak to strong inversion continuum and over the range of available channel lengths. The selection of inversion level and channel length permits necessary tradeoffs in circuit bandwidth, dc gain, dc matching, noise, minimum supply voltage, and power efficiency.

Simple, accurate, small-signal MOS hand analysis is available only in weak inversion (exponential-law I-V) and strong inversion (square-law I-V), and in the latter *only* if mobility reduction and velocity saturation effects are not considered. However, the modern designer may operate devices in moderate inversion for power-efficient transconductance and low V_{DSAT}, both needed for low supply voltage operation. Additionally, the square-law region of strong inversion vanishes as deeper submicron devices exhibit mobility reduction and velocity saturation effects at increasingly lower levels of inversion.

Although continuous inversion compact MOS models, like the EKV MOS model [1,2], offer manageable hand calculation of MOS transconductance in moderate inversion, simple hand analysis of transconductance is not available for short channel devices exhibiting mobility reduction and velocity saturation effects in strong inversion. Simple hand analysis of MOS output conductance, with its long history of serious MOS modeling errors, remains an especially elusive goal for analog designers. g_{ds} depends strongly on channel length and exhibits inversion-level dependency, especially for short channel devices where it increases at weak inversion due to Drain Induced Barrier Lowering (DIBL). At high levels of strong inversion, g_{ds} is governed mainly by velocity saturation and channel length modulation (CLM) effects.

Given the unavailability of usable hand analysis for MOS small signal parameters and the potential for serious modeling errors, the modern analog designer needs evaluation of small signal parameters over the dual dimensions of inversion level and available channel length. Such an evaluation can be obtained from traditional device curves, but would require extensive measurements and interpretation.

2. Normalization of Level of Inversion

The inversion coefficient (*IC*) provides a very useful way of identifying the operating region and level of inversion [3] of MOS transistors. The inversion coefficient will be used as the x-axis of the MOS transconductance and output conductance presented in this paper. The inversion coefficient is defined as

$$IC = \frac{I_D}{2nm_0C_{OX}(W/L)U_T^2} = \frac{I_D}{2nk_0(W/L)U_T^2}, \quad (1)$$

where I_D is the drain current, n is the slope factor, m_0 is the low-field mobility, C_{OX} is the gate oxide capacitance, U_T is the thermal voltage (kT/q), $k_0=m_0C_{OX}$, and W and L are the effective channel width and length respectively. Although n has slight gate bias dependency, decreasing with increasing gate bias, it is assumed constant here. The inversion coefficient can be expressed in simplified form as

$$IC = \frac{I_D}{I_0(W/L)}, \quad (2)$$

where I_0 is a process dependent current equal to $2nk_0U_T^2$. For the 0.5µm process considered here, the value of I_0 is 0.208µA for k_0 = 110µA/V^2 and n = 1.4 for NMOS, while I_0 is 0.07µA for k_0 = 37µA/V^2 and n = 1.4 for PMOS. The technology dependent current I_0 is the drain current of a unity shape factor device (W/L = 1) at the center of moderate inversion where IC = 1. The inversion

coefficient is less than 0.1 for weak inversion, 1 for the center of moderate inversion, and greater than 10 for strong inversion. The center of moderate inversion (IC = 1) is defined where the asymptotic value of transconductance to current ratio in weak inversion is equal to the asymptotic value of strong inversion [1], both of which overestimate the actual value in moderate inversion by almost 40%.

3. Continuum of Transconductances

Measurements were made on a custom semiconductor parameter analyzer. The analyzer has a 10-decade drain current range covering 10 pA to 100 mA, with most measurements made over a 1 nA to 10 mA range (7 decades) at an accuracy of approximately 0.1%. A/D and D/A conversion resolution is 16 bits.

Figures 1 and 3 show measured transconductance efficiency (or transconductance to current ratio g_m/I_D) for the NMOS and PMOS devices respectively over more than 7 decades of inversion (IC < 0.001 to IC > 1000). The asymptotes of ideal transconductance efficiency in weak and strong inversion, neglecting mobility reduction and velocity saturation effects, are indicated. The roll-off of transconductance efficiency is clearly observed for inversion above weak inversion and is nearly identical for the 0.5µm to 33.4µm range of channel lengths. At high levels of strong inversion, an additional degradation with respect to the ideal asymptotes occurs in particular for short-channel devices.

Figures 1 and 3 also show simulated results obtained with the EKV v2.6 MOS model [2]. The model shows a good qualitative behavior over most of the inversion levels, with particularly accurate results in weak and moderate inversion. In very strong inversion, the model remains accurate for long-channel devices, while the transconductance efficiency is slightly overestimated for the shorter-channel devices.[1]

Figures 2 and 4 show measured output conductance, expressed as the Early voltage, for the NMOS and PMOS devices respectively, over more than 5 decades of inversion (IC = 0.01 to IC ~ 1000). Here the strong dependency on channel length is clear, but inversion level dependency is also observed, illustrating potential problems with the assumption of a constant Early voltage depending only on channel length. Early voltage is observed to increase dramatically for short channel NMOS devices (output conductance decreasing dramatically) for high levels of inversion. As noted in the graphs, self-heating effects may possibly affect the data at high levels of inversion (IC > 100) and short channel length.[2] Nevertheless these characteristics provide important information to the designer, and furthermore they also constitute particularly difficult benchmark tests for the accuracy -- and adequacy -- of compact MOS models.

The data presented allow the analog IC designer to select virtually any level of MOS inversion, select virtually any channel length, and then observe the measured transconductance efficiency and Early voltage. From these, operating transconductance and output conductance are readily calculated for a selected drain current. Body effect transconductance, expressed as $h = g_{mb}/g_m$, was also evaluated but is not presented due to limited space.

4. Conclusions

A novel methodology for small signal characterization of CMOS technology for advanced analog IC design has been presented. Measured transconductance and output conductance from a 0.5µm CMOS process are presented from deep weak inversion to deep strong inversion over a range of channel lengths. Key device characteristics for analog CMOS design are consistently presented with respect to the level of inversion in MOS transistors. This characterization provides the designer with valuable information on measured small signal parameters for any inversion level and channel length. Such information is not readily available from hand-calculation methods. The increasingly important moderate inversion region is also addressed. In addition, the characterization method provides a rigorous and novel benchmark for compact MOS models. A comparison of the EKV v2.6 MOS model with the measured transconductance efficiency shows excellent agreement in weak and moderate inversion. The characterization methodology is applicable to deep submicron CMOS, where it may prove particularly useful in addressing the increasing uncertainty regarding small signal parameters and accuracy of compact MOS models.

References

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[2] M. Bucher, C. Lallement, C. Enz, F. Théodoloz, F. Krummenacher, "The EPFL-EKV MOSFET Model Equations for Simulation, Version 2.6", Technical Report, EPFL, 1997, http://legwww.epfl.ch/ekv/.

[3] E. Vittoz, "Micropower Techniques", in *Design of MOS VLSI Circuits for Telecommunications*, ed. J. Franca, Y. Tsividis, Prentice-Hall,1994.

[1] Model parameter extraction was performed on data from different dice than. the present measured data. Note that a single parameter set is used for all geometries.

[2] The exact measurement of g_{ds} is exceedingly difficult for low values in saturation and is especially subject to self-heating.

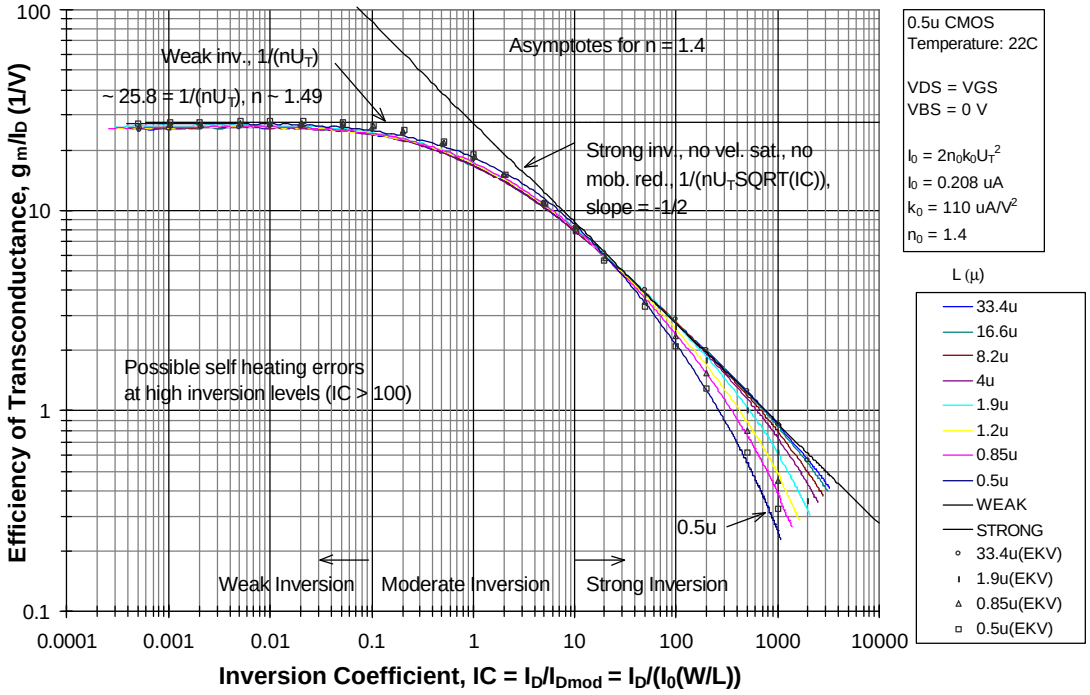

Fig. 1. NMOS g_m/I_D vs. inversion coefficient from weak through strong inversion for L = 0.5µm - 33.4µm. Measurement (lines) and simulation with the EKV v2.6 MOS model (markers).

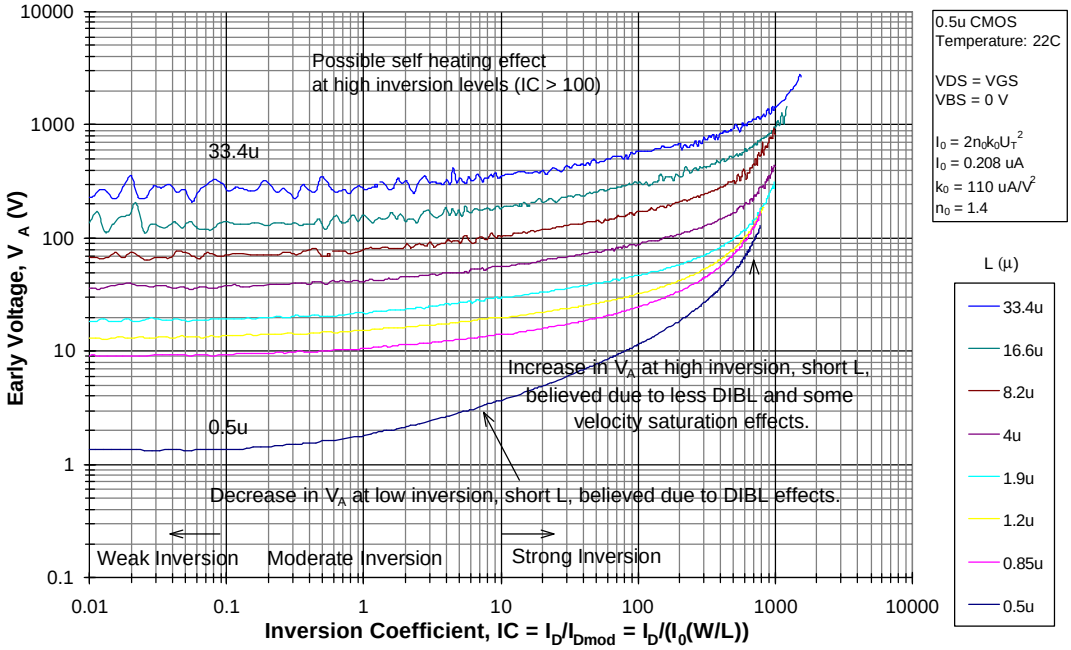

Fig. 2. Measured NMOS Early voltage vs. inversion coefficient from weak through strong inversion for L = 0.5µm - 33.4µm.

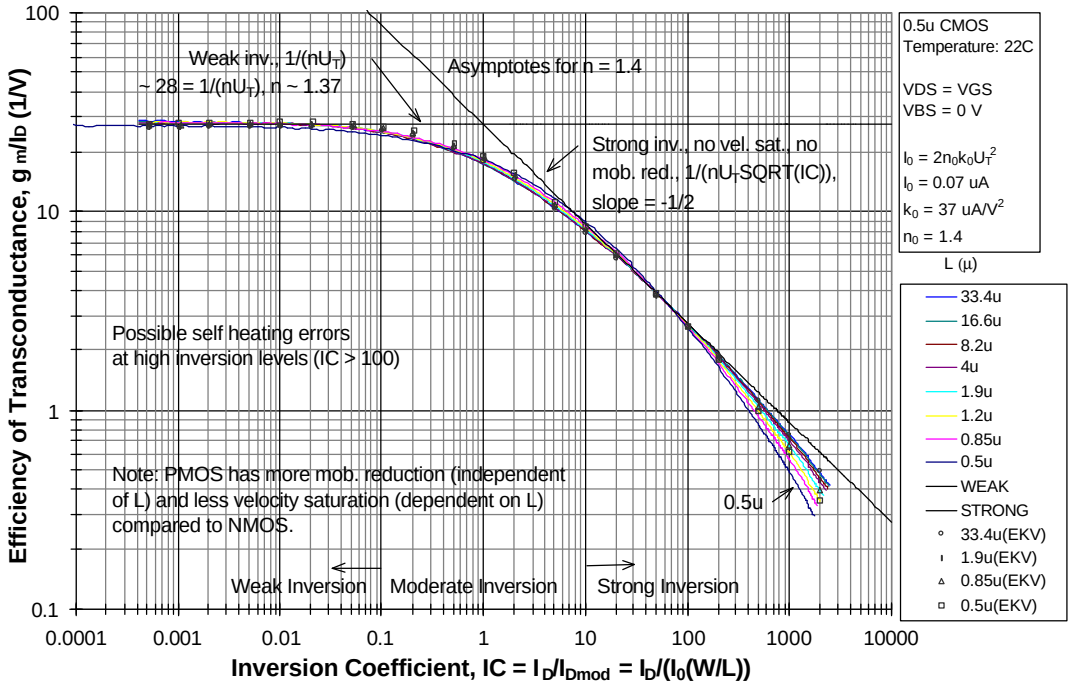

Fig. 3. PMOS g_m/I_D vs. inversion coefficient from weak through strong inversion for L = 0.5µm - 33.4µm. Measurement (lines) and simulation with EKV v2.6 MOS model (markers).

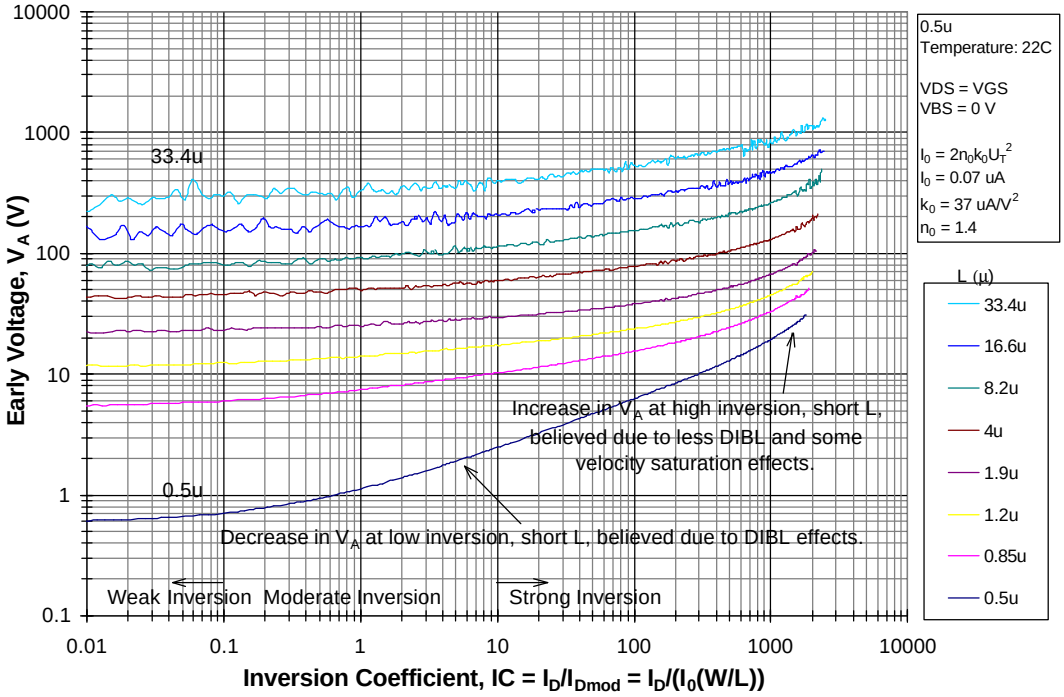

Fig. 4. Measured PMOS Early voltage vs. inversion coefficient from weak through strong inversion for L = 0.5µm - 33.4µm.