Analog Integrated Circuits and Signal Processing, 8, 83–114 (1995)

An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications

CHRISTIAN C. ENZ, FRANÇOIS KRUMMENACHER AND ERIC A. VITTOZ

Swiss Federal Institute of Technology of Lausanne, Electronics Laboratory, EL-Ecublens, CH-1015 Lausanne, Switzerland

enz@leg.de.epfl.ch

Abstract. A fully analytical MOS transistor model dedicated to the design and analysis of low-voltage, low-current analog circuits is presented. All the large- and small-signal variables, namely the currents, the transconductances, the intrinsic capacitances, the non-quasi-static transadmittances and the thermal noise are continuous in all regions of operation, including weak inversion, moderate inversion, strong inversion, conduction and saturation. The same approach is used to derive all the equations of the model: the weak and strong inversion asymptotes are first derived, then the variables of interest are normalized and linked using an appropriate interpolation function. The model exploits the inherent symmetry of the device by referring all the voltages to the local substrate. It is shown that the inversion charge Q'_{inv} is controlled by the voltage difference $V_P - V_{ch}$, where V_{ch} is the channel voltage, defined as the difference between the quasi-Fermi potentials of the carriers. The pinch-off voltage V_P is defined as the particular value of V_{ch} such that the inversion charge is zero for a given gate voltage. It depends only on the gate voltage and can be interpreted as the equivalent effect of the gate voltage referred to the channel. The various modes of operation of the transistor are then presented in terms of voltages $V_P - V_S$ and $V_P - V_D$. Using the charge sheet model with the assumption of constant doping in the channel, the drain current I_D is derived and expressed as the difference between a forward component I_F and a reverse component I_R. Each of these is proportional to a function of $V_P - V_S$, respectively $V_P - V_D$, through a specific current I_S. This function is exponential in weak inversion and quadratic in strong inversion. The current in the moderate inversion region is then modelled by using an appropriate interpolation function resulting in a continuous expression valid from weak to strong inversion. A quasi-static small-signal model including the transconductances and the intrinsic capacitances is obtained from an accurate evaluation of the total charges stored on the gate and in the channel. The transconductances and the intrinsic capacitances are modelled in moderate inversion using the same interpolation function and without any additional parameters. This small-signal model is then extended to higher frequencies by replacing the transconductances by first order transadmittances obtained from a non-quasi-static calculation. All these transadmittances have the same characteristic time constant which depends on the bias condition in a continuous manner. To complete the model, a general expression for the thermal noise valid in all regions of operation is derived. This model has been successfully implemented in several computer simulation programs and has only 9 physical parameters, 3 fine tuning fitting coefficients and 2 additional temperature parameters.

Keywords: MOS transistor, device modeling, low-voltage, low-current

1. Introduction

The performance of analog circuits strongly depends on how the characteristics of the transistors are exploited and mastered. Analog designers therefore need a model of the MOS transistor that is suited not only to final numerical circuit simulation but also to the creative task of exploring new circuits. This model must therefore provide several coherent hierarchical levels, from simple analytical expressions to support creative synthesis, to detailed expressions for precise computer simulation. The model must include a minimal number of independent parameters, all strongly based on physics, in order to keep track of correlations with temperature and process variations.

Analog designs often exploit the functional and structural source-drain symmetry of the transistor. A good model for analog must therefore respect this symmetry. Last and most important is the need to adapt the model to low-voltage and low-current circuits. The

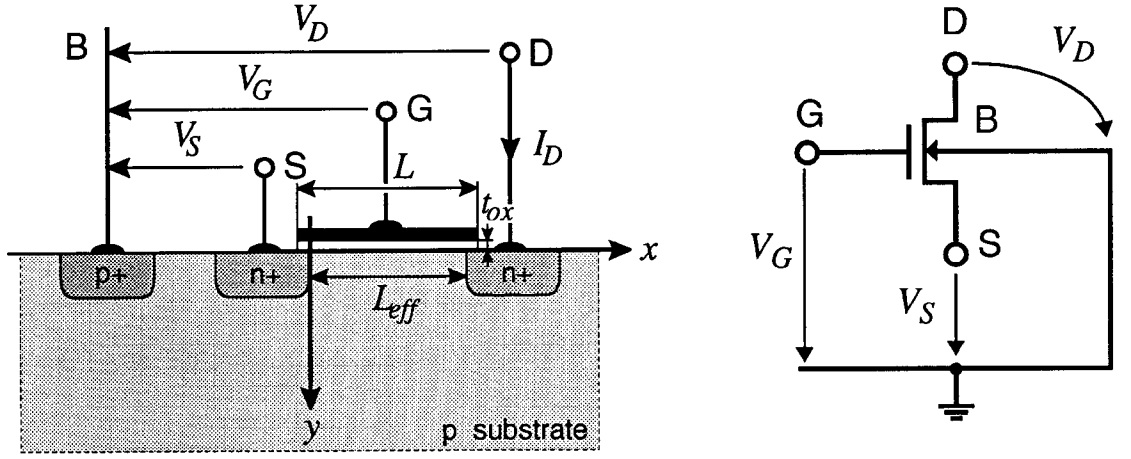


Fig. 1. Cross-section of an idealized n-channel MOS transistor and the corresponding symbol. All voltages are referred to the local p-type substrate.

Table 1. Definitions used in the model.

Symbols	Description	Units
q	Elementary charge	$A \cdot s$
$U_T = (k \cdot T)/q$	Thermodynamic voltage	V
n_i	Intrinsic carrier concentration of Si	m^{-3}
$\varepsilon_s, \varepsilon_{ox}$	Dielectric constant of Si and SiO_2	F/m
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	Gate oxide capacitance per unit area	F/m^2
N_{sub}	Doping concentration of substrate	m^{-3}
$\Phi_F = U_T \cdot ln(N_{sub}/n_i)$	Fermi potential in the substrate	V
V_{FB}	Flat-band voltage	V
$\Psi, \Psi_s = \Psi(y = 0)$	Electrostatic potential and surface potential	V
$V_{ch} = \phi_n - \phi_p = \phi_n - \Phi_F$	Channel potential	V
Q'_{inv}	Mobile inversion charge per unit area	$(A \cdot s)/m^2$
μ_n	Mobility of electrons in the channel	$m^2/(V \cdot s)$

model must therefore describe the behavior of the transistor in a continuous manner from very low currents (weak inversion or subthreshold operation) to large currents.

This paper reports the results of a long and evolutionary coordinated effort to meet these goals [2], [3], [4], [12], [19], [20].

2. Large-Signal Model Formulation

2.1. Definitions

Fig. 1 shows the cross-section and the corresponding symbol of an n-channel MOS transistor. In order to exploit the intrinsic symmetry of the device in the model, the source voltage V_S, the gate voltage V_G and the drain voltage V_D are all referred to the local substrate. This is not the convention adopted for SPICE models for which all potentials are referred to the source electrode. The definitions of the symbols used to derive this model are presented in Table 1.

The *surface potential* Ψ_s is defined as the *electrostatic potential* Ψ at the semiconductor surface ($y = 0$) and the Fermi potential Φ_F as the quasi-Fermi potential of the majority carriers. The *channel potential* V_{ch}, which depends on the position along the channel, is defined as the difference between the quasi-Fermi potential of the carriers forming the channel ϕ_n and the quasi-Fermi potential of the majority carriers ϕ_p. Since

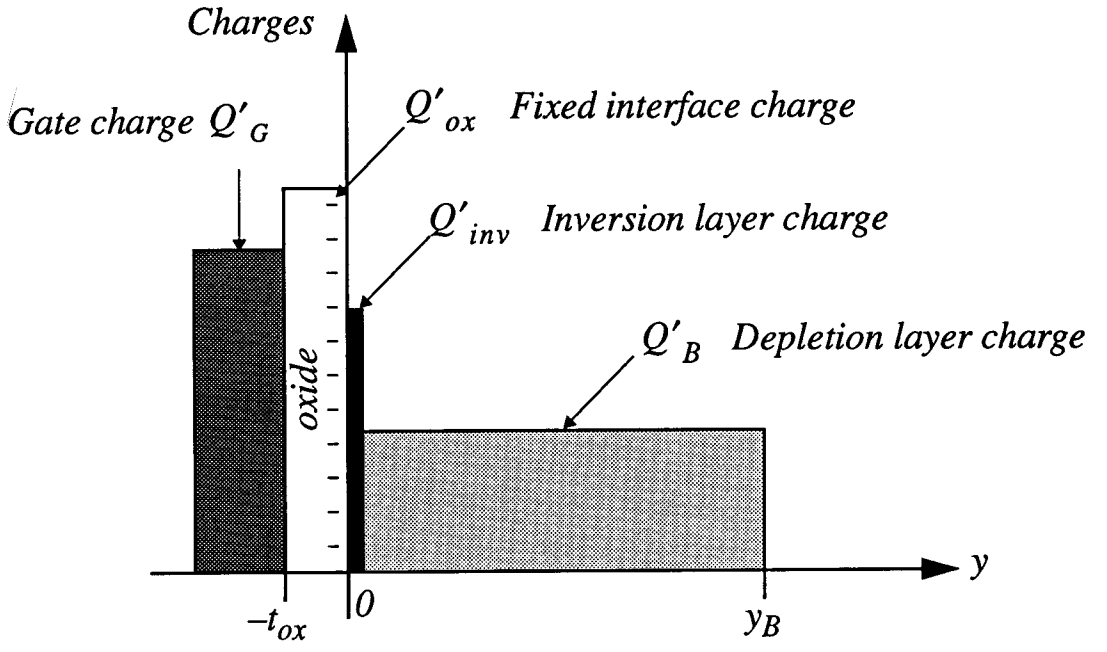


Fig. 2. Charges appearing across the MOS structure.

the current density of majority carriers (holes in the case of an n-channel transistor) is assumed to be negligible in the whole structure, the quasi-Fermi potential of majority carriers ϕ_p is equal to the Fermi potential Φ_F and thus the channel potential is simply equal to the difference $V_{ch} = \phi_n - \Phi_F$. This channel potential represents the disequilibrium in electron distribution produced by the source and the drain voltages.

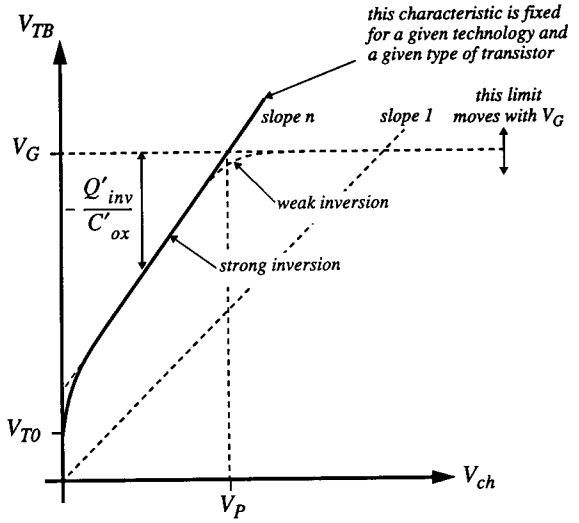


Fig. 3. Representation of the strong inversion threshold voltage V_{TB} and the mobile charge Q'_{inv} versus the channel potential V_{ch} for a given gate voltage V_G [6] [5].

2.2. *Inversion Charge in Strong Inversion and Pinch-Off Voltage Definition*

The different charges appearing across the MOS structure are represented in Fig. 2. The gate charge Q'_G is balanced by the fixed charge Q'_{ox} trapped at the Si-SiO_2 interface, the *inversion charge* Q'_{inv} and the *depletion charge* Q'_B.

The mobile charge density Q'_{inv} can be calculated as a function of Ψ_s and V_{ch} by integrating Poisson's equation. In the inversion region, Ψ_s is much larger than U_T and the mobile charge density Q'_{inv} simplifies to [1], [2]:

$$Q'_{inv} = -\gamma \cdot C'_{ox} \cdot \sqrt{U_T} \cdot \left\{ \sqrt{\frac{\Psi_s}{U_T} + \exp\left[\frac{\Psi_s - 2\Phi_F - V_{ch}}{U_T}\right]} - \sqrt{\frac{\Psi_s}{U_T}} \right\} \tag{1}$$

A relation between Ψ_s and the gate voltage is obtained

by applying Gauss' law:

$$V_G = V_{FB} + \Psi_s + \gamma \cdot \sqrt{\Psi_s} - \frac{Q'_{inv}}{C'_{ox}} \qquad (2)$$

where γ is the *substrate factor* or *body effect factor* defined as:

$$\gamma = \frac{\sqrt{2 \cdot q \cdot \varepsilon_s \cdot N_{sub}}}{C'_{ox}} \qquad (3)$$

The gate voltage can be calculated from the surface potential by using equations (1) and (2).

In *strong inversion*, the surface potential Ψ_s becomes a logarithmic function of the gate voltage and can thus be considered independent of the gate voltage. It can be approximated by a constant $\Psi_0 + V_{ch}$ where $\Psi_0 = 2\Phi_F +$ several U_T. Expressing Q'_{inv} as a function of Ψ_s and V_G using Eqn. 2 and replacing Ψ_s by $\Psi_0 + V_{ch}$ leads to an expression of the inversion charge per unit area valid in strong inversion:

$$Q'_{inv} = -C'_{ox} \cdot [V_G - V_{TB}(V_{ch})] \qquad (4)$$

where V_{TB} is the gate threshold voltage referred to the local substrate and defined as:

$$\begin{aligned} V_{TB} &\equiv V_{FB} + \Psi_0 + V_{ch} + \gamma \cdot \sqrt{\Psi_0 + V_{ch}} \\ &= V_{TO} + V_{ch} + \gamma \cdot \left[\sqrt{\Psi_0 + V_{ch}} - \sqrt{\Psi_0}\right] \end{aligned} \qquad (5)$$

The *threshold voltage* V_{T0} is defined as the gate voltage such as $Q'_{inv} = 0$ when the channel is at equilibrium ($V_{ch} = 0$):

$$\begin{aligned} V_{T0} &\equiv V_G\Big|_{\substack{V_{ch}=0 \\ Q'_{inv}=0}} \\ &= V_{TB}\Big|_{V_{ch}=0} = V_{FB} + \Psi_0 + \gamma \cdot \sqrt{\Psi_0} \end{aligned} \qquad (6)$$

The threshold voltage V_{TB} is plotted in Fig. 3 versus the channel voltage for a given gate voltage according to the representation originally proposed by Memelink [5], [6]. It is important to notice that the V_{TB} versus V_{ch} plot of Fig. 3 almost completely characterizes the technology.

Fig. 3 also shows the inversion charge Q'_{inv}, which for a given gate voltage becomes zero for a particular value of the channel potential V_P defined as the *pinch-off voltage*. The relation between V_P and the gate voltage is obtained from Eqn. 4 by setting Q'_{inv} to zero:

$$\begin{aligned} V_G\Big|_{\substack{V_{ch}=V_P \\ Q'_{inv}=0}} &\equiv V_{TB}|_{V_{ch}=V_P} \\ &= V_{T0} + V_P + \gamma \cdot \left[\sqrt{\Psi_0 + V_P} - \sqrt{\Psi_0}\right] \end{aligned} \qquad (7)$$

Each value of the gate voltage corresponds to a different value of the pinch-off voltage and thus the latter can be expressed in terms of the gate voltage by simply inverting Eqn. 7:

$$\begin{aligned} V_P &= V_G - V_{T0} - \gamma \\ &\cdot \left[\sqrt{V_G - V_{T0} + \left(\sqrt{\Psi_0} + \frac{\gamma}{2}\right)^2} \right. \\ &\left. - \left(\sqrt{\Psi_0} + \frac{\gamma}{2}\right)\right] \end{aligned} \qquad (8)$$

The derivative of the gate voltage with respect to the pinch-off voltage is defined as the *slope factor n* and is given by:

$$n \equiv \frac{dV_G}{dV_P} = 1 + \frac{\gamma}{2 \cdot \sqrt{\Psi_0 + V_P}} \qquad (9)$$

Since V_P depends on V_G, the slope factor can also be expressed directly as a function of V_G:

$$\begin{aligned} \frac{1}{n} &= \frac{dV_P}{dV_G} \\ &= 1 - \frac{\gamma}{2 \cdot \sqrt{V_G - V_{T0} + \left(\frac{\gamma}{2} + \sqrt{\Psi_0}\right)^2}} \end{aligned} \qquad (10)$$

This expression is useful for evaluating n at a certain operating point and for calculating the small-signal parameters presented in section 3.

For the values of γ and Φ_F used in practice, the pinch-off voltage is almost a linear function of the gate voltage. V_P can thus be approximated by:

$$V_P \cong \frac{V_G - V_{T0}}{n(V_G)} \qquad (11)$$

where $n(V_G)$ is evaluated from Eqn. 10.

Introducing the definition of the pinch-off voltage given by Eqn. 8 into Eqn. 4 leads to:

$$\begin{aligned} Q'_{inv} &= -C'_{ox} \cdot [V_P - V_{ch} + \gamma \\ &\cdot \left(\sqrt{\Psi_0 + V_P} - \sqrt{\Psi_0 + V_{ch}}\right)] \end{aligned} \qquad (12)$$

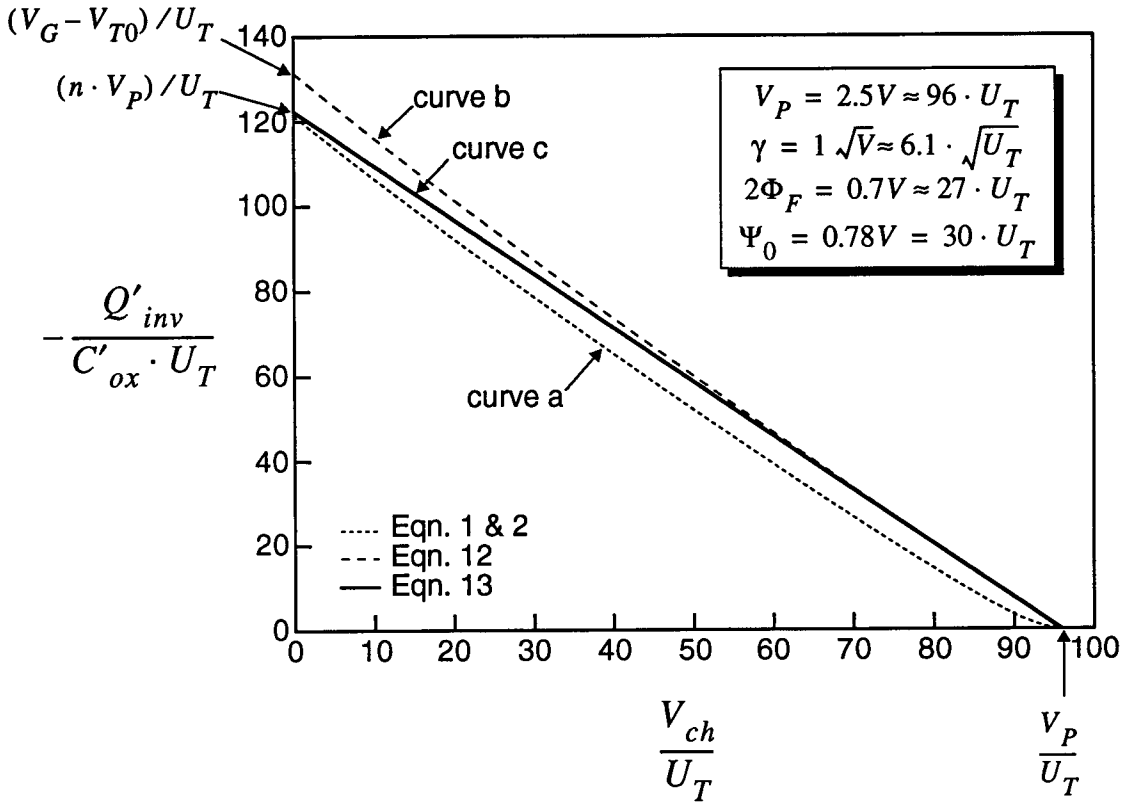


Fig. 4. Inversion charge versus channel potential for a given gate voltage.

Eqn. 12 clearly shows that the pinch-off voltage has the same effect as the channel potential but with an opposite sign. The pinch-off voltage can thus be interpreted as the equivalent effect of the gate voltage referred to the channel. It is important to notice that all the above relations have been developed assuming a *uniform doped substrate*. However, present-day CMOS processes use ion implantation in order to adjust the threshold voltages of the n and p-type devices. To take the effect of the implant into account, the relation between the gate and the pinch-off voltage has to be modified resulting in some additional parameters. There are several ways to include the effect of non-uniform doping that are extensively discussed in the literature and so will not be covered here [1], [7], [8], [9]. In the following derivation it will still be assumed that the doping is uniform.

The inversion charge Q'_{inv} given by Eqn. 12 has been plotted versus the channel potential in Fig. 4 (curve b). It can be compared to the result obtained by using the complete implicit expression given by equations (1) and (2) (curve a). Fig. 4 shows that Eqn. 12 overestimates the inversion charge, which will result in a current slightly higher than that which would be predicted by the complete expression. Curve c represents a linear approximation of the inversion charge Q'_{inv} obtained by taking a first order Taylor series expansion of Eqn. 12 with respect to V_{ch} evaluated at V_P:

$$Q'_{inv} \cong \left.\frac{\partial Q'_{inv}}{\partial V_{ch}}\right|_{V_{ch}=V_P} \cdot (V_{ch} - V_P)$$
$$= -C'_{ox} \cdot n \cdot (V_P - V_{ch}) \qquad (13)$$

This simple approximation, although better than curve b still overestimates the charge and thus the current. The fitting of curve a using Eqn. 13 but considering parameters V_{T0}, γ and Ψ_0 as three independent fitting parameters instead of three correlated "physical" parameters, greatly improves the approximation. In the case of Fig. 4, this would essentially result in a slightly higher value for V_{T0}, moving the crossing point of curve c with the x-axis a little bit to the left. The

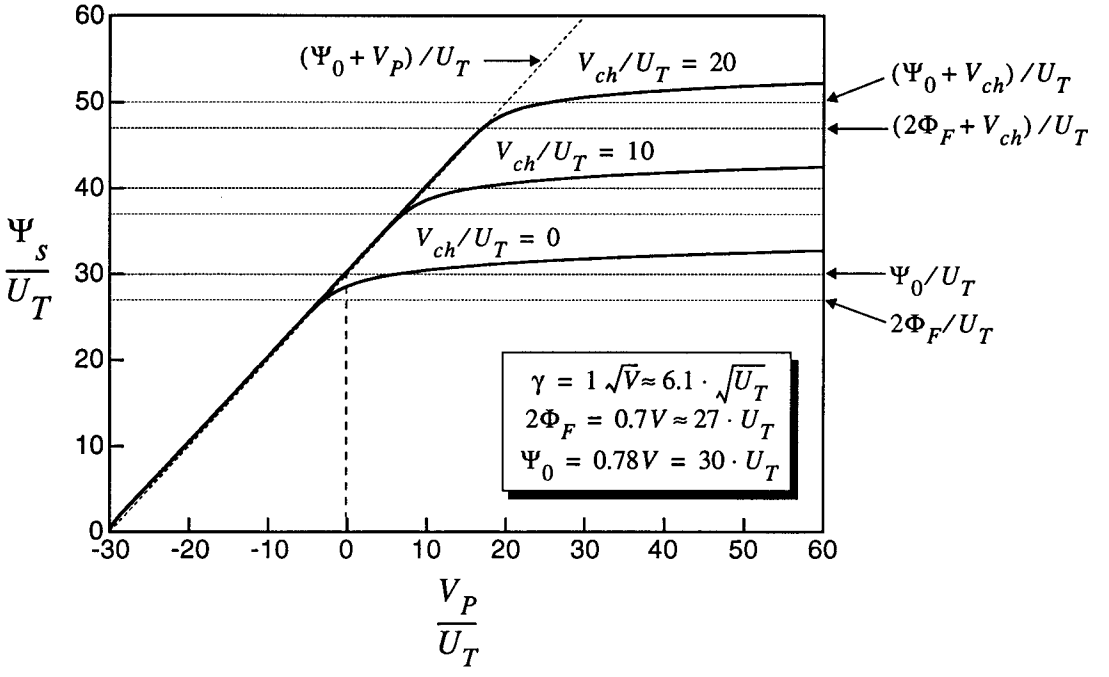


Fig. 5. Surface potential versus pinch-off voltage.

approximation given by Eqn. 13 is thus a good compromise between precision and simplicity.

2.3. *Inversion Charge in Weak Inversion*

The inversion charge Q'_{inv} does not vanish abruptly when V_{ch} reaches V_P, but decays smoothly as the channel leaves strong inversion as shown by curve a on Fig. 4. For V_{ch} somewhat larger than V_P, the channel is in *weak inversion* and the inversion charge becomes negligible with respect to the depletion charge due to the ionized impurities. The relation between the surface potential and the gate voltage is obtained from Eqn. 2 by neglecting the Q'_{inv} term and by introducing the definition of V_{T0}:

$$V_G = V_{T0} + (\Psi_s - \Psi_0) + \gamma \cdot \left(\sqrt{\Psi_s} - \sqrt{\Psi_0}\right) \qquad (14)$$

The pinch-off voltage, which has originally been defined in strong inversion, can also be used in weak inversion to approximate the surface potential. Comparing Eqn. 14 to Eqn. 7 results in:

$$\Psi_s = \Psi_0 + V_P \qquad (15)$$

Instead of representing the surface potential as a function of $V_G - V_{FB}$, as is generally the case, it can be plotted versus the pinch-off voltage as shown in Fig. 5 for different channel potentials. As expected, the surface potential varies linearly with respect to V_P up to $2\Phi_F + V_{ch}$. For V_P larger than V_{ch}, Fig. 5 shows that indeed the surface potential is almost constant in strong inversion. The choice of the value Ψ_0 is arbitrary and depends on the gate voltage range. The surface potential can finally be expressed as:

$$\Psi_s = \begin{cases} \Psi_0 + V_P & \text{for: } V_P < V_{ch} \quad (\textit{weak inversion}) \\ \Psi_0 + V_{ch} & \text{for: } V_P \geq V_{ch} \quad (\textit{strong inversion}) \end{cases} \qquad (16)$$

In weak inversion the surface potential is smaller than $2\Phi_F + V_{ch}$. The exponential term appearing in the general expression of the inversion charge given by Eqn. 1 is thus much smaller than Ψ_s/U_T. The square root can then be expanded into a first order Taylor series leading to a simplified expression of the inversion charge:

$$Q'_{inv} \cong -C'_{ox} \cdot \frac{\gamma}{2 \cdot \sqrt{\Psi_s}} \cdot U_T \cdot e^{\frac{\Psi_s - 2\Phi_F - V_{ch}}{U_T}}$$

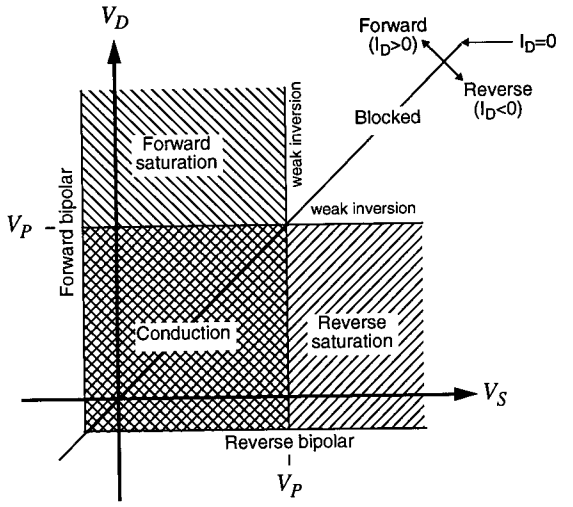


Fig. 6. Modes of operation of the transistor.

$$= -K_w \cdot C'_{ox} \cdot U_T \cdot e^{\frac{V_P - V_{ch}}{U_T}} \tag{17}$$

where K_w is a parameter that depends on the exact value taken for Ψ_0:

$$K_w = (n-1) \cdot e^{\frac{\Psi_0 - 2\Phi_F}{U_T}} \tag{18}$$

2.4. *Modes of Operation*

The different modes of operation of the MOS transistor can be defined according to the source and drain voltages with respect to the pinch-off voltage, as illustrated schematically in Fig. 6.

Symmetrical forward and reverse modes are possible, depending on the sign of $V_D - V_S$. For V_S and V_D both smaller than V_P , the channel is in strong inversion from the source to the drain and the transistor is in the *conduction* mode. If V_D is increased beyond V_P, the drain end of the channel is pinched-off and the device is in *forward saturation* mode. If V_S and V_D are both larger than V_P, the whole channel is pinched-off. The device operates in *weak inversion* as long as one of the source or drain voltage is still close to V_P, but becomes *blocked* if both of them are sufficiently larger than V_P.

If the drain or (and) the source junction is (are) forward biased beyond a junction voltage V_J, a bipolar mode is superimposed on the MOS mode [12][13].

There is of course no abrupt limit between these various modes, but rather smooth transitions. In particular weak and strong inversion are separated by a region of moderate inversion [1].

2.5. *General Expression for the Drain Current*

A general expression for the drain current that includes both the diffusion and the drift mechanisms is given by [1][10][11]:

$$I_D = W \cdot \mu_n \cdot (-Q'_{inv}) \cdot \frac{dV_{ch}}{dx} \tag{19}$$

where it has been assumed that the mobility μ_n is constant along the y axis. As shown in Fig. 7, the drain current is then obtained simply by integrating Eqn. 19 from the source, where $V_{ch} = V_S$ to the drain, where $V_{ch} = V_D$. Assuming that the mobility is also independent of x, this yields:

$$I_D = \beta \cdot \int_{V_s}^{V_D} \left[\frac{-Q'_{inv}(V_{ch})}{C'_{ox}} \right] \cdot dV_{ch} \tag{20}$$

where:

$$\beta = \mu_n \cdot C'_{ox} \cdot \frac{W}{L} \tag{21}$$

The drain current can be decomposed into a *forward current* I_F which depends only on the difference $V_P - V_S$ and a *reverse current* I_R which depends only on

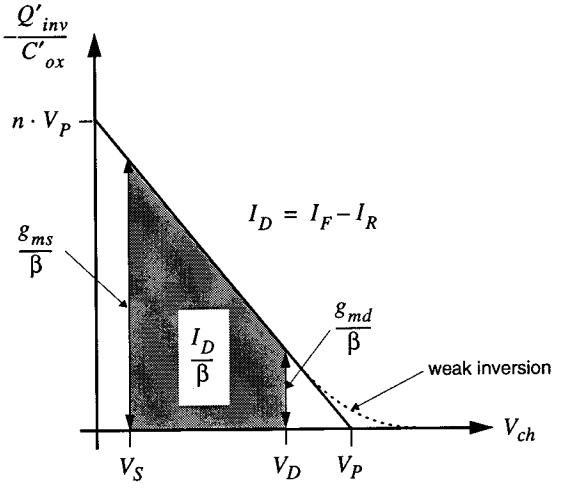


Fig. 7. Inversion charge versus the channel potential. The drain current is proportional to the shaded surface.

$V_P - V_D$ [11]:

$$I_D = \underbrace{\beta \cdot \int_{V_S}^{\infty} \left[-\frac{Q'_{inv}(V_{ch})}{C'_{ox}} \right] \cdot dV_{ch}}_{= I_F \text{ forwardcurrent}} - \underbrace{\beta \cdot \int_{V_D}^{\infty} \left[-\frac{Q'_{inv}(V_{ch})}{C'_{ox}} \right] \cdot dV_{ch}}_{= I_R \text{ reverse current}}$$

$$= I_F - I_R \tag{22}$$

Note that no assumption has been made on the mode of operation of the transistor and so Eqn. 22 is valid in all regions of operation including weak, moderate and strong inversion.

2.6. *Drain Current in Strong and in Weak Inversion*

The drain current in strong inversion is simply obtained by integrating Eqn. 13 which leads to the following expressions of the forward and reverse currents:

$$I_F = \begin{cases} \frac{n \cdot \beta}{2} \cdot (V_P - V_S)^2 & \text{for: } V_S < V_P \\ 0 & \text{for: } V_S \geq V_P \end{cases}$$

$$I_R = \begin{cases} \frac{n \cdot \beta}{2} \cdot (V_P - V_D)^2 & \text{for: } V_D < V_P \\ 0 & \text{for: } V_D \geq V_P \end{cases} \tag{23}$$

The same integration can be done to obtain the current in weak inversion:

$$I_F = K_w \cdot \beta \cdot U_T^2 \cdot e^{\frac{V_P - V_S}{U_T}}$$

$$I_R = K_w \cdot \beta \cdot U_T^2 \cdot e^{\frac{V_P - V_D}{U_T}} \tag{24}$$

All the expressions for the drain current are given in Table 2. The current in reverse saturation is not shown, but can be obtained by simply replacing V_S by V_D in the expression valid in the forward saturation region. The pinch-off voltage V_P can be evaluated from the gate voltage by using the approximation given by Eqn. 11 where n is calculated using Eqn. 10, or by using the complete expression given by Eqn. 8.

2.7. *Drain Current Normalization and Interpolation between Weak and Strong Inversion*

Expressions for the drain current have been derived in the asymptotic modes of operation defined as weak and strong inversion, but they are not valid in the moderate inversion region. A model valid in all regions of operation can be established from physical consideration by evaluating the surface potential either by iteration [1][14] or by using a better approximation than the simple constant used previously [15]. Unfortunately, these models are generally complicated, give rise to numerical problems and are therefore not suitable for simulation. An alternative is to use a so called semiempirical model where the different regions of operation of the device are described by different equations [16][17]. These models represent a good compromise between accuracy and complexity and therefore speed of simulation. In any case, for the model to be acceptable to a circuit simulator, the equations and their first derivatives must be continuous in the whole domain of operation [12].

The model presented hereafter is obtained by properly interpolating the current between the two known asymptotic regions, using an adequate continuous function. Before finding this interpolation function, the current has to be normalized to obtain a relation between the current and the voltages that is independent of the transistor sizes and of the technological parameters. To take into account the proportionality factors $n \cdot \beta$ and $\beta \cdot U_T^2$ that appear in the expressions of the current valid respectively in strong and in weak inversion, the *specific current* I_S can be used:

$$I_S \equiv 2 \cdot n \cdot \beta \cdot U_T^2 \tag{25}$$

The specific current I_S depends essentially on the W/L of the device and on the mobility μ_n. As shown in Fig. 8, it corresponds in fact to the cross-point of the weak and strong inversion asymptotes of the normalized source transconductance plotted versus the drain current. Choosing I_S as the normalization current implies:

$$K_w = 2 \cdot n \tag{26}$$

From Eqn. 18, this corresponds to a certain value of Ψ_0 slightly greater than $2\Phi_F$.

The voltages are simply normalized to the thermodynamic voltage U_T:

$$v_p \equiv \frac{V_P}{U_T} \qquad v_s \equiv \frac{V_S}{U_T} \qquad v_d \equiv \frac{V_D}{U_T} \tag{27}$$

The normalized current in weak and in strong inversion

Table 2. Drain current in strong and in weak inversion.

Mode	Weak Inversion	Strong Inversion
Conduction	$K_w \cdot \beta \cdot U_T^2 \cdot e^{V_P/U_T} \cdot \left[e^{-V_S/U_T} - e^{V_D/UT}\right]$ for: $\begin{cases} V_S > V_P \\ V_D > V_P \\ V_S \cong V_D \end{cases}$	$n \cdot \beta \cdot \left[V_P - \frac{V_S+V_D}{2}\right] \cdot (V_D - V_S)$ for: $\begin{cases} V_S \leq V_P \\ V_D \leq V_P \end{cases}$
Forward Saturation	$K_w \cdot \beta \cdot U_T^2 \cdot e^{\frac{V_P-V_S}{U_T}}$ for: $\begin{cases} V_S > V_P \\ V_D > V_P \\ V_D - V_S \gg U_T \end{cases}$	$\frac{n \cdot \beta}{2} \cdot (V_P - V_S)^2$ for: $\begin{cases} V_S \leq V_P \\ V_D > V_P \end{cases}$
Blocked	0 for: $\begin{cases} V_S \gg V_P \\ V_D \gg V_P \end{cases}$ or $V_S = V_D$	0 for: $\begin{cases} V_S > V_P \\ V_D > V_P \end{cases}$

can be expressed as:

$$i_d \equiv \frac{I_D}{I_S} = i_f - i_r = F(v_p - v_s) - F(v_p - v_d) \quad (28)$$

where $i_f \equiv I_F/I_S$ is the *forward normalized current* which is also defined as the *inversion coefficient* and $i_r \equiv I_R/I_S$ is the *reverse normalized current*. Function $F(v)$ is the interpolation function, which should have the following asymptotes:

$$F(v) = \begin{cases} \left(\frac{v}{2}\right)^2 & \text{for: } v \gg 0 \\ e^v & \text{for: } v \ll 0 \end{cases} \quad (29)$$

A good and simple interpolation has originally been proposed by H. Oguey and S. Cserveny [19][20] and has been simplified in order to remove the additional fitting coefficients:

$$F(v) = [ln(1 + e^{v/2})]^2 \quad (30)$$

The forward and reverse normalized currents are then given by:

$$\begin{aligned} i_f &= F(v_p - v_s) = \left[ln\left(1 + e^{\frac{v_p - v_s}{2}}\right)\right]^2 \\ i_r &= F(v_p - v_d) = \left[ln\left(1 + e^{\frac{v_p - v_d}{2}}\right)\right]^2 \end{aligned} \quad (31)$$

These functions can be conveniently inverted to express the voltages in terms of the forward or reverse currents as it is generally required in analog circuit design:

$$\begin{aligned} v_p - v_s &= 2 \cdot ln\left(e^{\sqrt{i_f}} - 1\right) \\ v_p - v_d &= 2 \cdot ln\left(e^{\sqrt{i_r}} - 1\right) \end{aligned} \quad (32)$$

A better interpolation function can be obtained by integration of the small-signal transconductance interpolation function given by Eqn. 39. The detailed calculation of the resulting interpolation function is presented in Appendix A1.

3. Small-Signal Quasi-Static Model

3.1. *Transconductances in Weak and in Strong Inversion*

The total change in the drain current due to small variations of the gate, source and drain voltages is given by:

$$\Delta I_D = \underbrace{\left.\frac{\partial I_D}{\partial V_G}\right|_{V_S, V_D}}_{=g_{mg}} \cdot \Delta V_G + \underbrace{\left.\frac{\partial I_D}{\partial V_S}\right|_{V_G, V_D}}_{=-g_{ms}} \cdot \Delta V_S + \underbrace{\left.\frac{\partial I_D}{\partial V_D}\right|_{V_G, V_S}}_{=g_{md}} \cdot \Delta V_D \quad (33)$$

where g_{mg}, g_{ms} and g_{md} are respectively the *gate*, *source* and *drain* transconductances. The correspondence with the transconductances defined when referring all voltages to the source electrode are given hereafter:

$$\begin{aligned} g_m &\equiv \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{BS}, V_{DS}} = g_{mg} \\ g_{mb} &\equiv \left.\frac{\partial I_D}{\partial V_{BS}}\right|_{V_{GS}, V_{DS}} = g_{ms} - g_{mg} - g_{md} \end{aligned}$$

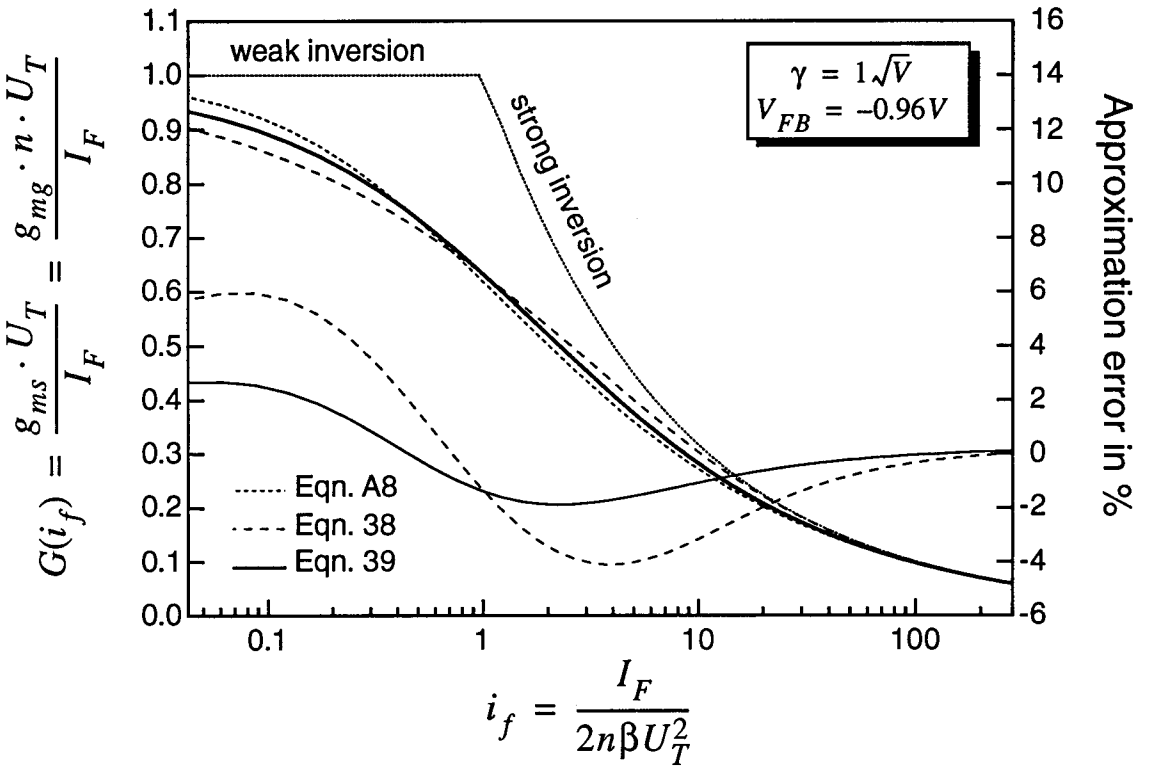


Fig. 8. Transconductance interpolation functions.

$$g_{ds} \equiv \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS},V_{BS}} = g_{md} \tag{34}$$

The value of the transconductances in strong and in weak inversion can be calculated respectively from Eqn. 23 and Eqn. 24. They are summarized in Table 3. Source and gate transconductances in saturation are proportional to the drain current when the transistor is biased in weak inversion and proportional to the square root of the drain current in strong inversion.

Since the variation of the pinch-off voltage is n times smaller than the corresponding gate voltage variation and the forward current depends only on the voltage difference $V_P - V_S$, the gate transconductance in saturation (i.e. for $I_R = 0$) is n times smaller than the source transconductance:

$$\begin{aligned} g_{mg}|_{I_R=0} &= \left.\frac{\partial I_F}{\partial V_G}\right|_{V_S} = \frac{1}{n}\cdot\left.\frac{\partial I_F}{\partial V_P}\right|_{V_S} \\ &= \frac{1}{n}\cdot\left(-\left.\frac{\partial I_F}{\partial V_S}\right|_{V_G}\right) = \frac{g_{ms}}{n} \end{aligned} \tag{35}$$

This relation is true in saturation from weak to strong inversion.

3.2. *Transconductance Normalization and Interpolation between Weak and Strong Inversion*

In order to obtain an interpolation function that is independent of the transistor's size, the transconductances in saturation can be normalized to their maximum value which is reached in weak inversion. They can then be written in terms of the normalized forward or reverse current using the same interpolation function $G(i)$:

$$\begin{aligned} \frac{g_{mg}\cdot n\cdot U_T}{I_F} &= \frac{g_{ms}\cdot U_T}{I_F} = G(i_f) \\ \frac{g_{md}\cdot U_T}{I_R} &= G(i_r) \end{aligned} \tag{36}$$

Function $G(i)$ should be continuous and have the following asymptotes:

Table 3. Transconductances in strong and in weak inversion.

	Strong Inversion		Weak Inversion
	Conduction	Forward Saturation	
g_{mg}	$\beta \cdot (V_P - V_S) = \sqrt{\frac{2 \cdot \beta \cdot I_F}{n}}$	$\frac{I_D}{n \cdot U_T}$	
g_{ms}	$n \cdot \beta \cdot (V_P - V_S) = \sqrt{2 \cdot n \cdot \beta \cdot I_F}$	$n \cdot \beta \cdot (V_P - V_S) = \sqrt{2 \cdot n \cdot \beta \cdot I_F}$	$\frac{I_F}{U_T}$
g_{md}	$n \cdot \beta \cdot (V_P - V_D) = \sqrt{2 \cdot n \cdot \beta \cdot I_R}$	O	$\frac{I_R}{U_T}$

$$G(i) = \begin{cases} 1 & \text{for: } i \ll 1 \quad (\textit{weak inversion}) \\ 1/\sqrt{i} & \text{for: } i \gg 1 \quad (\textit{strong inversion}) \end{cases} \tag{37}$$

This function can be derived from the large-signal interpolation function given by Eqn. 31:

$$\begin{aligned} G(i_f) &= -\frac{U_T}{I_F} \cdot \frac{\partial I_F}{\partial V_S}\bigg|_{V_G} \\ &= -\frac{1}{i_f} \cdot \frac{\partial i_f}{\partial v_s}\bigg|_{v_s} \\ &= \frac{1}{i_f} \cdot \frac{dF(v)}{dv} = \frac{1 - e^{-\sqrt{i_f}}}{\sqrt{i_f}} \end{aligned} \tag{38}$$

This function is plotted versus the forward normalized current in Fig. 8. It can be compared to the exact result obtained from the numerical evaluation of the inversion charge and of the current as derived in Appendix A2. It tends to overestimate the exact result in strong inversion, while it underestimates in weak inversion. The approximation error is less than 6% for $\gamma = 1\sqrt{V}$. A better and simpler interpolation function is given by:

$$G(i_f) = \frac{1}{\sqrt{i_f + \frac{1}{2} \cdot \sqrt{i_f} + 1}} \tag{39}$$

The error corresponding to this interpolation is less than 3% for γ ranging from $0.5\sqrt{V}$ to $2\sqrt{V}$. It is therefore better than the interpolation function given by Eqn. 38. Due to its precision and inherent simplicity, it has been chosen for the computer simulation model. In order to obtain the large-signal current interpolation function corresponding to the transconductances, Eqn. 39 can be integrated to express the normalized voltage as a function of the normalized current (cf. Appendix A1). Unfortunately, the resulting function is rather complicated and cannot be inverted to express the current in terms of the voltage. This has little consequences in the case of computer simulation model where the large-signal function can be tabulated. Furthermore, in some circuit simulators the derivatives are calculated numerically instead of using an analytic expression. In such a case, the use of a large-signal interpolation function derived from Eqn. 39 ensures a good approximation of the transconductances.

3.3. *Experimental Results*

The gate and source transconductances of a long and wide transistor ($W = L = 100\ \mu$m) have been measured. The I_D/g_{mg} ratio is plotted versus the drain current in Fig. 9a) for two different source-to-bulk voltages $V_S = 0$ and $V_S = 2$ V. It is compared to the simple analytical formulation derived from equations (36) and (39):

$$\begin{aligned} \frac{I_D}{g_{mg}} &= \frac{n \cdot U_T}{G(i_f)} \\ &= n \cdot U_T \cdot \sqrt{i_f + \frac{1}{2} \cdot \sqrt{i_f} + 1} \quad (\textit{saturation}) \end{aligned} \tag{40}$$

Good agreement is observed between the experimental and the analytical results. The variation of the I_D/g_{mg} ratio with the source voltage observed in Fig. 9a) at low current, is due to a variation of the slope factor n. At a fixed drain current, the pinch-off voltage follows the source voltage, which causes the slope factor to vary. The difference between the slope factor for $V_S = 0$ and $V_S = 2$ V is dominant in weak inversion and since n tends to unity for large V_P (or V_G), the two curves shown in Fig. 9a) merge in strong inversion.

Similarly, Fig. 9 b) shows the measured I_D/g_{ms} ratio, plotted versus the drain current for two different

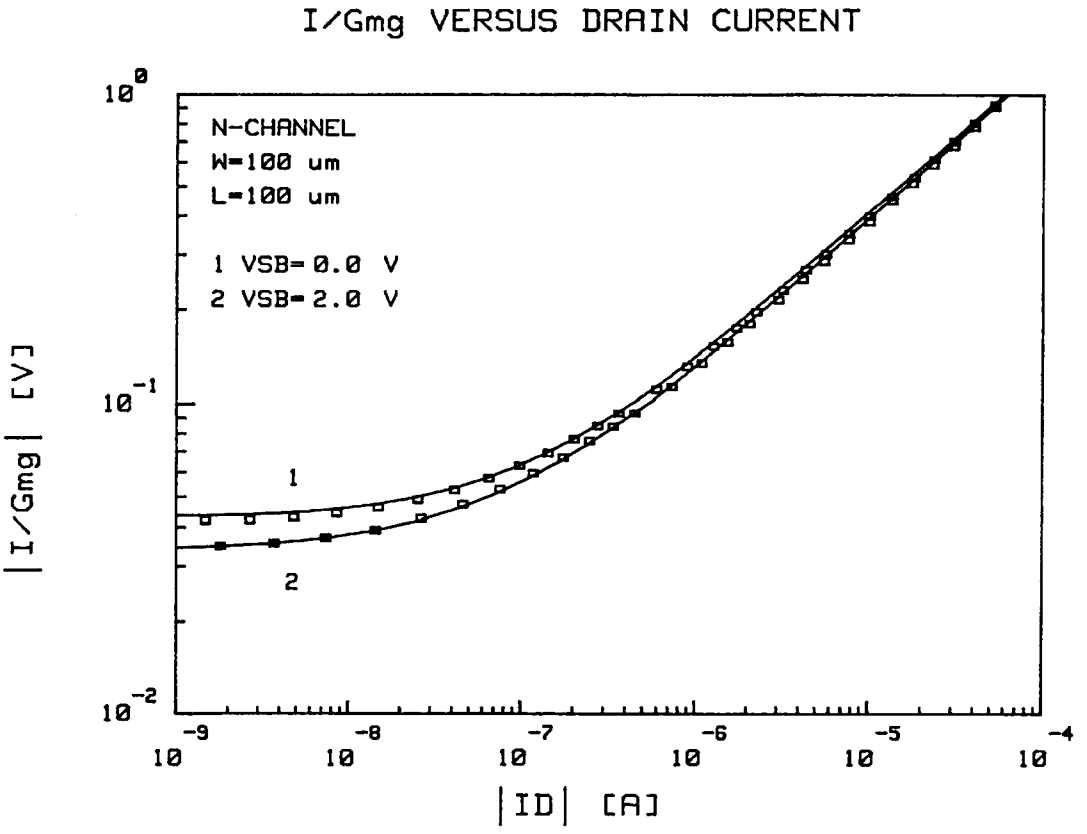


Fig. 9. (a) Saturation current to gate transconductance ratio versus drain current measured from weak to strong inversion.

gate voltages $V_G = 1$ V and $V_G = 4$ V. A good agreement is observed between the experimental data and the analytical formula given by:

$$\frac{I_D}{g_{ms}} = \frac{U_T}{G(i_f)} = U_T \cdot \sqrt{i_f + \frac{1}{2} \cdot \sqrt{i_f} + 1} \qquad (41)$$

The difference between the I_D/g_{ms} ratio measured at $V_G = 1$ V and $V_G = 4$ V that is observed at high current is also caused by a change in the slope factor n. For $V_{G1} > V_{G2}$, the corresponding slope factor n_1 and the specific current I_{S1} are smaller than n_2 and I_{S2} respectively. This implies that for a given drain current I_D, the I_D/g_{ms} ratio is larger for inversion coefficient i_{f1} than for i_{f2}.

3.4. *Quasi-Static Model for the Intrinsic Capacitances*

The operation of the MOS transistor is mainly controlled by the region between source and drain which contains the inversion layer, the depletion region, the oxide and the gate plate. This region constitutes the *intrinsic* part, while the rest of the device is called the *extrinsic* part and is responsible for parasitic effects. Assuming quasi-static operation, the effect of external time varying potentials can be analyzed by evaluating the variation of the different charges present in the intrinsic part. For medium frequency, only the global change of these charges is taken into account. In the simple quasi-static model developed hereafter, the distributed nature of the coupling between the gate, the inversion layer and the bulk will be ignored. A first-order non-quasi-static model is presented in the next section.

The dynamic behavior of the intrinsic MOS is de-

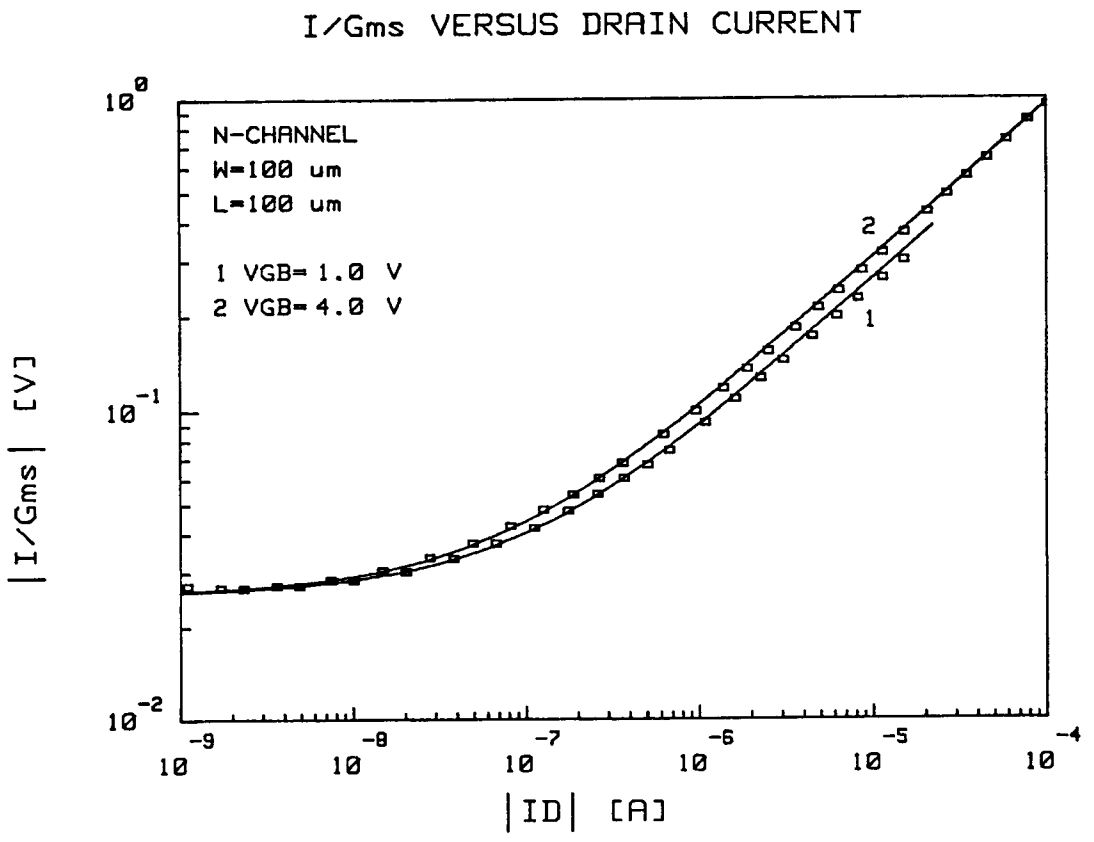


Fig. 9. (b) Saturation current to source transconductance ratio versus drain current measured from weak to strong inversion.

scribed by the variation of the total charges Q_G, Q_B and Q_{inv} stored respectively on the gate, in the bulk and in the channel. These charges are obtained by integration along the channel from source to drain:

$$Q_{inv} = W \cdot \int_0^L Q'_{inv}(x) \cdot dx$$

$$= -\frac{W^2 \cdot \mu_n}{I_D} \cdot \int_{V_S}^{V_D} [Q'_{inv}(V_{ch})]^2 \cdot dV_{ch} \quad (42)$$

$$Q_B = W \cdot \int_0^L Q'_B(x) \cdot dx$$

$$= -\frac{W^2 \cdot \mu_n}{I_D} \cdot \int_{V_S}^{V_D} Q'_B \cdot Q'_{inv} \cdot dV_{ch} \quad (43)$$

$$Q_G = -Q_{inv} - Q_B - Q_{ox} \quad (44)$$

where Eqn. 19 has been used to express dx in terms of I_D, Q'_{inv}, and dV_{ch}. The medium frequency quasi-static variations of the previously defined charges can be modelled by the simple circuit presented in Fig. 10. In addition to the gate, source and drain transconductances accounting for the low-frequency variations of the drain current, the equivalent small-signal circuit of Fig. 10 includes five different capacitors modeling the transient currents at each terminal of the device that are necessary to change the global charges Q_G, Q_B and Q_{inv}.

Since the charge stored on the gate is totally isolated from the conducting channel, capacitances between the gate and the other terminals are preferably defined using the variation ΔQ_G of this charge with respect to variations of the terminal voltages ΔV_S, ΔV_D and ΔV_B:

$$C_{gs} \equiv -\frac{\Delta Q_G}{\Delta V_S} = -\left.\frac{\partial Q_G}{\partial V_S}\right|_{V_G, V_B, V_D}$$

$$C_{gd} \equiv -\frac{\Delta Q_G}{\Delta V_D} = -\left.\frac{\partial Q_G}{\partial V_D}\right|_{V_G, V_B, V_S} \quad (45)$$

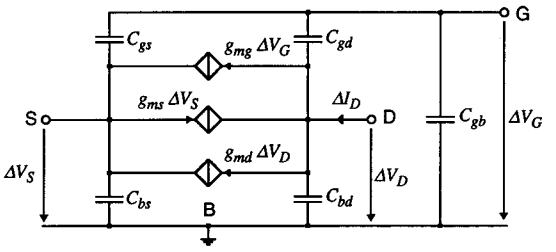


Fig. 10. Medium frequency small-signal equivalent circuit.

$$C_{gb} \equiv -\frac{\Delta Q_G}{\Delta V_G} = -\left.\frac{\partial Q_G}{\partial V_B}\right|_{V_G,V_S,V_D} \tag{46}$$

C_{gb} can equivalently be defined in terms of C_{gs} and C_{gd} by considering that an increase of the bulk voltage with respect to an external potential is equivalent to a simultaneous decrease of the gate, source and drain voltages, keeping the bulk voltage constant. The gate charge variation for $\Delta V_G = \Delta V_S = \Delta V_D = -\Delta V_B$ is then given by:

$$\Delta Q_G = \left(C_{gs} + C_{gd} - \left.\frac{\partial Q_G}{\partial V_G}\right|_{V_B,V_S,V_D}\right) \cdot \Delta V_B \tag{47}$$

and thus:

$$\begin{aligned} C_{gb} &= \left.\frac{\partial Q_G}{\partial V_G}\right|_{V_B,V_S,V_D} - C_{gs} - C_{gd} \\ &= \frac{1}{n} \cdot \left.\frac{\partial Q_G}{\partial V_P}\right|_{V_B,V_S,V_D} - C_{gs} - C_{gd} \end{aligned} \tag{48}$$

In a similar way, the bulk-to-source and bulk-to-drain capacitances are defined by considering a variation ΔQ_B of the bulk charge due respectively to a variation of the source voltage ΔV_S and of the drain voltage ΔV_D:

$$\begin{aligned} C_{bs} &\equiv -\frac{\Delta Q_B}{\Delta V_S} = -\left.\frac{\partial Q_B}{\partial V_S}\right|_{V_G,V_B,V_D} \\ C_{bd} &\equiv -\frac{\Delta Q_b}{\Delta V_D} = -\left.\frac{\partial Q_B}{\partial V_D}\right|_{V_G,V_B,V_S} \end{aligned} \tag{49}$$

A detailed quasi-static analysis shows that the previously defined capacitances are non-reciprocal and therefore that $C_{kl} \neq C_{lk}$. This means that in general the charge variation occurring at node k due to a change of voltage at node l is not equal to the variation of charge at node l due to a change of voltage at node k. To take this non-reciprocity into account, the equivalent model of Fig. 10 should be completed by five transcapacitances, accounting for the currents flowing in the channel due to a variation of the division of the global inversion charge between source and drain. In strong inversion, two of the transcapacitances are zero and the three remaining are connected between source and drain and are proportional to the time derivatives of voltages V_G, V_S and V_D. They can be combined with the transconductances to make three transadmittances proportional to their respective transconductances and to a common factor $1 - (s \cdot \tau)$. From the non-quasi-static analysis presented in section 4, it turns out that this common term corresponds to a first order approximation of the non-quasistatic transadmittances derived in section 4 and having the same characteristic time constant τ (equations (76), (90) and (91)). For this reason and in order to maintain a simple model, the transcapacitances will be ignored in this quasi-static analysis. Their effect will be taken into account in the more accurate non-quasi-static model presented in section 4. Since the non-quasi-static model is derived from transistors operating in the conduction region, it is important to notice that for $V_D = V_S$, all the transcapacitances vanish, leaving only the transconductances and the capacitances, as shown in Fig. 10.

A general relation between capacitances C_{bs} and C_{gs} can be derived from the equivalent circuit of Fig. 10, by first considering only the transient currents flowing through the source and the drain terminals which are charging or discharging the capacitances connected to them [2][21]. Let Q_S be defined as the total charge stored on the source side of capacitances C_{gs} and C_{bs} and Q_D the total charge stored on the drain electrode of capacitances C_{gd} and C_{bd}.

Consider now the effect of a small variation in the gate potential, while keeping the source and drain potential fixed. As illustrated in Fig. 11, a positive charge $+C_{gs} \cdot \Delta V_G$ will now flow through the gate electrode

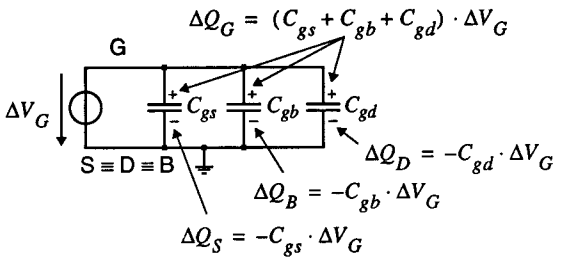


Fig. 11. Effect of a gate potential variation.

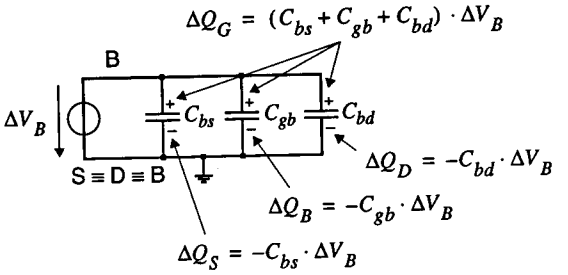


Fig. 12. Effect of a bulk potential variation.

to the top plate of capacitor C_{gs} and a negative charge $\Delta Q_S = -C_{gs} \cdot \Delta V_G$ will come to the bottom plate of capacitor C_{gs}. Therefore C_{gs} can also be expressed as:

$$C_{gs} = -\frac{\Delta Q_S}{\Delta V_G} = -\left.\frac{\partial Q_S}{\partial V_G}\right|_{V_B.V_S.V_D} \tag{50}$$

Let 's repeat the above experiment, but this time imposing a bulk voltage variation while keeping other potentials constant, as illustrated in Fig. 12. Looking at the variation of the charge stored on the source electrode yields another definition of capacitor C_{bs}:

$$C_{bs} = -\frac{\Delta Q_S}{\Delta V_B} = -\left.\frac{\partial Q_S}{\partial V_B}\right|_{V_G.V_S.V_D} \tag{51}$$

The sum of the variations ΔQ_S and ΔQ_D of the source and drain charges represent in fact the change ΔQ_{inv} of the total inversion charge. Since the inversion charge Q'_{inv} in both strong and weak inversion is a function of $V_P - V_{ch}$, Q_{inv} and therefore ΔQ_S and ΔQ_D are also functions of $V_P - V_S$ and $V_P - V_D$. Consequently, the effect of a source voltage increase on the source charge is equivalent to the decrease in the gate voltage multiplied by the slope factor n:

$$\frac{\partial Q_S}{\partial V_S} = -\frac{\partial Q_S}{\partial V_P} = -\frac{\partial Q_S}{\partial V_G} \cdot \frac{dV_G}{dV_P} = -n \cdot \frac{\partial Q_S}{\partial V_G} \tag{52}$$

On the other hand, an increase in the bulk voltage, keeping all other voltages constant, has the same effect as a simultaneous decrease in the gate, source and drain voltages, keeping the bulk voltage constant. In other terms, the variation of the source charge due to ΔV_B is equivalent to a simultaneous variation $\Delta V_G = \Delta V_S = \Delta V_D = -\Delta V_B$:

$$\left.\frac{\partial Q_S}{\partial V_B}\right|_{V_G.V_S.V_D} = -\left.\frac{\partial Q_S}{\partial V_G}\right|_{V_B.V_S.V_D} - \left.\frac{\partial Q_S}{\partial V_S}\right|_{V_G.V_B.V_D} \tag{53}$$

Replacing the partial derivatives by the definitions of capacitors C_{gs} and C_{bs}, given by equations (50) and (51), and combining with Eqn. 52 leads to:

$$C_{bs} = (n-1) \cdot C_{gs} \tag{54}$$

The same relation holds for C_{gd} and C_{bd}:

$$C_{bd} = (n-1) \cdot C_{gd} \tag{55}$$

The bulk-to-source (bulk-to-drain) capacitance is therefore n-1 times the gate-to-source (gate-to-drain) capacitance. Note that equations (54) and (55) were derived only by using the equivalent model of Fig. 10 and the relation between a source charge increase due to a source voltage variation and its equivalent gate voltage action. Therefore equations (54) and (55) are valid in all regions of operation. Finally, all the capacitances can be calculated from the partial derivatives of the gate charge, according to equations (45), (48), (54) and (55).

3.5. *Intrinsic Capacitances in Strong Inversion*

The total charge forming the channel can be calculated using equations (13) and (42):

$$Q_{inv} = -n \cdot U_T \cdot C_{ox} \cdot \frac{4}{3} \cdot \frac{i_f + \sqrt{i_f \cdot i_r} + i_r}{\sqrt{i_f} + \sqrt{i_r}} \tag{56}$$

where C_{ox} is the total gate capacitance given by:

$$C_{ox} = W \cdot L \cdot C'_{ox} \tag{57}$$

i_f and i_r are the normalized currents which in strong inversion are given by:

$$i_f = \left(\frac{V_P - V_S}{2U_T}\right)^2$$

$$i_r = \left(\frac{V_P - V_D}{2U_T}\right)^2 \tag{58}$$

The total bulk charge obtained from Eqn. 43, can be expressed in terms of Q_{inv} as follows:

$$Q_B = -\gamma \cdot C_{ox} \cdot \sqrt{\Psi_0 + V_P} - \frac{n-1}{n} \cdot Q_{inv} \tag{59}$$

Using charge neutrality, the total gate charge is simply given by:

$$Q_G = \gamma \cdot C_{ox} \cdot \sqrt{\Psi_0 + V_P} - \frac{1}{n} \cdot Q_{inv} - Q_{ox} \tag{60}$$

Differentiating Eqn. 60 with respect to V_S, V_D and V_P leads to the expressions for the intrinsic capacitances in strong inversion:

$$\begin{aligned} C_{gs-strong} &= -\left.\frac{\partial Q_G}{\partial V_S}\right|_{V_G.V_B.V_D} \\ &= C_{ox} \cdot \frac{2}{3} \cdot \left[1 - \frac{i_r}{\left(\sqrt{i_f} + \sqrt{i_r}\right)^2}\right] \end{aligned} \tag{61}$$

$$\begin{aligned} C_{gd-strong} &= -\left.\frac{\partial Q_G}{\partial V_D}\right|_{V_G.V_B.V_S} \\ &= C_{ox} \cdot \frac{2}{3} \cdot \left[1 - \frac{i_f}{\left(\sqrt{i_f} + \sqrt{i_r}\right)^2}\right] \end{aligned} \tag{62}$$

$$\begin{aligned} C_{gb-strong} &= \frac{1}{n} \cdot \left.\frac{\partial Q_G}{\partial V_P}\right|_{V_B.V_S.V_D} - C_{gs} - C_{gd} \\ &= C_{ox} \cdot \frac{n-1}{3 \cdot n} \cdot \left[1 - \frac{4 \cdot \sqrt{i_f \cdot i_r}}{\left(\sqrt{i_f} + \sqrt{i_r}\right)^2}\right] \end{aligned} \tag{63}$$

Note that Eqn. 63 has been obtained by considering the slope factor n as being constant.

The bulk-to-source and bulk-to-drain intrinsic capacitances in strong inversion are given by equations (54) and (55).

3.6. *Intrinsic Capacitances in Weak Inversion*

The total inversion charge can easily be calculated using equations (17) and (42):

$$\begin{aligned} Q_{inv} &= -C_{ox} \cdot \frac{K_w}{2} \cdot U_T \cdot (i_f + i_r) \\ &= -C_{ox} \cdot n \cdot U_T \cdot (i_f + i_r) \end{aligned} \tag{64}$$

where the normalized currents i_f and i_r are given by:

$$\begin{aligned} i_f &= e^{\frac{V_P - V_S}{U_T}} \\ i_r &= e^{\frac{V_P - V_D}{U_T}} \end{aligned} \tag{65}$$

In weak inversion the surface potential is given by Eqn. 15 and so is constant from source to drain. The total bulk charge is simply obtained by multiplying the charge per unit area by the gate surface and replacing Ψ_s by $\Psi_0 + V_P$:

$$Q_B = -\gamma \cdot C_{ox} \cdot \sqrt{\Psi_0 + V_P} \tag{66}$$

The total charge stored on the gate is obtained from Eqn. 44:

$$\begin{aligned} Q_G &= \gamma \cdot C_{ox} \cdot \sqrt{\Psi_0 + V_P} - Q_{inv} - Q_{ox} \\ &\cong \gamma \cdot C_{ox} \cdot \sqrt{\Psi_0 + V_P} - Q_{ox} \end{aligned} \tag{67}$$

where $Q_{ox} = W \cdot L \cdot Q'_{ox}$. Note that even if Eqn. 67 gives a good approximation of the total charge stored on the gate electrode, it does not accurately model the dependence of the total gate charge on the source potential in weak inversion. For this reason, it is better to evaluate capacitances C_{gs} and C_{gd} by directly using the total charge Q_{inv} stored in the channel, which has been evaluated accurately. This can be done by applying the definition of C_{gs} given by Eqn. 45 to Eqn. 44:

$$\begin{aligned} C_{gs} &= \left.\frac{\partial Q_B}{\partial V_S}\right|_{V_G.V_B.V_D} + \left.\frac{\partial Q_{inv}}{\partial V_S}\right|_{V_G.V_B.V_D} \\ &= -C_{bs} + \left.\frac{\partial Q_{inv}}{\partial V_S}\right|_{V_G.V_B.V_D} \end{aligned} \tag{68}$$

Introducing the relation between C_{gs} and C_{bs} given by Eqn. 54 leads to the following:

$$\begin{aligned} C_{gs-weak} &= \frac{1}{n} \cdot \left.\frac{\partial Q_{inv}}{\partial V_S}\right|_{V_G.V_B.V_D} \\ &= C_{ox} \cdot \frac{K_w}{2 \cdot n} \cdot i_f = C_{ox} \cdot i_f \end{aligned} \tag{69}$$

where Eqn. 26 has been used for K_w.

Similarly the gate-to-drain capacitance in weak inversion is given by:

$$C_{gd-weak} = C_{ox} \cdot i_r \tag{70}$$

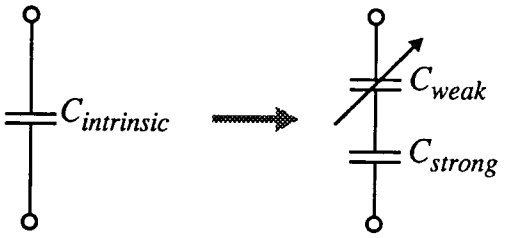


Fig. 13. Intrinsic capacitances model for interpolation.

The gate-to-bulk capacitance is calculated from the total charge stored in the bulk Q_B and is given by:

$$C_{gb-weak} \cong C_{bg-weak} = -\frac{1}{n} \cdot \frac{\partial Q_B}{\partial V_P}\bigg|_{V_B, V_S, V_D}$$
$$= \frac{n-1}{n} \cdot C_{ox} \tag{71}$$

All the intrinsic capacitances are summarized in Table 4. After having calculated the intrinsic capacitances versus i_f and i_r, an interpolation function that relates weak to strong inversion will be derived.

3.7. *Interpolation of the Intrinsic Capacitances*

To interpolate the intrinsic capacitances from weak to strong inversion, it is assumed that they can be modelled by connecting two capacitors C_{strong} and C_{weak} in series as presented in Fig. 13. Each of these capacitor represents the asymptotic behavior of weak and strong inversion, but only C_{weak} is used to interpolate between these asymptotes, using the transconductance interpolation function given by Eqn. 39.

The expressions for the interpolated intrinsic capacitances are given by:

$$C_{gs} = C_{ox} \cdot \left[\frac{1}{c_{gss}(i_f, i_r)} + \frac{1}{c_{gsw}(i_f)}\right]^{-1}$$
$$C_{gd} = C_{ox} \cdot \left[\frac{1}{c_{gss}(i_r, i_f)} + \frac{1}{c_{gsw}(i_r)}\right]^{-1}$$
$$C_{gb} = C_{ox} \cdot \left(\frac{n-1}{n}\right)$$
$$\cdot \left[1 - \frac{c_{gbs}(i_f, i_r) \cdot c_{gbw}(i_f, i_r)}{c_{gbs}(i_f, i_r) + c_{gbw}(i_f, i_r)}\right] \tag{72}$$

where:

$$c_{gss}(i_f, i_r) \equiv \frac{2}{3} \cdot \left[1 - \frac{i_r}{\left(\sqrt{i_f} + \sqrt{i_r}\right)^2}\right]$$
$$c_{gsw}(i_f) \equiv i_f \cdot G(i_f) \tag{73}$$
$$c_{gbs}(i_f, i_r) \equiv \frac{2}{3} \cdot \left[1 + 2 \cdot \frac{\sqrt{i_f \cdot i_r}}{\left(\sqrt{i_f} + \sqrt{i_r}\right)^2}\right]$$
$$c_{gbw}(i_f, i_r) \equiv i_f \cdot G(i_f) + i_r \cdot G(i_r) \tag{74}$$

and where $G(i)$ is given by Eqn. 39.

The five interpolated intrinsic capacitances normalized to C'_{ox} are plotted in Fig. 14a) versus the gate voltage in conduction ($V_D = 0$ V) and in saturation ($V_D = 2$ V). Fig. 14b) shows the same normalized capacitances plotted versus the drain voltage in moderate inversion ($V_G = 0.8$ V) and in strong inversion ($V_G = 2.4$ V). In both cases, the source voltage has been set to zero. These plots are in good accordance with the results presented in [1] and [22].

3.8. *Experimental Results*

The intrinsic capacitances in saturation have been measured versus the gate voltage for $V_S = 0$ and 2 V and are presented in Fig. 15 a). They are compared to the analytical expressions given above, where the normalized current was evaluated from the gate voltage using the large-signal equations (8) and (31). Capacitance C_{bs} could not be measured, but the predicted behavior is in accordance with the experimental data presented in reference [22]. Fig. 15 b) illustrates the variation of the gate-to-source capacitance with the current as predicted by Eqn. 72.

In addition to the intrinsic capacitances, there are also some extrinsic capacitances due to the source and drain junctions and to the overlap of the gate on the source and drain diffusions [1].

4. A First-Order Non-Quasi-Static Model

It can be shown that the model derived in section 3 is only valid for frequencies much smaller than $\omega_0/6$ where ω_0 is the transition frequency, given by [1]:

$$\omega_0 = \frac{\mu_n}{L^2} \cdot (V_P - V_S) \tag{75}$$

For frequencies above $\omega_0/6$, a non-quasi-static approach is needed. Note that because ω_0 is inversely

Table 4. Normalized intrinsic capacitances.

Normalized Capacitances	Weak Inversion	Strong Inversion	
		Conduction	Forward Saturation
C_{gs}/C_{ox}	i_f	$\frac{2}{3}\cdot\left[1-\frac{i_r}{\left(\sqrt{i_f}+\sqrt{i_r}\right)^2}\right]$	$\frac{2}{3}$
C_{gd}/C_{ox}	i_r	$\frac{2}{3}\cdot\left[1-\frac{i_f}{\left(\sqrt{i_f}+\sqrt{i_r}\right)^2}\right]$	≈ 0
C_{bs}/C_{ox}	$(n-1)\cdot C_{gs}/C_{ox}$		
C_{bd}/C_{ox}	$(n-1)\cdot C_{gd}/C_{ox}$		
C_{gb}/C_{ox}	$1-\frac{1}{n}$	$\frac{n-1}{3\cdot n}\cdot\left[1-\frac{4\cdot\sqrt{i_f\cdot i_r}}{\left(\sqrt{i_f}+\sqrt{i_r}\right)^2}\right]$	$\frac{n-1}{3\cdot n}$

proportional to the square of the transistor length, this limit can appear quite rapidly for very long transistors. Beyond this limit, a non-quasi-static approximation is necessary to take into account the effects of a distributed time constant, also known as "transmission line effects." A first order non-quasi-static model can be obtained from the equivalent circuit of Fig. 10 by replacing the transconductances by appropriate transadmittances. In order to derive these transadmittances, the MOS transistor can be split into a series of elementary transistors sufficiently small that they all operate in conduction and in a quasi-static mode. Since the transcapacitances are negligible in conduction, the elementary transistors can be replaced by the quasi-static model presented previously. The corresponding small-signal circuit is shown in Fig. 16 and corresponds to a non-uniform multilayer distributed RC line [23].

Each elementary capacitor of the small-signal circuit introduces a pole in the gate transadmittance Y_{mg}. If the section becomes infinitesimal, the transadmittance is made of an infinite number of different negative real poles distributed along the real axis as a function of the spatial distribution of the elementary resistances and capacitances along the channel:

$$\begin{aligned} Y_{mg} &\equiv \left.\frac{\Delta I_D}{\Delta V_G}\right|_{\Delta V_D=\Delta V_S=0} \\ &= \frac{g_{mg}}{\prod_{n=1}^{\infty}(1+s\cdot\tau_n)} \\ &\cong \frac{g_{mg}}{1+s\cdot\tau} \end{aligned} \tag{76}$$

where g_{mg} depends on i_f and i_r and is given by Eqn. 36.

A first order approximation of the transadmittance can be made by assuming that the poles introduced by each elementary capacitance have only minor effect and therefore can be superimposed separately taking into account their non-uniform spatial distribution. The time constant associated with an elementary section can be calculated using the zero-value time constant approximation [24] on the circuit of Fig. 17, where $C''(x)$ represents the total capacitance between the channel and the ground of one elementary section. Note that $C''(x)$ is in capacitance per unit length and depends on the position x along the channel.

The conductance seen by the capacitance $C''(x)$ is the sum of the drain and the source transconductance of transistors T_1 and T_2:

$$\begin{aligned} g(x) &= g_{md1}+g_{ms2} \\ &= \frac{I_{R1}}{U_T}\cdot G(i_{r1})+\frac{I_{F2}}{U_T}\cdot G(i_{f2}) \end{aligned} \tag{77}$$

where:

$$\begin{aligned} I_{R1} &= 2\cdot n\cdot\beta_1\cdot U_T^2\cdot i_{r1}(x) \\ &= 2\cdot n\cdot\mu_n\cdot C'_{ox}\cdot U_T^2\cdot i(x)\cdot\frac{W}{x} \end{aligned} \tag{78}$$

$$\begin{aligned} I_{F2} &= 2\cdot n\cdot\beta_2\cdot U_T^2\cdot i_{f2}(x) \\ &= 2\cdot n\cdot\mu_n\cdot C'_{ox}\cdot U_T^2\cdot i(x)\cdot\frac{W}{L-x} \end{aligned} \tag{79}$$

$$i_{r1}(x) = i_{f2}(x) = i(x) \tag{80}$$

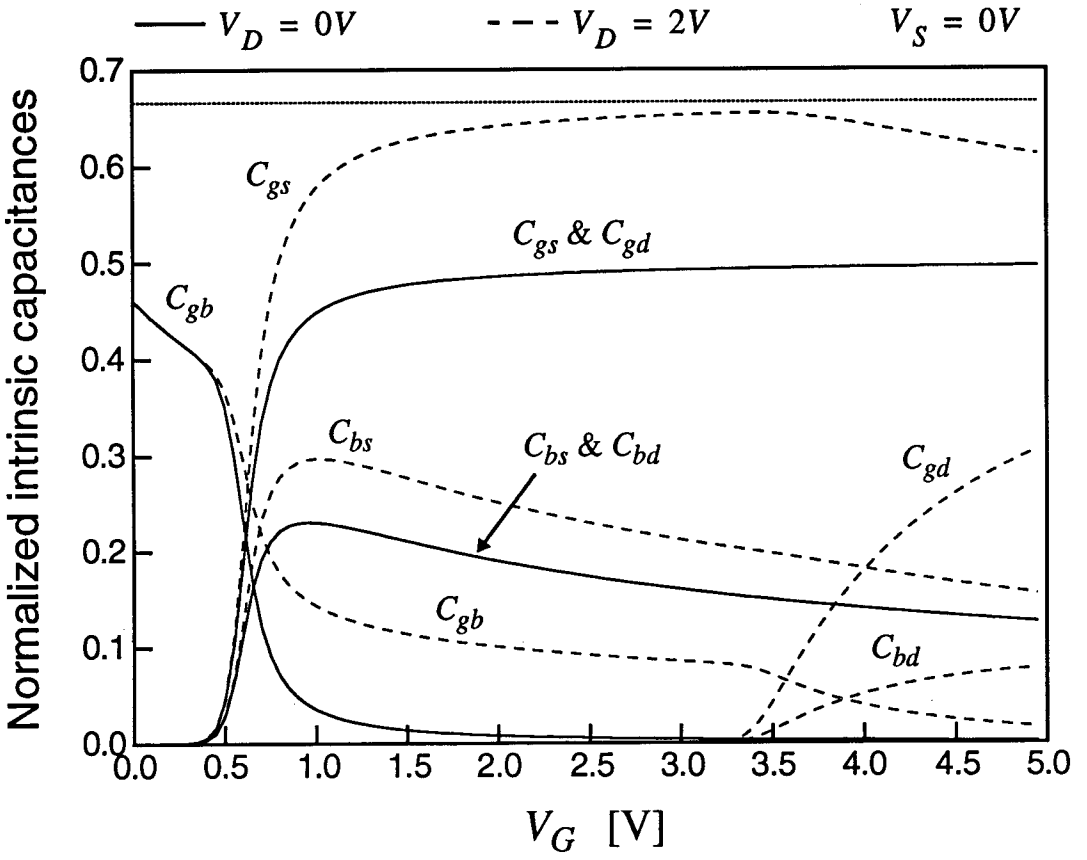


Fig. 14. (a) Calculated normalized capacitances versus V_G.

Substituting equations (78) to (80) into Eqn. 77 leads to:

$$R(x) \equiv \frac{1}{g(x)} = \frac{x \cdot (L-x)}{2 \cdot n \cdot W \cdot L \cdot \mu_n \cdot C'_{ox} \cdot U_T} \cdot \frac{1}{i \cdot G(i)} \tag{81}$$

The capacitance $C''(x)$ is simply the sum of the gate-to-drain and drain-to-bulk capacitances of transistor T_1 and the gate-to-source and source-to-bulk capacitances of transistor T_2, all evaluated at $i_{f2} = i_{r1} = i(x)$:

$$C''(x) = 2 \cdot n \cdot W \cdot C'_{ox} \cdot \frac{2 \cdot i \cdot G(i)}{1 + 2 \cdot i \cdot G(i)} \tag{82}$$

The first order time constant is obtained by summing all the elementary time constants $R(x) \cdot C''(x)$ along the channel:

$$\tau = \int_0^L R(x) \cdot C''(x) \cdot dx \tag{83}$$

Introducing the relation existing between the normalized current $i(x)$ and the position in the channel given in Appendix A3 (Eqn. A.10) leads to:

$$\tau = \frac{2 \cdot \tau_0}{(i_f - i_r)^3} \cdot \int_{i_r}^{i_f} \frac{(i_f - i) \cdot (i - i_r)}{1 + 2 \cdot i \cdot G(i)} \cdot di \tag{84}$$

where:

$$\tau_0 \equiv \frac{L^2}{2 \cdot \mu_n \cdot U_T} \tag{85}$$

This integral expression of τ depends only on the normalized forward and reverse currents i_f and i_r of the transistor and therefore is valid for all modes of operation. Unfortunately, it cannot be integrated analytically, but it has been integrated numerically and plotted versus the inversion factor i_f in Fig. 18 for different $\alpha = i_r / i_f$ ratios. Fig. 18 shows that τ is constant and independent of the mode of operation of the transistor in weak inversion and decreases with $1/\sqrt{i_f}$ in strong inversion with a slight dependence on the α ratio. The

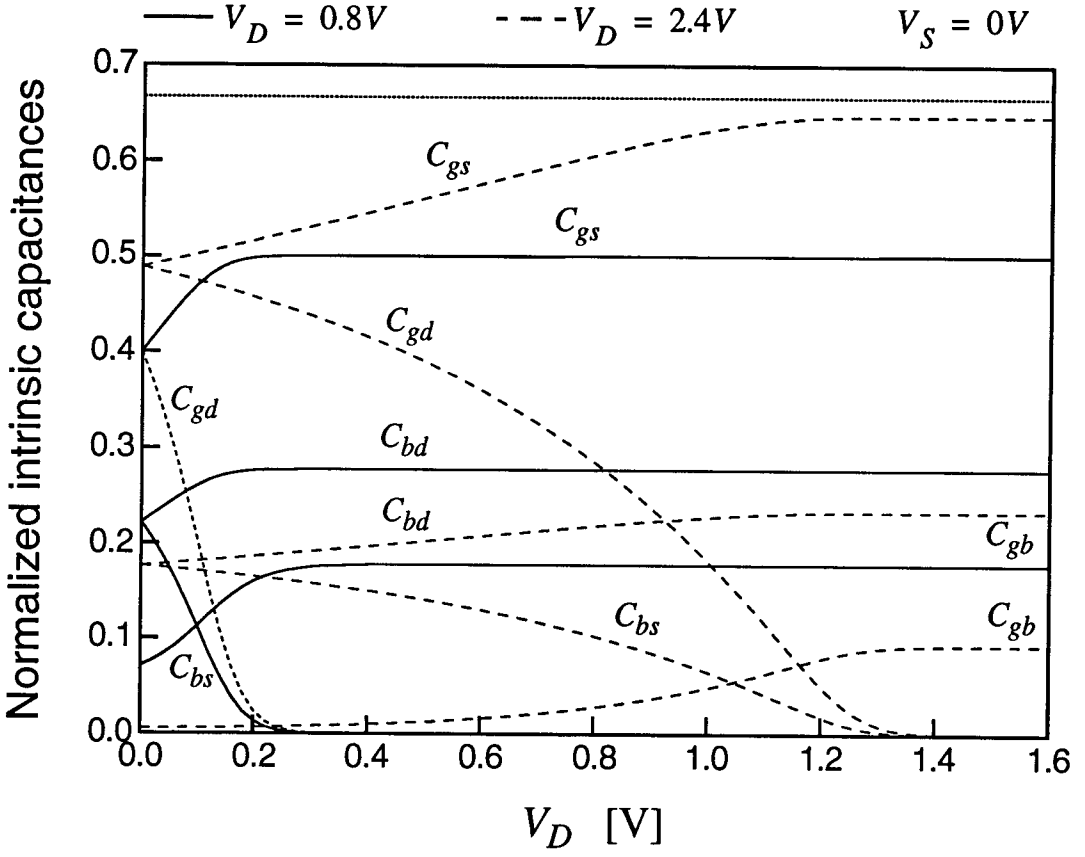


Fig. 14. (b) Calculated normalized capacitances versus V_D.

integral can be simplified in the asymptotic case of weak inversion where i_f, i_r and i can be assumed to be much smaller than 1:

$$\tau \cong \frac{2 \cdot \tau_0}{(i_f - i_r)^3} \cdot \int_{i_r}^{i_f} (i_f - i) \cdot (i - i_r) \cdot di = \frac{\tau_0}{3}$$

(*weak inversion*) (86)

This corresponds to the value obtained for the base transit time of a bipolar transistor [25]. An equivalent approximation can be made to find the asymptotic value in strong inversion where i_f and i_r are much larger than 1:

$$\tau \cong \frac{\tau_0}{(i_f - i_r)^3} \cdot \int_{i_r}^{i_f} \frac{(i_f - i) \cdot (i - i_r)}{\sqrt{i}} \cdot di = \tau_0 \cdot \frac{4}{15} \cdot \frac{i_f + 3 \cdot \sqrt{i_f \cdot i_r} + i_r}{\left(\sqrt{i_f} + \sqrt{i_r}\right)^3}$$

(*strong inversion*) (87)

Note that τ reduces to $\tau_0/6$ in conduction ($i_f = i_r$) which can also be obtained by expanding the hyperbolic functions obtained in the case of a uniform transmission line [23]. In saturation ($i_r = 0$), the time constant corresponds to the results obtained by Tsividis [1] and Khorramabadi [26].

To obtain an approximation of the time constant that is valid in all modes of operation, the curves of Fig. 18 can be fitted by the following simple function:

$$\frac{\tau}{\tau_0} \cong \frac{1}{3} \cdot \frac{1}{\sqrt{1 + i_f / i_k}} \quad (88)$$

where:

$$i_k \equiv \left[\frac{4}{5} \cdot \frac{1 + 3 \cdot \sqrt{\alpha} + \alpha}{(1 + \sqrt{\alpha})^3}\right]^2 \text{ and}$$

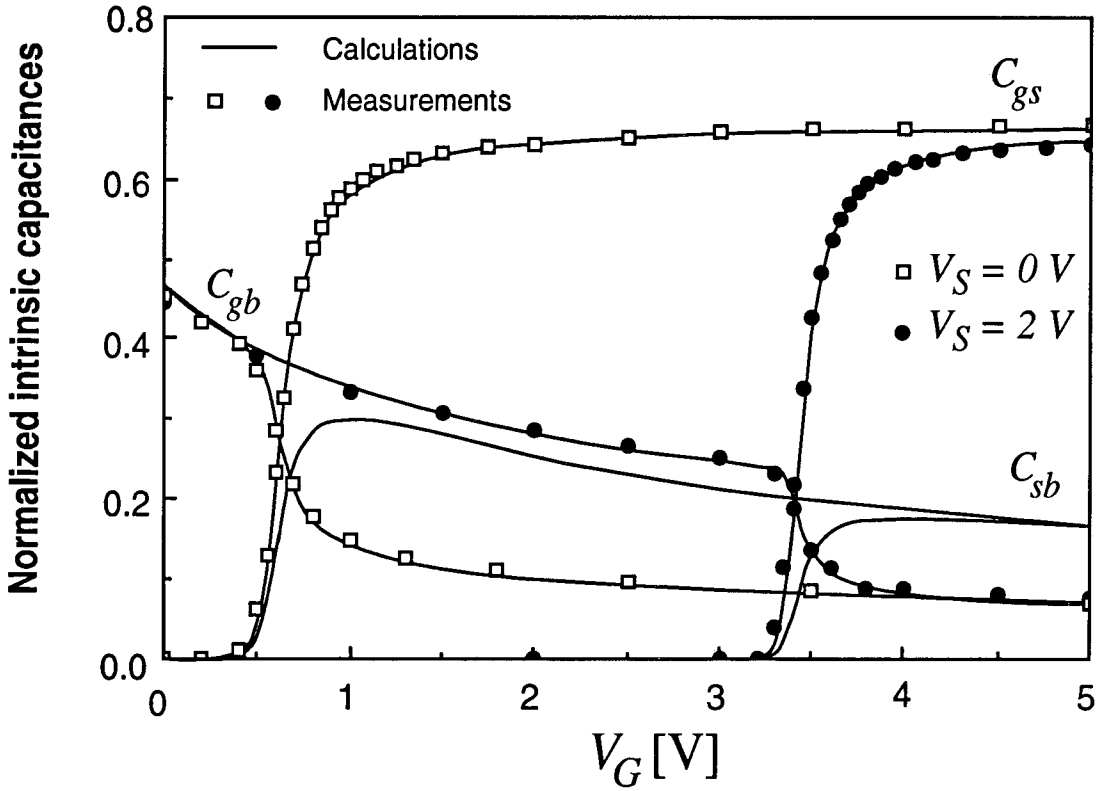


Fig. 15. (a) Intrinsic capacitances normalized to C_{ox} in saturation versus the gate voltage for $V_S = 0$ and 2 V.

$$\alpha \equiv \frac{i_r}{i_f} \tag{89}$$

The maximum fitting error obtained from Eqn. 88 in strong inversion is typically less than 2%. The same time constant can be used for the source and drain transadmittances:

$$Y_{ms} \equiv -\left.\frac{\Delta I_D}{\Delta V_S}\right|_{\Delta V_G=\Delta V_D=0} = \frac{g_{ms}}{1+s\cdot\tau} \tag{90}$$

$$Y_{md} \equiv \left.\frac{\Delta I_D}{\Delta V_D}\right|_{\Delta V_G=\Delta V_S=0} = \frac{g_{md}}{1+s\cdot\tau} \tag{91}$$

where g_{ms} and g_{md} are given by Eqn. 36 and τ is given by Eqn. 88.

The complete high-frequency small-signal model is then simply obtained by replacing the transconductances by the previously defined transadmittances as shown in Fig. 19. This model can still be improved for higher frequency by changing the intrinsic capacitances with more complex admittances as described in [1] and [22].

5. Thermal Noise Model

5.1. *General Expression of the Thermal Noise Power Spectral Density*

A general expression for the thermal noise Power Spectral Density (PSD) can be established by first considering an elementary section of the channel of length dx having a resistance dR. This resistance produces a noise voltage dV_{ch} which has a PSD given by:

$$dS_{\Delta V_{ch}} = 4\cdot k\cdot T\cdot dR \tag{92}$$

where:

$$dR = \frac{dV_{ch}}{I_D} = \frac{dx}{W\cdot\mu_n\cdot(-Q'_{inv})} \tag{93}$$

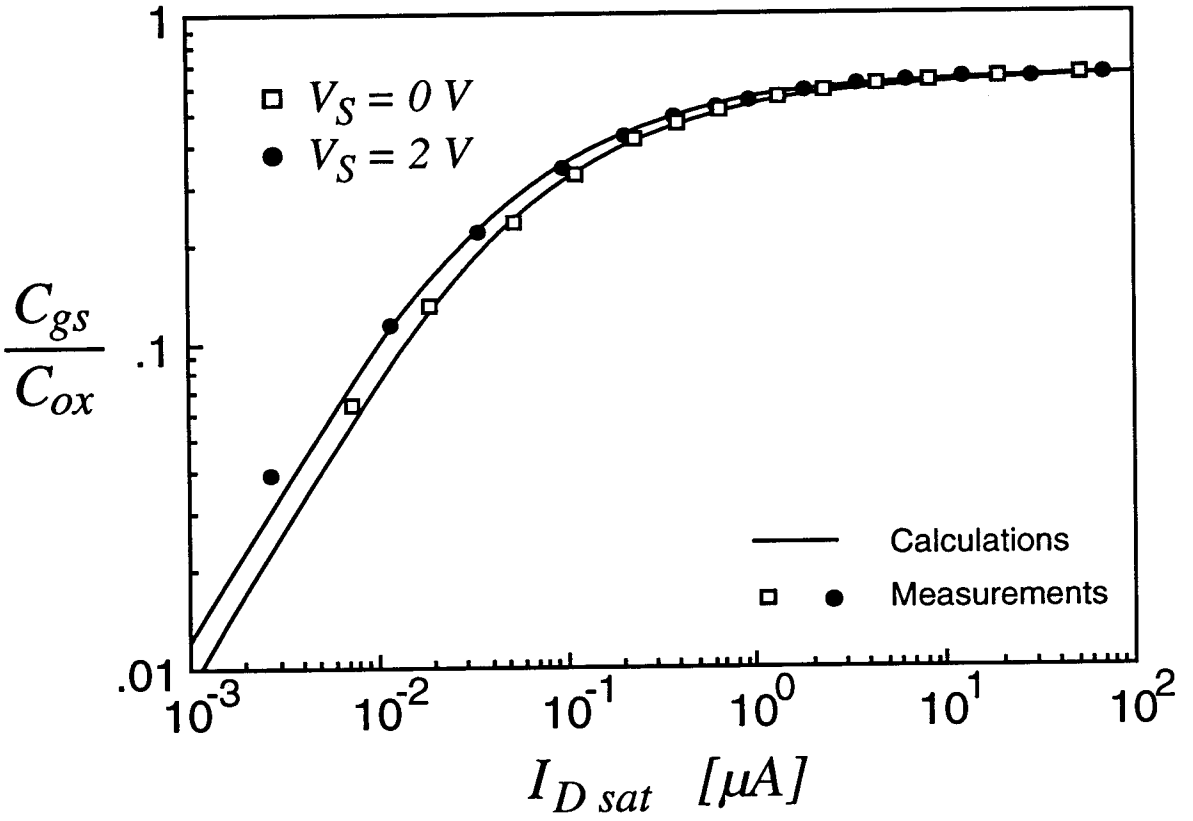


Fig. 15. (b) Normalized intrinsic gate-to-source capacitance in saturation versus the drain current for $V_S = 0$ and 2 V.

The PSD of the drain current fluctuation due to this localized noise voltage source is obtained by multiplying $dS_{\Delta V_{ch}}$ by the square of the local channel conductance g_{ch} defined as:

$$g_{ch} = \frac{dI_D}{dV_{ch}} = \mu_n \cdot \frac{W}{L} \cdot (-Q'_{inv}) \tag{94}$$

Leading to:

$$\begin{aligned} dS_{\Delta I_D} &= g_{ch}^2 \cdot dS_{\Delta V_{ch}} \\ &= 4 \cdot k \cdot T \cdot \frac{\mu_n}{L^2} \cdot W \cdot (-Q'_{inv}) \cdot dx \end{aligned} \tag{95}$$

Integrating from source to drain gives the total PSD of the drain current fluctuations which can be expressed in terms of a thermal noise conductance G_{Nth}:

$$S_{\Delta I_D} = 4 \cdot k \cdot T \cdot G_{Nth} \tag{96}$$

$$\begin{aligned} G_{Nth} &= \frac{\mu_n}{L^2} \cdot W \cdot \int_0^L -Q'_{inv} \cdot dx \\ &= \frac{\mu_n}{L^2} \cdot |Q_{inv}| \end{aligned} \tag{97}$$

Eqn. 97 shows that the current fluctuation PSD is proportional to the total charge stored in the channel. This is true in strong inversion as well as in weak inversion. The thermal noise can be modelled as a current source between source and drain having a PSD given by Eqn. 96. In saturation, it can also be referred to the gate as a voltage source having an equivalent thermal noise resistance given by:

$$R_{Nth} = \frac{G_{Nth}}{g_{mg}^2} \quad (saturation) \tag{98}$$

It can now be expressed in terms of the normalized currents by using the total channel charge already calculated for the intrinsic capacitances.

5.2. *Thermal Noise Power Spectral Density (PSD) in Strong and in Weak Inversion*

The total channel charge in strong inversion is given by Eqn. 56 and the corresponding thermal noise conduc-

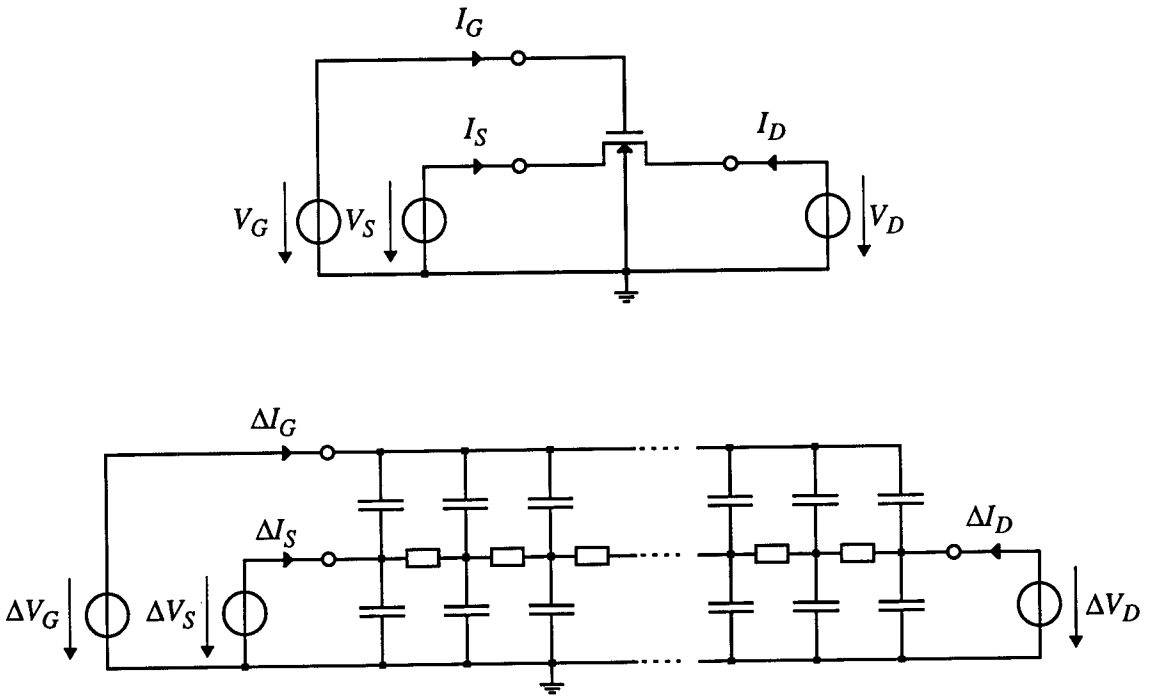


Fig. 16. Small-signal equivalent circuit of the distributed MOS transistor.

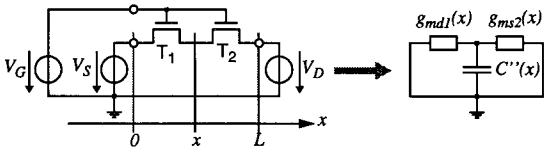


Fig. 17. Equivalent circuit to calculate the time constant of one elementary section using zero-value time constant approximation.

tance is given by:

$$G_{Nth-strong} = n \cdot \beta \cdot U_T \cdot \frac{4}{3} \cdot \frac{i_f + \sqrt{i_f \cdot i_r} + i_r}{\sqrt{i_f} + \sqrt{i_r}} \qquad (99)$$

$$= \begin{cases} g_{ms} & \text{for: } i_f = i_r \quad (V_D = V_S) \\ \frac{2}{3} \cdot g_{ms} & \text{for: } i_f \gg i_r \quad (V_D \gg V_S) \end{cases}$$

Eqn. 99 shows that the noise conductance is proportional to the source transconductance. The equivalent noise resistance in saturation is given by:

$$R_{Nth-strong} = \frac{2}{3} \cdot \frac{n}{g_{mg}} \quad (saturation) \qquad (100)$$

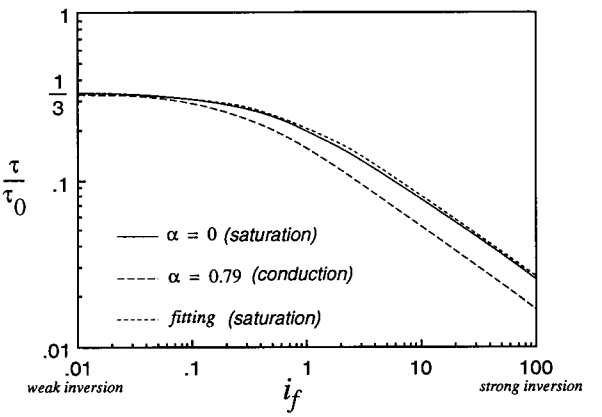


Fig. 18. Normalized transadmittance time constant versus the inversion factor i_f for different $\alpha = i_r / i_f$ ratios.

The thermal noise conductance and equivalent noise resistance in weak inversion are derived from Eqn. 64:

$$G_{Nth-weak} = n \cdot \beta \cdot U_T \cdot (i_f + i_r)$$

$$= \begin{cases} g_{ms} & \text{for: } i_f = i_r \quad (V_D = V_S) \\ \frac{g_{ms}}{2} & \text{for: } i_f \gg i_r \quad (V_D \gg V_S) \end{cases} \qquad (101)$$

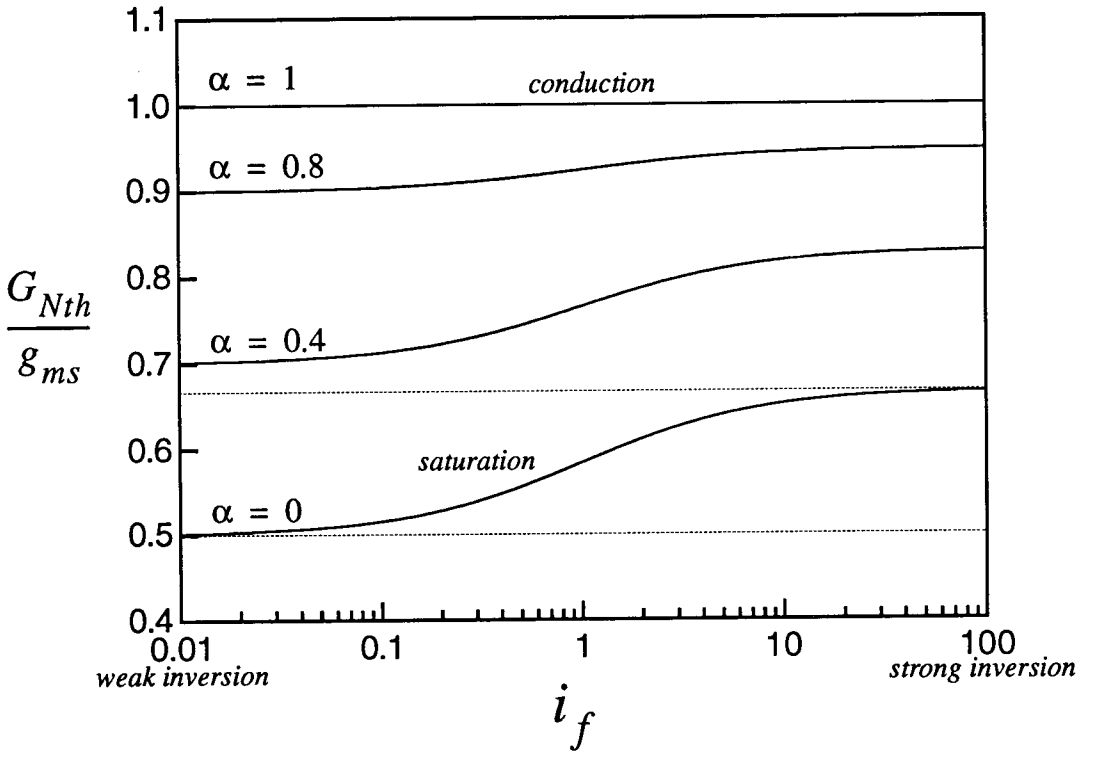


Fig. 20. (a) Thermal noise interpolation function plotted from weak to strong inversion for different values of $\alpha = i_r/i_f$.

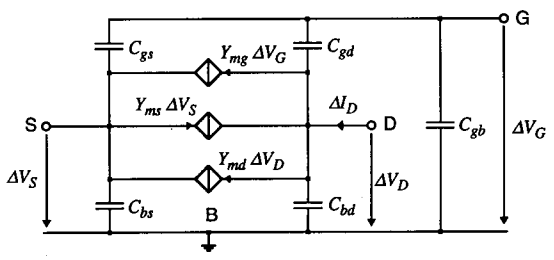


Fig. 19. Complete high-frequency small-signal model.

$$R_{Nth-weak} = \frac{n}{2 \cdot g_{mg}} \quad (saturation) \tag{102}$$

In weak inversion, the PSD can also be written by replacing the normalized forward and reverse currents appearing in Eqn. 101 by their definitions $i_f \equiv I_F/I_S$ and $i_r \equiv I_R/I_S$ with $I_S \equiv 2 \cdot n \cdot \beta \cdot U_T^2$:

$$S_{\Delta I_D} = 4 \cdot k \cdot T \cdot n \cdot \beta \cdot U_T \cdot \frac{I_F + I_R}{2 \cdot n \cdot \beta \cdot U_T^2}$$

$$= 2 \cdot q \cdot (I_F + I_R) \tag{103}$$

Eqn. 103 corresponds to full shot noise of both the *forward and the reverse components* [27].

5.3. *Interpolation of the Thermal Noise PSD from Weak to Strong Inversion*

The thermal noise PSD can also be interpolated from weak to strong inversion using the following function:

$$\frac{G_{Nth}}{g_{ms}} = \frac{1}{1+i_f} \cdot \left[\frac{1+\alpha}{2} + \frac{2}{3} \cdot i_f \cdot \frac{1+\sqrt{\alpha}+\alpha}{1+\sqrt{\alpha}}\right]$$

$$\text{where: } \alpha = \frac{i_r}{i_f} \tag{104}$$

Eqn. 104 is plotted in fig. 20 versus if for different values of α ranging from 0 (saturation) to 1 (conduction).

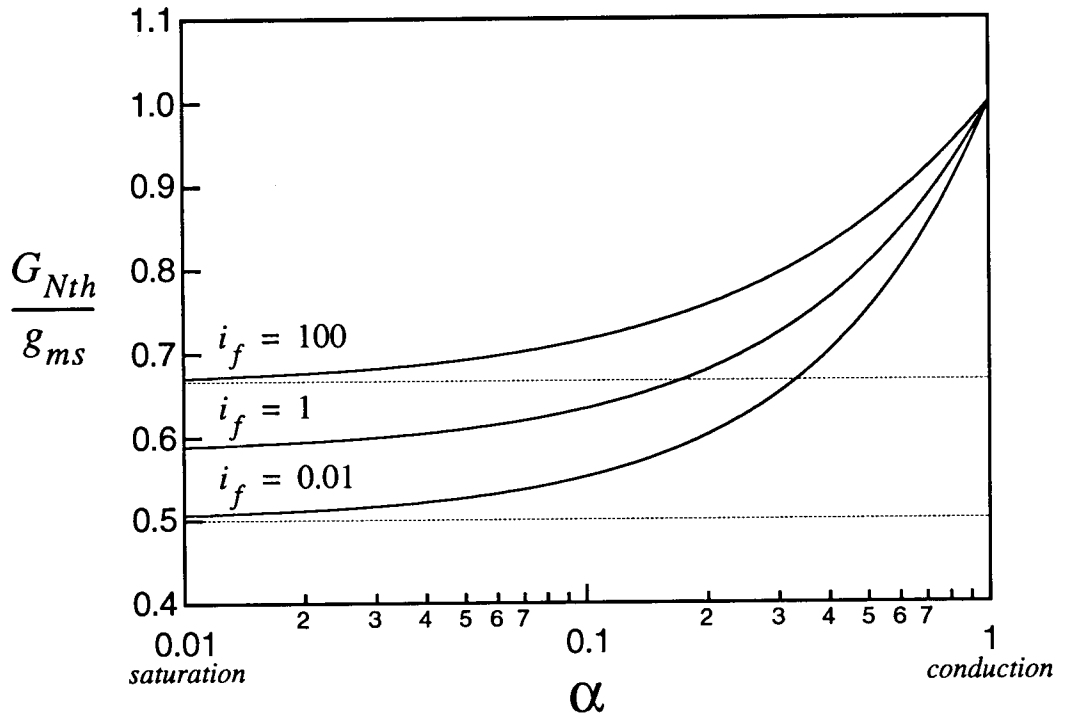


Fig. 20. (b) Thermal noise interpolation function plotted from saturation to conduction for different values of i_f.

6. Second-Order Effects

6.1. Mobility Reduction Due to Vertical Field

The effective mobility taking into account the effect of the normal field is defined as:

$$\mu_{eff} \equiv \frac{\mu_n}{1 + \theta \cdot V_P} \tag{105}$$

where parameter θ typically ranges between 0.1 and 0.5 V^{-1}. From the definition of μ_{eff} it can be noticed that the mobility decreases for an increase in the gate-to-bulk voltage and is independent of the source-to-bulk voltage.

6.2. Velocity Saturation

The effect of velocity saturation tends to reduce the saturation current with respect to the V_{DS} voltage according to [1]:

$$I_D = \frac{I_{D0}}{1 + \frac{V_D^* - V_S}{L \cdot E_C}} \qquad \text{where:}$$

$$V_D^* \equiv \begin{cases} V_D & \text{for: } V_D < V_{Dsat} \\ V_{Dsat} & \text{for: } V_D \geq V_{Dsat} \end{cases} \tag{106}$$

where I_{D0} is the current evaluated without velocity saturation, V_{Dsat} is the value of V_D where the current takes its maximum and E_c is the critical field [1]. As shown in Fig. 21, the effect of velocity saturation is to reduce the initial current calculated without velocity saturation and particularly the saturation current obtained for $V_D > V_P$. Introducing this effect according to Eqn. 106 while keeping V_P as the drain saturation voltage would produce an undesirable bump at $V_D = V_{Dsat}$. This can be avoided by simply clamping the drain voltage at a certain value V_{Dsat} for which the current is maximum, as shown in Fig. 21. The value of this new saturation voltage V_{Dsat} is obtained by calculating the derivative of Eqn. 106 and solving it with respect to V_D taking into account the critical field E_c and the transistor length L. Note that the clamping of V_D should be made smoothly in order to have continuous derivatives and thus continuous output conductance.

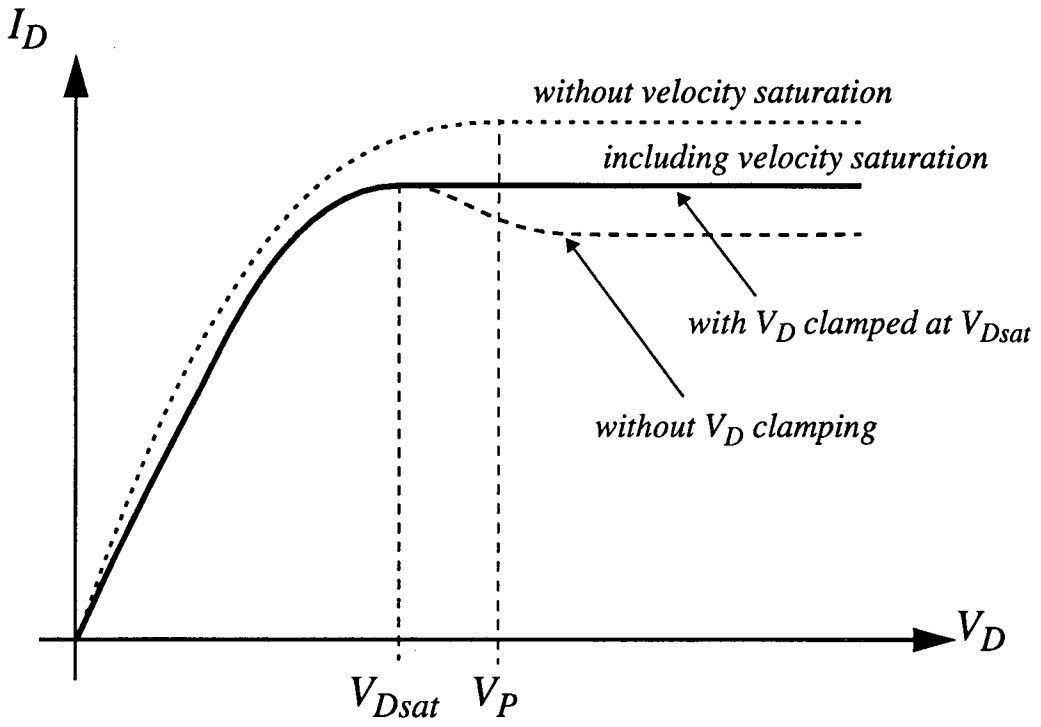


Fig. 21. (a) Effect of the velocity saturation on the drain current.

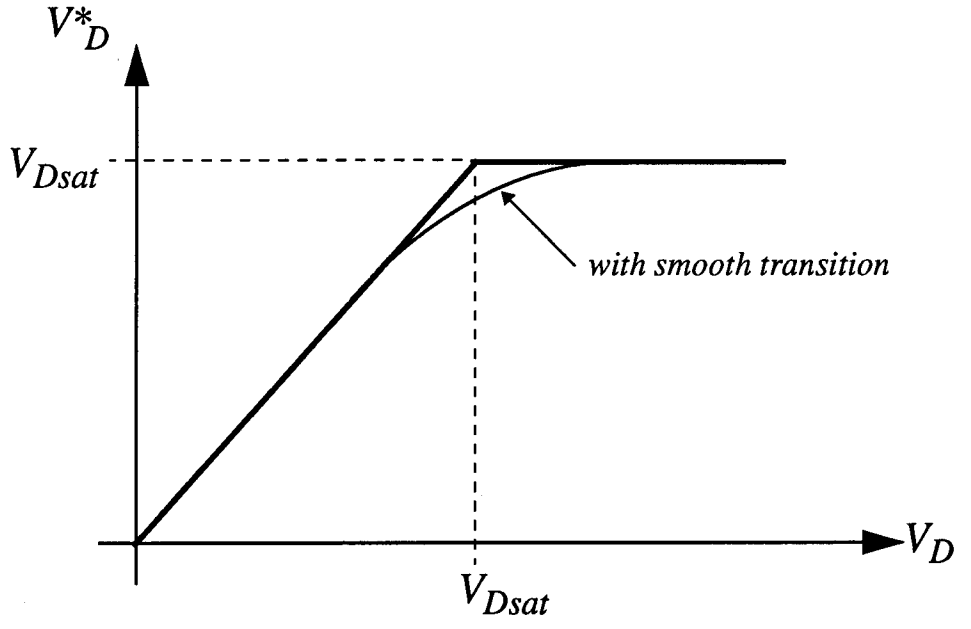


Fig. 21. (b) Drain voltage clamping.

6.3. *Channel Length Modulation and Output Conductance*

Although channel shortening is a very complicated phenomenon, involving two-dimensional analysis, it can be illustrated as follows: when V_D becomes equal to V_P, the channel is pinched-off just at the drain diffusion limit. When $V_D > V_P$, the pinch-off point moves towards the source, reducing the channel length by ΔL. The inversion charge between this point and the drain is nearly zero and therefore this region can be considered as a depletion region. The channel length reduction ΔL can then be approximated by [1]:

$$\Delta L \cong \zeta \cdot \sqrt{V_D - V_P} \quad \text{for: } V_D \geq V_P \tag{107}$$

where:

$$\zeta \equiv \frac{2 \cdot \varepsilon_s}{\gamma \cdot C'_{ox}} = \sqrt{\frac{2 \cdot \varepsilon_s}{q \cdot N_{sub}}} \tag{108}$$

Correcting the drain current in the saturation region according to Eqn. 107 yields the output characteristics shown in Fig. 22a). Clearly, these are not satisfactory for small-signal analysis since the output conductance suffers from strong discontinuities. The latter characteristic is currently improved by:

a) using V'_{Dsat} instead of V_P in Eqn. 107, where V'_{Dsat} is obtained by evaluating the gap between the 2 values of V_D for which the drain-to-source conductance is the same (see Fig. 22a));
b) smoothing the function $\Delta L(V_D - V'_{Dsat})$ around $V_D - V'_{Dsat}$.

A qualitative representation of the obtained characteristics is depicted in Fig. 22b).

The final evaluation of V'_{Dsat} also takes into account the velocity saturation described previously.

A default evaluation of channel length modulation parameter ζ can be performed from the value of process parameters γ and C'_{ox}. It may be further used as a fitting parameter in conjunction with measured data.

6.4. *Short and Narrow-Channel Effects*

The modelling of short- and narrow-channel effects is based on the charge-sharing concept. Following the derivation presented in [1], V_P now becomes a function of V_G, V_{T0}, γ, Ψ_0 and of new variable $\alpha(\Psi_0, V_S, V_D, L, W, \eta_L, \eta_W)$, in which parameters η_L and η_W account for short- and narrow-channel effects respectively:

$$V_P = V_G - V_{T0} + \gamma \cdot \sqrt{\Psi_0} - \alpha \cdot \gamma \cdot \left[\sqrt{V_G - V_{T0} + \gamma \cdot \sqrt{\Psi_0} - \left(\frac{\alpha \cdot \gamma}{2}\right)^2} - \frac{\alpha \cdot \gamma}{2} \right] \tag{109}$$

where:

$$\alpha = 1 + \zeta \cdot \left\{ \frac{\eta_W}{W_{eff}} \cdot \sqrt{\Psi_0 + V_S} - \frac{\eta_L}{L_{eff}} \cdot \left(\sqrt{\Psi_0 + V_S} + \sqrt{\Psi_0 + V_D} \right) \right\} \tag{110}$$

Dimensionless parameters η_W and η_L can be given default values based on known process parameters, or can be extracted from measured data.

7. Conclusions

The symmetry of the transistor can be preserved by referring all voltages to the local substrate. The state of any point of the channel of a transistor is controlled by $V_P - V_{ch}$, where the non-equilibrium voltage V_{ch}, simply called channel "potential" is produced by drain and source voltages V_D and V_S, and V_P is the pinch-off voltage depending only on the gate voltage V_G. This state can be characterized by the degree of inversion of the channel. Weak inversion for $V_{ch} > V_P$ corresponds to a density of mobile charge that can be neglected in the field calculations, whereas strong inversion for $V_{ch} < V_P$ corresponds to a large density of mobile charge which clamps the surface potential to a value that can be approximated as constant. The various possible modes of operation (conduction, forward and reverse saturation, weak inversion, blocked) depend on the degree of inversion at each end of the channel, and therefore on $V_P - V_S$ and $V_P - V_D$ (Fig. 6).

Using the charge sheet model with the assumption of constant doping in the channel, the drain current I_D can be expressed as the difference of a forward component I_F and a reverse component I_R (Fig. 7). Each of these is proportional to a function of $V_P - V_S$, respectively $V_P - V_D$, through a specific current I_S given by Eqn. 25. This function is exponential in weak inversion and quadratic in strong inversion (Eqn. 29). It can be continuously

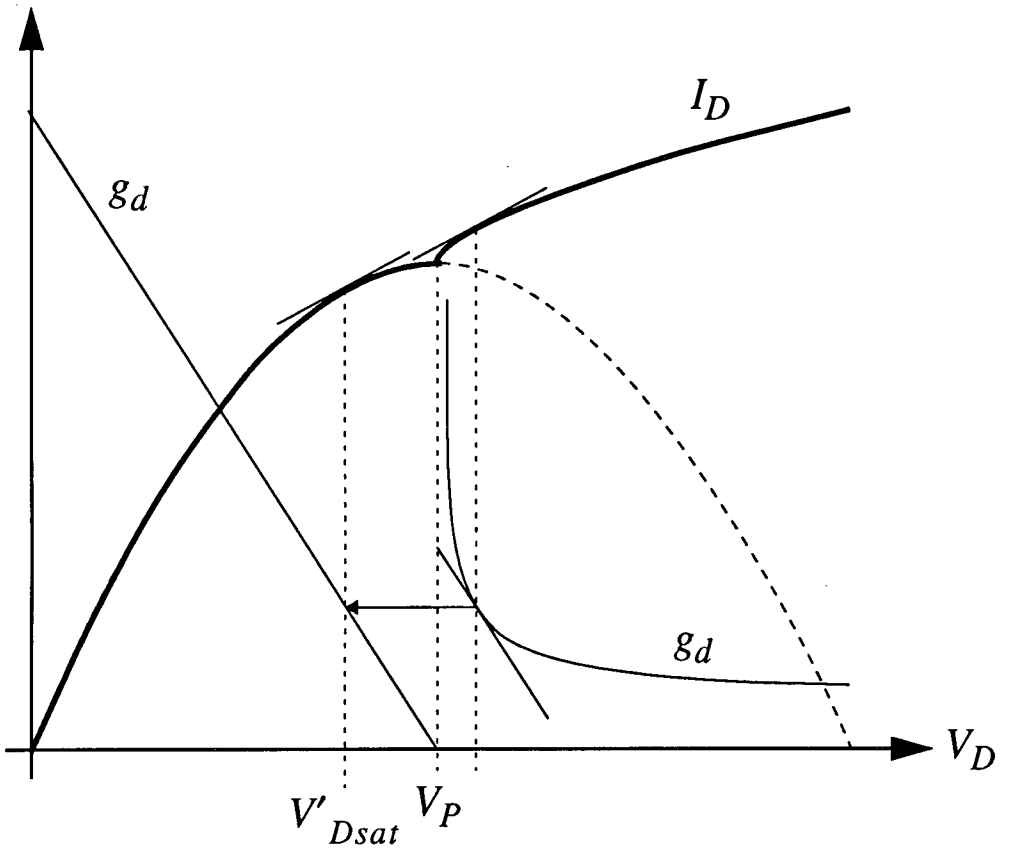


Fig. 22. Channel length modulation effect: (a) Eqn. 107 with $V_{Dsat} = V_P$.

interpolated in between (Eqn. 30). $I_D(V_P, V_S, V_D)$ can thus be expressed from very low to high currents by means of a single parameter I_S.

Describing $I_D(V_G, V_S, V_D)$ requires as additional parameters the threshold V_{T0}, and in a first approximation the slope factor n (Eqn. 11). For better precision, the value of n can be adapted to V_G (Eqn. 10) or the complete expression of $V_P(V_G)$ (Eqn. 7) can be used, requiring two additional parameters, γ (bulk modulation factor) and Ψ_0 (surface potential in strong inversion for $V_D = V_S = 0$), for a total of only four parameters.

The small-signal model is directly obtained by differentiation (Eqn. 38); the resulting transconductance is continuous from weak to strong inversion and is within 10% of exact calculations and experimental data. A better precision of 3% is obtained with another interpolation for the transconductance (Eqn. 39), which can then be integrated to obtain the corresponding large-signal interpolation function (Eqn. A3).

A simple quasi-static small-signal model is obtained by adding five intrinsic capacitors. Each of them is proportional to a function of I_F/I_S and I_R/I_S through a single additional parameter, namely the gate oxide capacitance C'_{ox} (Table IV). This model is valid for frequencies much lower than the transition frequency of the transistor given by Eqn. 75. Higher frequencies may be treated with a first-order non quasi-static model (equations (88) to (91)) which does not require any additional parameter.

Thermal noise is proportional to the total charge in the channel and can be expressed continuously from weak to strong inversion without any new parameter (Eqn. 104).

Second order effects like mobility reduction, velocity saturation, channel length modulation and short and narrow channel effects are added on top of the basic model and are included in the complete formulation

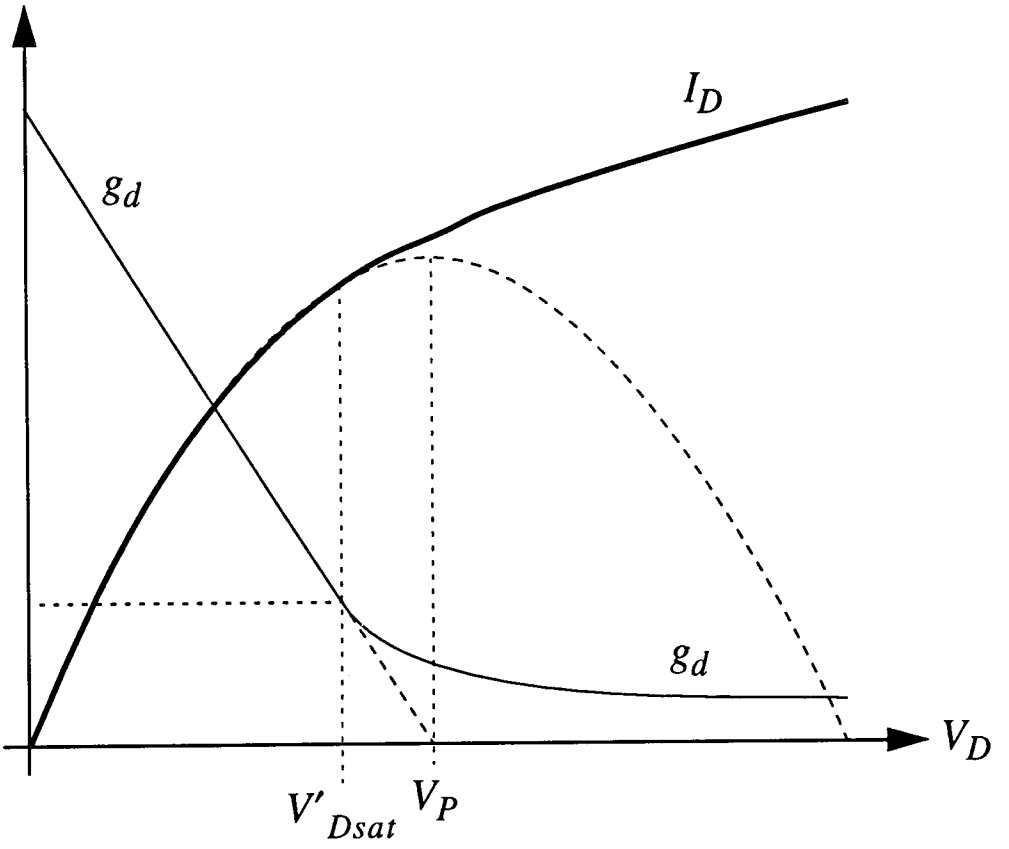


Fig. 22. Channel length modulation effect: (b) improved transition from conduction to saturation with $V'_{Dsat} < V_P$.

for computer simulation, which is already available with several commercial circuit simulation programs. This model has only 9 physical parameters (COX, VTO, GAMMA, PHI, KP, THETA, UCRIT, DW, DL), 3 fine tuning fitting coefficients (LAMBDA, WETA, LETA) and 2 additional temperature parameters.

8. Notice

Further information concerning the model formulation for computer simulation is available from:

Prof. Christian C. Enz
EPFL
Electronics Laboratory (LEG)
ELB Ecublens
CH-1015 Lausanne
Switzerland

9. Appendix

A1. Derivation of the Large-Signal Interpolation Function Corresponding to Eqn. 39

The relation between the normalized voltage $v = v_p - v_s$ (respectively $v_p - v_d$) and the normalized current i_f (i_r) can be derived from the definition of the transconductance interpolation function $G(i_f)$ given by Eqn. 39 and from the definition of transconductances and Eqn. 36:

$$dv = \frac{di_f}{i_f \cdot G(i_f)} = \frac{\sqrt{i_f + \frac{1}{2} \cdot \sqrt{i_f} + 1}}{i_f} \cdot di_f \qquad \text{(A.1)}$$

and so:

$$v = \int \frac{\sqrt{i_f + \frac{1}{2} \cdot \sqrt{i_f} + 1}}{i_f} \cdot di_f \qquad \text{(A.2)}$$

Performing the integration gives the large-signal interpolation function corresponding to Eqn. 39:

$$\begin{aligned} v &= ln(i) + 2\cdot(\sqrt{r}-1) - 2 \\ &\quad \cdot ln\left(\frac{\sqrt{i}+4\cdot(\sqrt{r}+1)}{8}\right) + \frac{1}{2} \\ &\quad \cdot ln\left(\frac{1+4\cdot(\sqrt{i}+\sqrt{r})}{5}\right) \end{aligned} \tag{A.3}$$

where:

$$r = i + \frac{1}{2}\cdot\sqrt{i} + 1 \tag{A.4}$$

Variables v and i are either equal to $v_p - v_s$ and i_f, or $v_p - v_d$ and i_r. The interpolation function given by Eqn. A3 has the same asymptotes as Eqn. 29, but it can unfortunately not be inverted to express the current as a function of the voltage as required in circuit simulators. Nevertheless, it can easily be tabulated and interpolated using Lagrangian polynomials.

A2. Exact Calculation of the Normalized Transconductance from Weak to Strong Inversion

The source transconductance can be expressed in terms of the inversion charge Q'_{inv} by differentiating Eqn. 20 with respect to V_S:

$$g_{ms} = \beta\cdot\frac{(-Q'_{inv})}{C'_{ox}} \tag{A.5}$$

Introducing Eqn. A5 in the expression of the transconductance interpolation function given by Eqn. 36 leads to:

$$G(i_f) = \frac{g_{ms}\cdot U_T}{I_F} = \frac{1}{2\cdot n\cdot i_f}\cdot\frac{(-Q'_{inv})}{U_T\cdot C'_{ox}} \tag{A.6}$$

where the forward normalized current i_f can be calculated by:

$$\begin{aligned} i_f &\equiv \frac{I_F}{2\cdot n\cdot\beta\cdot U_T^2} \\ &= \frac{1}{2\cdot n}\cdot\int_{v_s}^{\infty}\frac{(-Q'_{inv})}{U_T\cdot C'_{ox}}\cdot dv_{ch} \text{ where:} \\ v_{ch} &\equiv \frac{V_{ch}}{U_T},\ v_s \equiv \frac{V_S}{U_T} \end{aligned} \tag{A.7}$$

Combining equations (A6) and (A7) leads to:

$$G(v_s) = \frac{\frac{(-Q'_{inv})}{U_T\cdot C'_{ox}}}{\int_{v_s}^{\infty}\frac{(-Q'_{inv})}{U_T\cdot C'_{ox}}\cdot dv_{ch}} \tag{A.8}$$

This equation can be evaluated numerically for different parameters γ and V_{FB}. The result of this numerical calculation is plotted in Fig. 8 for $\gamma = 1\sqrt{V}$ and $V_{FB} = -0.96$ V corresponding to $V_{T0} = 0.6$ V.

A3. Channel Potential Versus Position

Having defined an interpolation function, it can be used to evaluate the non-equilibrium voltage V_{ch} along the channel from source to drain. Integrating the drain current from the source to an intermediate point x along the channel results in:

$$\begin{aligned} \frac{x}{L}\cdot I_D &= \underbrace{\beta\cdot\int_{V_S}^{\infty}\left[-\frac{Q'_{inv}(V)}{C'_{ox}}\right]\cdot dV}_{=I_F(V_P,V_S)} \\ &\quad \underbrace{-\beta\cdot\int_{V_{ch}(x)}^{\infty}\left[-\frac{Q'_{inv}(V)}{C'_{ox}}\right]\cdot dV}_{=I_x(V_P,V_{ch})} \\ &= \cancel{\frac{x}{L}}\cdot(I_F - I_x) \end{aligned} \tag{A.9}$$

where $V_{ch}(x)$ is the value of the channel potential at point x. The current I_x represents the drain current of a transistor working in the saturation region and having $V_{ch}(x)$ as source voltage. The corresponding normalized current i_x can thus be written as:

$$\begin{aligned} i_x(v_p - v_{ch}) &= i_f - \frac{x}{L}\cdot i_d \\ &= i_f - \frac{x}{L}\cdot(i_f - i_r) \end{aligned} \tag{A.10}$$

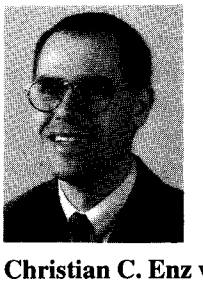
Eqn. A10 can be inverted using the interpolation function given by the inverse of Eqn. 30, in order to express the channel voltage as a function of position along the channel for a given value of the forward and reverse normalized currents (depending on the terminal voltages):

$$\begin{aligned} V_{ch}(x) &= V_P - 2\cdot U_T \\ &\quad \cdot ln\left\{e^{\sqrt{i_f - \frac{x}{L}\cdot(i_f - i_r)}} - 1\right\} \end{aligned} \tag{A.11}$$

Notice that a more accurate expression could be derived by using Eqn. A3 instead of the inverse of Eqn. 30.

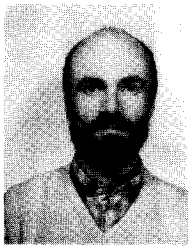
References

1. Y. P. Tsividis, *Operation and Modelling of the MOS Transistor*, McGraw-Hill, 1987.
2. C. C. Enz, "High precision CMOS micropower amplifiers," Ph.D. thesis, No. 802, EPFL, Lausanne, 1989.
3. E. A. Vittoz, "Micropower techniques," in *Design of MOS VLSI Circuits for Telecommunications*, edited by J. Franca and Y. Tsividis, Prentice-Hall, 1993.
4. E. A. Vittoz, "MOS transistor," Intensive Summer Course on CMOS & BiCMOS VLSI Design, Analog&Digital, Lausanne (EPFL), Switzerland, September 1993.
5. J. A. van Nielen and O. W. Memelink, "Influence of substrate upon the DC characteristics of MOS transistors," Philips Research Reports, vol. 22 pp. 55–71, 1967.
6. H. Wallinga and K. Bult, "Design and analysis of CMOS analog signal processing circuits by means of a graphical MOST model," *IEEE J. Solid-State Circuits* vol. SC-24 pp. 672–680, June 1989.
7. A. L. Silburt, R. C. Foss and W. F. Petrie,"An efficient MOS transistor model for computer-aided design," *IEEE Trans. Comput.-Aided Des.* vol. CAD-4 pp. 104–111, 1982.
8. N. D. Arora and L. M. Richardson,"MOSFET modeling for circuit simulation," in *Advanced MOS Device Physics*, edited by by N. G. Einspruch and G. S. Gildenblat, pp. 237–276, Academic Press, 1989.
9. N. D. Arora,"Semi-empirical model for the threshold voltage of double implanted MOSFET and its temperature dependence," *Solid-State Electronics* vol. 30 pp. 559–569, 1987.
10. H. C. Pao and C. T. Sah, "Effects of diffusion current on the characteristics of metal-oxide (insulator)-semiconductor transistors," *Solid-State Electronics* vol. 10 pp. 927–937, 1966.
11. J. D. Chatelain, "Dispositifs à semiconducteurs," *Traité d'électricité* vol. VII, Presses Polytechniques Romandes, 1979.
12. E. A. Vittoz,"MOS transistors operated in the lateral bipolar mode and their application in CMOS technology," *IEEE J. Solid-State Circuits* vol. SC-18 pp. 273–279, June 1983.
13. X. Arreguit, "Compatible lateral bipolar transistors in CMOS technology: model and applications," Ph.D. thesis N0817, EPFL, Lausanne, 1989.
14. W. Budde and W. H. Lamfried, "A charge-sheet capacitance model based on drain current modeling," *IEEE Trans. Electron Devices* vol. ED-37 pp. 1678–1687, July 1990.
15. A. I. A. Cunha, R. T.Gongalves, M. C. Schneider and C. G. Montoro, "An accurate and explicit physical model of the MOS transistor," *Proceedings of the 8th conference of the sociedade Brasileira de Microelectronica*, Sept. 1993.
16. B. J. Sheu, D. L. Scharfetter, P. K. Ko and M. C. Jeng,"BSIM: Berkeley Short-channel IGFET model for MOS transistors," *IEEE J. Solid-State Circuits* vol. SC-22 pp. 558–566, Aug. 1987.
17. J. A. Power and W. A. Lane, " An enhanced SPICE MOSFET model suitable for analog applications," *IEEE Trans. Computer-Aided Design* vol. CAD-11 pp. 1418–1425.
18. Y. Tsividis and K. Suyama,"MOSFET modeling for analog circuit CAD: Problems and prospects," *Proceedings of CICC '93*, San Diego, May 1993.
19. H. J. Oguey and S. Cserveny, "MOS modelling at low current density," Summer Course on "Process and Device Modelling," ESAT Leuven-Heverlee, Belgium, June 1983.
20. H. Oguey and S. Cserveny, "Modèle du transistor MOS valable dans un grand domaine de courants," *Bull. SEV/ VSE*, Feb. 1982.
21. Y. P. Tsividis, "Relation between incremental intrinsic capacitances and transconductances in MOS transistors," *IEEE Trans. Electron Devices* vol. ED-27 pp. 2383–2391, May 1980.
22. M. Bagheri and Y. Tsividis, "A small signal dc-to-high-frequency nonquasistatic model for the four-terminal MOSFET valid in all regions of operation," *IEEE Trans. Electron Devices* vol. ED-32 pp. 2383–2391, Nov. 1985.
23. M. S. Ghausi and J. J. Kelly, *Introduction to Distributed-Parameter Networks with Application to Integrated Circuits*, Holt, Rinehart and Winston, 1968.
24. P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, Wiley, 1977.
25. R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, Wiley, 1977.
26. H. Khorramabadi and P. R. Gray, "High-frequency CMOS continuous-time filters," *IEEE J. Solid-State Circuits* vol. SC-19 pp. 939–948, Dec. 1984.
27. R. Sarpeshkar, T. Delbrück, and C. A. Mead, "White noise in MOS transistors and resistors," *IEEE Circuits & Devices Magazine* vol. 9 pp. 23–29, Nov. 1993.



Christian C. Enz was born in Zürich, Switzerland, on December 24, 1957. He received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology, Lausanne (EPFL) in 1984 and 1989 respectively.

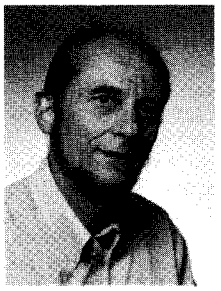
From 1984 to 1989 he has been research assistant at the EPFL, working in the field of micropower and high-performance analog CMOS integrated circuits design. In 1989 he was one of the founders of Smart Silicon Systems S.A. (S3), an IC design company established in Lausanne, Switzerland. In 1990 he became director of S3. Since 1991, he has been lecturing at the EPFL where he became an assistant professor in 1992. He is currently with the Electronics Laboratory of the EPFL. His current technical interests are in device modeling, in low-power analog CMOS circuit design, in SC and continuous-time filters, low-noise IC design for instrumentation and sensor interface. Prof. Enz has contributed to numerous publications, conference presentations and advanced engineering courses.



François Krummenacher was born in Lausanne, Switzerland, on April 29, 1955. He received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1979 and 1985, respectively.

Since 1979 he has been with the Electronics Laboratory of EPFL, working in the field of low-power and high performance analog CMOS integrated circuit design. From April to October 1983 he was with the Electrical Engineering Department of the University of California, Los Angeles, where he was involved in the design of MOS switched-capacitor circuits.

He is one of the founders of Smart Silicon Systems S.A., a company specialized in the design of mixed analog/digital ASIC's, where he is currently R&D Project Manager. He is also responsible for research activities in analog circuit design at the Electronics Laboratory of EPFL. Dr. Krummenacher has published over 40 papers on CMOS analog circuit design.



Eric A. Vittoz received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology in Lausanne (EPFL) in 1961 and 1969 respectively.

He joined the Centre Electronique Horloger S.A. (CEH), Neuchâtel, in 1962, where he participated in the development of the first prototypes of electronic watches. In 1971, he was appointed Vice-Director of CEH, supervising advanced developments in electronic watches and other micropower systems. In 1984, he took the responsibility of the Circuits and Systems Research Division at the Swiss Center for Electronics and Microtechnology (CSEM) in Neuchâtel, where he was appointed Executive Vice-President, Integrated Circuits and Systems, in 1991. He is also directly responsible for the Advanced Research section of CSEM. His field of personal research interest and activity is the design of low-power analog CMOS circuits, with emphasis on their application to advanced perceptive processing. Since 1975, he has been lecturing and supervising undergraduate and graduate student projects in analog circuit design at EPFL, where he became Professor in 1982. Dr. Vittoz is an IEEE fellow, has published more than 90 papers and holds 25 patents.